Co-Design and Abstraction of a Network-on-Chip Using Deterministic Network Calculus

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Abstract—Network-on-Chip (NoC) is the dominant paradigm for on-chip interconnects. Two approaches for architecting a NoC can be distinguished. One is the generalization of bus-based interconnects inside a SoC, where transactions are associated with memory addresses. The other is the on-chip integration of connection-oriented networks, which transport frames without addressing into the destination memory. Connection-oriented NoCs are well-suited to terminating macro-networks such as Ethernet, and to supporting quality of service (QoS) by using formal methods such as deterministic network calculus (DNC).

We present the design objectives and architecture of the NoC of the 3rd-generation Kalray MPPA processor, which implements a clustered manycore architecture. The MPPA3 NoC is connected to high-speed Ethernet controllers that operate at level-2 for networking and at level-1 to extend the NoC protocol across processors. By contrast with the time-triggered approach for ensuring QoS, this NoC is designed to guarantee delays by the adequate configuration of DMA engines and traffic limiters at ingress. We discuss the abstraction of the MPPA3 NoC network elements for the purpose of bounding delays by application of a DNC formulation. Delay bounding and the associated usage domains are motivated by time-critical applications.

Keywords—Network-on-Chip, Many-Core Processor, Network Guaranteed Services, Deterministic Network Calculus