Panel Discussions

“Challenges to the Scaling Limits: How Can We Achieve Sustainable Power-Performance Improvements?“

Abstract
Moore’s Law, doubling the number of transistors in a chip every two years, has so far been contributed to the evolution of computer systems, e.g., employing large on-chip caches, increasing DRAM (or main memory) capacity, introducing manycore accelerations, etc. The growth of such hardware implementation makes a lot of optimization opportunities available to software developers. Unfortunately, we cannot expect transistor shrinking anymore, i.e., the end of Moore’s Law will come. On the other hand, our society strongly requires sustainable computing efficiency for the next generation ICT applications such as AI, IoT, Big-Data, etc. To satisfy such requirements, we have to rethink computer system designs from the bottom. The goal of this panel is to discuss and explore the future direction of computer system architectures by focusing on especially high-performance, low-power computing such as data-centers and supercomputers. We first try to share the knowledge, experience, and opinions of our excellent panelists and then discuss the technical challenges to overcome the scaling limits for obtaining sustainable power-performance improvements.

Organizer & Moderator
Koji Inoue (Kyushu University)

Panelists
Takuya Araki (NEC)
Takumi Maruyama (Fujitsu)
Pritish Narayanan (IBM Research - Almaden)
Takashi Oshima (Hitachi)
Martin Schulz (Technische Universität München)
Organizer & Moderator’s Biography

Koji Inoue received the B.E. and M.E. degrees in computer science from Kyushu Institute of Technology, Japan in 1994 and 1996, respectively. He received the Ph.D. degree in Department of Computer Science and Communication Engineering, Graduate School of Information Science and Electrical Engineering, Kyushu University, Japan in 2001. In 1999, he joined Halo LSI Design & Technology, Inc., NY, as a circuit designer. He is currently a professor of the Department of I&E Visionaries, Kyushu University. His research interests include power-aware computing, high-performance computing, secure computer systems, 3D microprocessor architectures, multi/many-core architectures, nano-photonic computing, and single flux quantum computing.