Deep neural networks use the computational power of massively parallel processors in applications such as autonomous driving. Autonomous driving demands resiliency (as in safety and reliability) and trillions of operations per second of computing performance to process sensor data with extreme accuracy. This keynote examines various approaches to achieve resiliency in autonomous cars and makes the case for design diversity based redundancy.

**Bio:** Nirmal R. Saxena is currently a distinguished engineer at NVIDIA and is responsible for HPC and automotive resilient computing. From 2011 through 2015, Nirmal was associated with Inphi Corp as CTO for Storage & Computing and with Samsung Electronics as Sr. Director working on fault-tolerant DRAM memory and storage array architectures. During 2006 through 2011, Nirmal held roles as a Principal Architect, Chief Server Hardware Architect & VP at NVIDIA. From 1991 through 2009, he was also associated with Stanford University’s Center for Reliable Computing and EE Department as Associate Director and Consulting Professor respectively. During his association with Stanford University, he taught courses in Logic Design, Computer Architecture, Fault-Tolerant Computing, supervised six PhD students and was co-investigator with Professor Edward J. McCluskey on DARPA’s ROAR (Reliability Obtained through Adaptive Reconfiguration) project. Nirmal held senior technical and management positions at Alliance Semiconductors, Chip Engines, Tiara Networks, Silicon Graphics, HaL Computers, and Hewlett Packard.

Nirmal received his Ph.D. EE degree (1991) from Stanford University. He is a Fellow of the IEEE (2002) and was cited for his contributions to reliable computing.
Keynote 2

9:30 AM, Tuesday, March 13

Reliable Ultra-Low Energy Security Circuit Primitives for IoT Edge Systems, Sanu Mathew, Intel

Low-area energy-efficient security primitives are key building blocks for enabling end-to-end content protection, user authentication and data security in IoT platforms. This talk describes the design of reliable security circuit primitives with optimal arithmetic for seamless integration into area/battery constrained IoT systems: 1) A 2040-gate AES accelerator achieving 289Gbps/W efficiency in 22nm CMOS, 2) Hardened hybrid Physically Unclonable Function (PUF) circuit to generate a 100% stable encryption key. The talk will also discuss design issues related to side-channel leakage of embedded secret keys, and how they may be addressed during design of encryption circuits. We will also discuss the effect of aging on PUF circuits and techniques to handle aging issues over the lifetime of the die.

Bio: Sanu Mathew is a Senior Principal Engineer with the Circuits Research Labs at Intel Corporation, Hillsboro, Oregon, where he leads research and development of energy-efficient hardware accelerators for encryption and security. Sanu obtained his Ph.D. degree in Electrical and Computer Engineering from State University of New York at Buffalo in 1999. He holds 41 issued patents, with another 63 patents pending and has published over 77 conference/journal papers. He has been with Intel for the past 18 years. Sanu is a Fellow of the IEEE.
Real Limits to Nanoelectronics: Interconnects and Contacts
Krishna Saraswat, Stanford University

Modern electronics has advanced at a tremendous pace over the course of the last half century primarily due to enhanced performance of MOS transistors due to dimension scaling. Silicon bulk CMOS dominated the microelectronics industry in the past. However, future Si technology is reaching practical and fundamental limits. To go beyond these limits FinFETs have been introduced and novel device structures like surround gate FETs, TunneFETs, etc. and potentially higher performance material like Ge, III-Vs, carbon nanotubes and 2D materials are being aggressively studied. However, as device scaling continues, parasitic source resistance largely dominated by contact resistance, is beginning to limit the device performance. Historically the method to reduce $\rho_c$ is by increasing doping density thereby thinning the barrier, thus allowing more tunneling current. This method works well for n-Si and p-Ge which can be doped heavily. However, it is not very practical for n-Ge, p-Si, many III-Vs and 2D materials because of inability to dope them heavily. In this talk we will explore other alternatives to reduce contact resistance, such as, metastable doping, Fermi level de-pinning and band engineered heterostructures.

While novel structures and materials have enhanced the transistor performance, the opposite is true for the interconnects that link these transistors. Looking into the future the relentless scaling paradigm is threatened by the limits of copper/low-k interconnects, including excessive power dissipation, insufficient communication bandwidth, and signal latency for both off-chip and on-chip applications. Many of these obstacles stem from the physical limitations of copper/low-k electrical wires, namely the increase in copper resistivity, as wire dimensions and grain size become comparable to the bulk mean free path of electrons in copper and the dielectric capacitance. Thus, it is imperative to examine alternate interconnect schemes and explore possible advantages of novel potential candidates. This talk will address effects of scaling on the performance of Cu/low-k interconnects, alternate interconnect schemes: carbon nanotubes (CNT), graphene, optical interconnect, three-dimensional (3-D) integration and heterogeneous integration of these technologies on the silicon platform.