THE IEEE International Integrated Reliability Workshop (IIRW) is a special event that takes place every year at the beautiful Fallen Leaf Lake, CA, USA. This workshop brings together semiconductor reliability engineers and researchers to exchange ideas over four days in a friendly informal environment. The workshop focuses on the recent progress in research concerning the reliability of integrated devices and systems, and topics include electro-migration, advanced modeling, simulation and characterization techniques, FET Reliability from FinFETs to high-voltage devices (including transistors based on wide bandgap materials), package reliability, and reliability of Flash and emerging memories and novel devices.

In the year 2017, fifteen regular papers and eleven invited papers were presented for oral and poster sessions.

This special section is a representative selection of papers from IIRW 2017 for wider impact and dissemination to the semiconductor integrated device reliability community.

The four papers in this special section cover a broad spectrum of recent research topics, including new characterization methodologies for self-heating and EDMR at wafer level, new characterization of threshold voltage shift under real operation, and a study of ferroelectric device reliability of power devices.

In the first selected paper, Peter Paliwoda and coauthors present three different measurements methodologies for the electrical characterization of self-heating in FinFET at wafer level. Using three different types of integrated temperature sensors, authors showed that the self-heating is underestimated by 35% when sensed at neighboring devices.

In the second paper, Duane McCrory and coauthors report on a novel semiconductor device reliability technique that merges electrically detected magnetic resonance (EDMR) with a conventional semiconductor wafer probing station. This allows EDMR to be performed at wafer level without the need for a resonance cavity. Such a technique simplifies the EDMR detection scheme and offers promise for widespread EDMR adoption in semiconductor reliability laboratories.

In the third paper, Katja Puschkarsky and coauthors present a study of the threshold voltage hysteresis in SiC power MOSFETs. They present a measurement technique that enables the measurement of the real threshold voltage shifts during bipolar AC gate stress applied in typical applications. The authors investigate the capture and emission-time constants of charge trapping in the gate oxide and interface as a function of gate bias, finally showing that the threshold voltage hysteresis has no harmful effect on switching operation.

In the fourth paper, Milan Pesic and coauthors discuss the reliability (endurance and operation stability) of new memory concepts introduced by the discovery of the ferroelectric (FE) properties of HfO₂, that is, FE- and Anti-ferroelectric (AFE) devices. The physical mechanisms responsible for degradation of both FE and AFE memories were investigated by combining advanced characterization and modeling techniques. The much more stable and higher endurance of AFE devices were attributed to the lower energetic barrier and field to be applied for AFE memory operation.

I would like to thank all of the authors for their efforts in preparing manuscripts including new, expanded, or extended results compared to those included in the IIRW 2017 proceedings.

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