Review on Renewable Energy Source Fault Characteristics Analysis

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***Abstract*—The increase of renewable energy sources (RESs), especially wind power and photovoltaic, is bringing different fault features to the power system compared with the traditional synchronous generator, resulting in the urgent need for precise fault analysis. According to the sequentially activated fault features, the short circuit characteristics of RES can be divided into three fault stages. Within the staged framework of fault duration, the published research is reviewed to provide a systematic analysis of RES fault characteristics. It's concluded that the hardware parameter determines the sub-transient fault features of RES, whereas RES control begins to dominate during the following transient stage. However, the neglection of voltage transition and unavailable RES output phase shall impede the application of the analytical conclusions in protection design. To solve the existing problems, interaction among RES and networks must be figured out. Therefore, the fault calculation of the integral RES-grid system is offered as the research prospect.**

***Index Terms*—Fault characteristics analysis, fault stages, renewable energy sources.**

I. Introduction

With the increasing application of renewable energy sources (RESs) throughout the world, the power system's operations are changing from synchronous generator (SG) domination to RES domination [1], [2]. The limited fault current amplitude and distorted waveforms of RESs are leading challenges to the conventional protection methods [3]–[7]. Accordingly, new protection methods oriented to RES connected systems have been developed. These novel protections use the modified power-frequency current [8]–[10], fault transient [11], [12], and traveling waves [13], [14] for better performance. However, there are problems in the protection settings considering the RES faulted features in different stages. To address these issues, a full investigation of RES fault characteristics is required.

Despite the knowledge that RES is of low inertia due to the rapid reaction feature of power electronic converters, the fault response of RES does present explicit staged features rather than changing in an instant [15], [16], as the field recordings shown in Fig. 1. As it can be observed in Fig. 1(a), the fault current of PV has a brief spike (I_{a}) and distortion during the initial period (within 5 ms) after fault inception ($t = 0$), marked as *Stage-1*. After that, there is a transitional duration for about 30 milliseconds (marked as *Stage-2*) until the fault current reaches steady state (marked as *Stage-3*). Likewise, the fault current of DFIG also presents staged features in Fig. 1(b). This stage division is intuitively made according to the waveform features of RES outputs. From the perspective of the internal mechanism, RES's fault response stage can be defined more rationally by the different bandwidth of each control loop and sequential switching of controls [17]–[19], which is furtherly discussed in Section II. Comparison of fault stages of SG and RES, as well as the definition of each stage, is depicted in Fig. 2, where IIG refers to the inverter interfaced generations (such as PV and Type-4 WT). Except for the shorter duration of each stage, the fault stage division of RES is different from SG which depends on the different time constants of the current attenuation components. Fault stage division helps to obtain a better knowledge of the influencing factors of RES fault characteristics.

Aimed at the widely used IIG- and DFIG-type RESs, the existing fault characteristics research has been undertaken in regards to the three fault stages. For the IIG-type RES, the current distortion within the sub-transient stage (STS) was discussed in [20]. Research on fault transient stage (FTS) characteristics was primarily about the impacts of proportional-integral (PI) controller parameters [21]–[25], PI windup [26]–[28] and phase-locked loop (PLL) delay on IIG fault transient characteristics [29], [30]. The features of current limiting and negative sequence control during fault steady stage (FSS) had been fully studied in [19], [31]–[42]. Regarding the DFIG-type RES, the fault features within the STS stage are analyzed in [43]–[45]. The FTS characteristics research was primarily about the rotor converter control [46]–[51] and crowbar [52]–[57]. Fault steady state characteristics were analyzed in [58]–[61]. As the published research partially focuses on different individual stages, a complete cognition of the RES fault characteristics is needed.

This paper attempts to provide a systematic analysis of RES fault characteristics and to offer the various research prospects. The remainder of this paper is organized as follows. The generic structure and dynamic property of RESs are overviewed to further illustrate the fault stage division of RES in Section II. Based on the perspective of staged-fault

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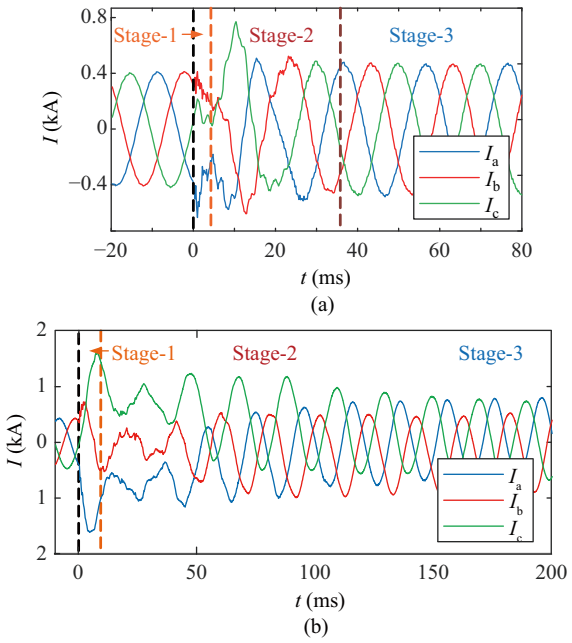

Fig. 1. Field recordings of RESs' fault currents. (a) PV; (b) DFIG-based WT.

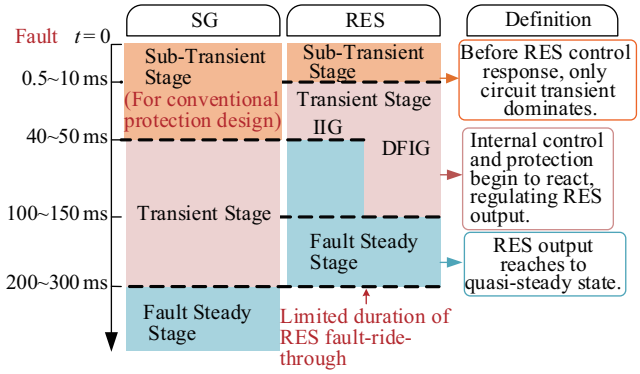

Fig. 2. Division and definition of RES fault response stages.

response, Section III contains the analysis of various factors within different RES fault stages and the review of the existing research. The current challenges and research prospects of RES fault characteristics analysis are provided in Section IV. Finally, Section V provides the conclusions.

II. Overview of RES Structure and Dynamic Property of RES

The overview of the RES structure is the basis of RES fault characteristics analysis. In this section, structures and dynamic performances of the two types of widely applied RESs are introduced.

A. Structure and Dynamic of IIG

Despite the various control strategies and hardware configurations used in IIG, the main structure is composed of outer/inner feedback control loops, PLL, pulse width modulation (PWM), and filter, as depicted in Fig. 3. The *dq*-reference frame control type and LCL filter, widely adopted in grid-connecting IIG, are used for illustration. Figure 4 shows the relationship of IIG output current and references, and voltage disturbance. Superscript '*' denotes the reference, and the single quotation mark denotes the quantity used in the control system. After fault occurrence, the outer loop is usually shut for faster tracking speed, where only the inner loop works. Among the blocks, $G_{\mathrm{PI}}(s)$ depends on the current feedback loop controller, $G_{\mathrm{PWM}}(s)$ represents the gain of PWM modulation, $G_{\mathrm{F}}(s)$ is the transfer function of the inverter filter, $H_{\mathrm{S}}(s)$ is the sensor gain and $H_{\mathrm{T}}(s)$ is the gain of *Park* transformation caused by PLL. As can be simply derived from the block diagram, the inverter controller and filter jointly determine the output current $i_{d,q}$, as (1) shows.

$$i_{d,q} = F_{\mathrm{C}}(s) i^{*}_{d,q} + F_{\mathrm{F}}(s) \cdot [u_{d,q} \pm \omega L i_{q,d}] \tag{1}$$

Different controls involved in IIG, seen as inertial systems, respond to the disturbance at different speeds due to their various dynamic performances. The most prevalent tuning method for the two main parts, current controller and filter, is suggested by the IEEE technological report [62] and published guideline [63].

$$k_p = \omega_c L \quad k_i = \omega_c R \tag{2}$$

where k_p, k_i are parameters of PI controller, and ω_c is the cut-off frequency [29]. Considering the parameters tuning, the bandwidth of the closed current control loop is about 0.5∼7 times the power frequency (50 or 60 Hz) [64]. The bandwidth of the LCL filter is generally set 10 times higher than the current controller for better harmonic attenuation capability and to avoid unwanted interactions [23]. In other words, voltage drop takes the lead in determining IIG output current via filter, within 0.5∼5 ms after fault inception [29]. Subsequently, the current controller rises to dominate IIG fault characteristics.

B. Structure and Dynamic of DFIG

The DFIG is composed of an induction generator, rotor side converter (RSC), grid side converter (GSC), auxiliary protection (i.e., crowbar and chopper), and wind turbine, as is shown in Fig. 5. The converter controller is the same structure as that of IIG, readers can refer to [43] for more detail. As the GSC is typically rated at lower than 30% of the total capacity [45], [46], fault characteristics of DFIG are primarily dominated by the RSC-controlled generator. The equivalent circuit of DFIG is also depicted in Fig. 5, where U_{rdq} is the excitation voltage controlled by RSC, I_{rdq} is the rotor current, R and L are resistance and inductance respectively, ψ is the flux linkage, subscripts "r" and "s" represent rotor and stator winding respectively, L_{m} is the magnetizing inductance among rotor and stator, ω_{s} and ω_{r} are the synchronous and rotating angular frequencies, U_{sdq} and I_{sdq} are the voltage and current of the stator. The basic circuit equation of DFIG can be given as:

$$\begin{cases} u_{\mathrm{s}} = R_{\mathrm{s}} i_{\mathrm{s}} + \mathrm{j}\omega_{\mathrm{s}} \psi_{\mathrm{s}} + \mathrm{d}\psi_{\mathrm{s}}/\mathrm{d}t \\ u_{\mathrm{r}} = R_{\mathrm{r}} i_{\mathrm{r}} + \mathrm{j}\omega_{p} \psi_{\mathrm{r}} + \mathrm{d}\psi_{\mathrm{r}}/\mathrm{d}t \\ \psi_{\mathrm{s}} = L_{\mathrm{s}} i_{\mathrm{s}} + L_{\mathrm{m}} i_{\mathrm{r}} \\ \psi_{\mathrm{r}} = L_{\mathrm{m}} i_{\mathrm{s}} + L_{\mathrm{r}} i_{\mathrm{r}} \end{cases} \tag{3}$$

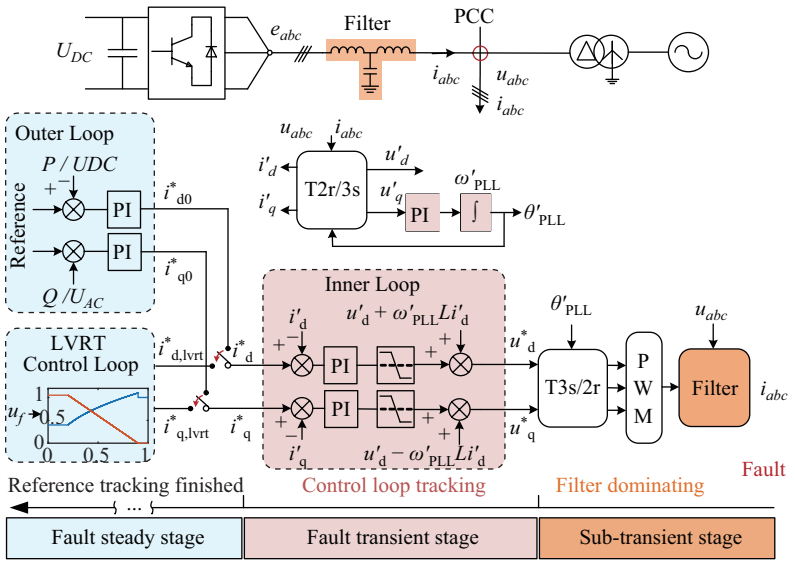

Fig. 3. Schematic generic control and hardware structure of IIG-type RES.

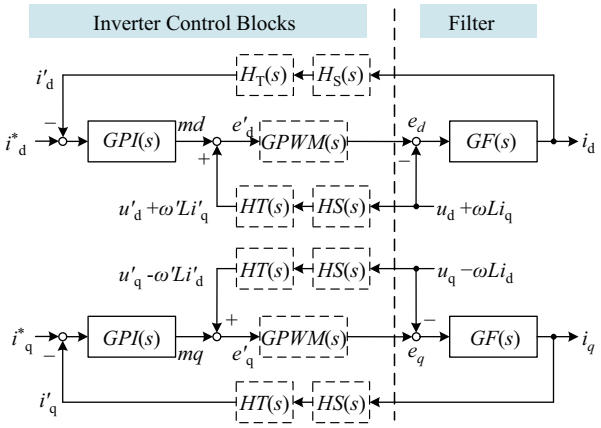

Fig. 4. Block diagram of IIG output current and reference, voltage.

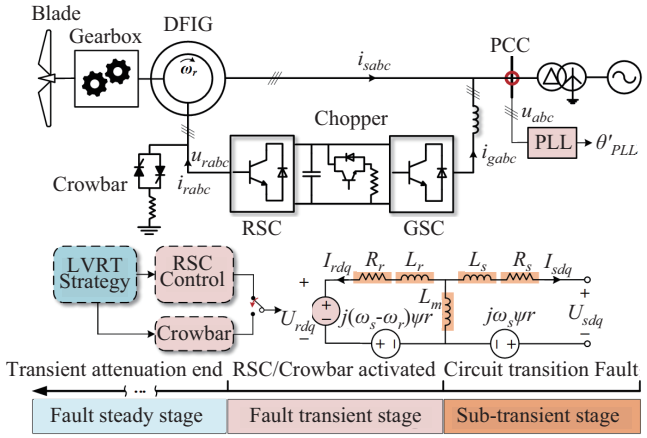

Fig. 5. Schematic structure of DFIG-type RES.

where u, i and ψ are voltage, current and flux respectively, subscripts s and r refer to the stator and rotor quantities, $\omega_p = \omega_s - \omega_r$, $L_s = L_m + L_{\sigma s}$, $L_r = L_m + L_{\sigma r}$, wherein $L_{\sigma s}$ and $L_{\sigma r}$ are the leakage inductances of stator and rotor. Intuitively, the DFIG output current can be deduced from the flux.

During short-circuit fault, sequential switching of DFIG control determines the fault characteristics of DFIG within different stages. The RSC reacts to the voltage drop by modulating the excitation voltage, to achieve fault-ride-through. During the severe fault condition, the crowbar is switched on to protect the semiconducting devices and energy storage elements from overload. But before the crowbar triggering, there is a brief ramping period of rotor current to the preset threshold. The time delay of crowbar action is determined by the voltage dips, rotating speed, and DFIG capacity [45]. Therefore, the initial fault stage (STS) of DFIG can be defined according to the switching of the RSC control and crowbar. Note that GSC accompanied with the chopper barely impacts the RSC and can be considered as a constant voltage source. After the excitation voltage is altered, the transition of the armature reaction involved in the generator dominates the fault features of DFIG. This transient stage would last for about 100∼150 ms depending on the time constants of the windings.

Although there are differences between the two types of RESs, both possess the generic cascaded structure of power electronic converter and electric circuit. The dynamics of the cascaded structure contributes to the complicated fault features of RES. As a result, the whole process of RES fault response can be divided into different stages as shown in Fig. 2. Hereinafter, the fault characteristics analysis of RES and review of the relative literature are classified by the three fault stages.

III. Fault Characteristics Analysis of RES by Stages

In this section, RES fault characteristics during different fault stages are resumptively analyzed.

A. Fault Characteristics in Sub-Transient Stage

As the reaction of control cannot be instant, fault characteristics of RES within the sub-transient stage are dominated by

the nature of the hardware, i.e., filter of IIG and coil circuits of DFIG.

1) IIG-Type RES

At the initial period after grid fault inception, distortion and initial transient spike exist in IIG output current by observation of fault recording and simulations [23]. Such a transitory period is not related to the control loop due to relatively low control bandwidth. The main contribution of the current distortion comes from the inverter filter [20] which can be analyzed as:

$$i_{d,q} = \frac{T(s)}{1+T(s)}\frac{1}{H_{\mathrm{S}}(s)}i^*_{d,q} - \frac{G_{x2}(s)}{1+T(s)}u_{d,q} \tag{4}$$

where $i_{d,q}$ refers to d,q component output current, $T(s)$ depends on the loop gain of current loop and PWM delay, G_{x2} depends on the inverter filter, s is the *Laplace* operator.

As the filter has a much higher bandwidth than the current control loop, the contribution from reference i^*_k through the control loop is regarded as constant. IIG output current during the sub-transient stage was cursorily deduced as the spike current with exponential decay.

$$i^{STS}_{d,q}(t) = i_{d,q0} + I_{\text{spike}}\mathrm{e}^{\frac{-t}{T''}} \tag{5}$$

where the superscript *STS* refers to fault sub-transient stage, $i_{d,q0}$ is the pre-fault current value, T'' is an approximated decay time constant, and I_{spike} is an empirical peak value obtained from EMT lab tests. Equation (4) indicates that IIG output current not only depends on the reference current but also on the voltage at the point of common coupling (PCC).

An intuitive explanation is that the initial spike of IIG current has its roots in the release of energy stored in the inverter filter. As the filter discharging would be faster than the inverter controller response, the dynamic of the filter dominates fault characteristics within the IIG sub-transient stage. In addition, the delay of sensor and PWM may play an important role during this brief period.

2) DFIG-Type RES

As mentioned above, RSC control and crowbar cannot be activated instantly at the occurrence of grid fault, there is a brief sub-transient stage for a few milliseconds wherein only armature reaction among the rotor and stator windings dominates DFIG's behavior. According to the well-known theory of constant flux linkages and the concept of trapped flux, voltage dips would introduce transient flux components into both rotor and stator coils. For the stator coil part, there are steady synchronous frequency flux, DC attenuation flux determined by the stator circuit transient time constant, and the rotor-speed frequency (induced by the rotor-side DC flux) attenuation flux determined by the rotor circuit transient time constant. Based on equation (3), DFIG output current within the sub-transient stage can be furtherly deduced as:

$$i^{STS}_{\mathrm{s}}(t) = A_{\mathrm{s}}\mathrm{e}^{\mathrm{j}\omega_{\mathrm{s}}t} + B_{\mathrm{s}}\mathrm{e}^{-\tau_{\mathrm{s}}t} + C_{\mathrm{s}}\mathrm{e}^{\mathrm{j}\omega_{\mathrm{r}}t}\mathrm{e}^{-\tau_{\mathrm{r}}t} \tag{6}$$

where i^{STS}_{s} is sub-transient current of DFIG, τ_{s}, and τ_{r} are the time constants of stator and rotor circuits as shown in (7), A_{s}, B_{s} and C_{s} are the amplitudes of each component respectively (see [43], [45]).

$$\begin{cases} \tau_{\mathrm{s}} = R_{\mathrm{s}}L_{\mathrm{r}}/(L_{\mathrm{s}}L_{\mathrm{r}} - L^2_{\mathrm{m}}) \\ \tau_{\mathrm{r}} = R_{\mathrm{r}}L_{\mathrm{s}}/(L_{\mathrm{s}}L_{\mathrm{r}} - L^2_{\mathrm{m}}) \end{cases} \tag{7}$$

As the fault characteristics of DFIG within the sub-transient stage are determined by the natural response of the induction generator, the short circuit current shown in (6) is similar to that of SG due to the delay of crowbar triggering [43], [45]. In this case, the superposition of the pre-fault steady-state solution and zero-state responses to the equivalent fault sources is carried out in [45].

B. Fault Characteristics in Transient Stage

Within the fault transient stage, the internal control and protection of RES rise to dominate, conjointly determining the transient output. Note that the circuit transient process continues within this period.

1) IIG-Type RES

For the IIG-type RES, the major influencing factors include PI controller parameters, windup of PI controller, and PLL delay. Hereinafter, these factors are respectively analyzed.

PI Controller Parameters: Following the sub-transient stage, IIG switches to low voltage ride-through (LVRT) control generally executed by the current controller (the inner loop). PI controllers regulate output current to reach the reference $i^*_{d,q}$ calculated according to the LVRT strategy. As the design of voltage feedforward compensation decoupling, output $i_{d,q}$ are expected to be determined by its reference respectively. On this basis, the transient current output of IIG could be regarded as the response of the PCC voltage drop through the governing equation in [21], [22]. The transient current $i_{d,q}$ (in per-unit value) can be seen as the response of the second-order closed-loop transfer function of the current control loop.

$$i_{d,q} = \frac{k_p s + k_i}{Ls^2 + (R+k_p)s + k_i}i^*_{d,q} \tag{8}$$

where k_p, k_i are PI controller parameters, L is the filter inductance, R is the parasitic resistance of the filter inductance. Calculation of output current based on the frequency domain (S-domain) function is straightforward, yet lacking the ability to consider nonlinearity factors, such as PI saturation.

Literatures [23]–[25] took another approach by solving the current equation in the time domain (T-domain). Based on the simultaneous equations of the current control loop and filter-branch, a second-order differential equation about $i_{d,q}$ would be derived as:

$$\frac{\mathrm{d}^2 i_{d,q}}{\mathrm{d}t^2} + \frac{R+k_p}{L}\frac{\mathrm{d}i_{d,q}}{\mathrm{d}t} + \frac{k_i}{L}i_{d,q} = \frac{k_i}{L}i^*_{d,q} \tag{9}$$

The characteristic equation roots of (9), i.e., the parameter setting of k_p, k_i, L, and R, would determine the solution form of $i_{d,q}$ [21], influencing not only the value but also the attenuation components of IIG transient current. But for the most prevalent tuning method of the inverter [65] as described in (2), there would be dual real roots of (9). Therefore, the IIG transient current solution can be deduced as:

$$i^{FTS}_{d,q} = I_{\mathrm{T}1}\mathrm{e}^{r_1 t} + I_{\mathrm{T}2}\mathrm{e}^{r_2 t} + i^*_{d,q} \tag{10}$$

where the superscript *FTS* refers to the fault transient stage.

$$r_{12} = 0.5\left(-k_p/L \pm \sqrt{(k_p/L)^2 - 4k_i/L}\right) \tag{11}$$

$$\begin{cases} I_{\mathrm{T}1} = (i_{d,q0} - i^*_{d,q})(r_2 L/k_p + 1) \\ I_{\mathrm{T}2} = -(i_{d,q0} - i^*_{d,q})(r_1 L/k_p + 1) \end{cases} \tag{12}$$

As seen from (10)–(12), parameters of the PI controller in the current loop, combined with filter parameters determine both the amplitude and attenuation rate of the exponential term of IIG transient current.

Windup of PI Controller: To avoid sharp current surge during disturbance for inverter protection, the integral windup is generally designed to restrict the speed of current change in the PI controller [26]. For severe fault cases, windup would cause the PI controller to first operate in a nonlinear region and shift into a linear region [26]. Note that PI saturation is designed to restrict the change rate of the output current, while the current limitation is the restriction on the current reference value.

Literatures [27] and [28] studied the impact of PI windup on IIG fault response. PI saturation leads to PI output restricted as the threshold value M, resulting in the current feedback control switches from the second-order system shown in (8) which switches to the first-order system as shown in (13).

$$i_{d,q}(s) = \frac{1}{sL + R} M \tag{13}$$

The piecewise linearization method in T-domain is suitable to analyze the impact of PI windup during IIG fault response. By calculating the time for PI to quit the saturation region via (14), the transition of the PI state can be analytically modeled in the IIG fault response. Output current during PI saturation can be deduced as (15).

$$k_p(i^*_{d,q} - i_{d,q}) + k_i \int (i^*_{d,q} - i_{d,q})\mathrm{d}t = M \tag{14}$$

$$\hat{i}^{FTS}_{d,q} = \left(i_{d,q0} - \frac{M}{R}\right)\mathrm{e}^{-\frac{R}{L}t} + \frac{M}{R} \tag{15}$$

where the symbol " ˆ " is used to distinguish transient current within PI saturation and the transient current within the PI linear region shown in (10). It is worth noting that [28] also contains the verification of the field fault test in a wind power plant, proving the impact of PI saturation on RES fault transient characteristics.

PI saturation may restrict the current change speed in the initial period of IIG fault response. PI saturation state may cause the sole exponential attenuation term in the transient current, of which the amplitude depends on PI saturated threshold M and the time constant depends on filter-branch. To take the impact of PI saturation into consideration of the IIG fault transient analysis, the mathematical model of staged linear differential equation in T-domain is more applicable.

Phase Tracking Delay of PLL: For the dq-frame grid-connecting IIG, decoupled control based on current feedback compensation is realized under the premise of accurate phase locking. However, PLL is designed for steady state operations. For an abrupt disturbance, PLL cannot track the PCC voltage phase in real-time, which causes re-coupling of the dq current control loops during the fault transient stage. The re-coupled control loops complicate IIG behavior by altering the linear system in (8) to a nonlinear coupled system.

Literatures [29] and [30] studied the delay impact of SRF-PLL and DSOGI-PLL on fault transient current of IIG, respectively. For SRF-PLL, phase-locking delay comes from the PI controller involved in PLL. Based on the deduction of the small-signal model of SRF-PLL as is depicted in (16), PLL tracked phase θ_{PLL} after disturbance can be expressed as the true phase of voltage plus exponential decay terms as (17) shows.

$$U(\theta - \theta_{\mathrm{PLL}})\left(k_{p\mathrm{PLL}} + \frac{k_{i\mathrm{PLL}}}{s}\right) = s\theta_{\mathrm{PLL}} \tag{16}$$

$$\theta_{\mathrm{PLL}}(t) = \theta(t) + \Delta\theta\left[\frac{k_1}{2\lambda}\exp(-k_1 t) - \frac{k_2}{2\lambda}\exp(-k_2 t)\right] \tag{17}$$

where U is the amplitude of PCC voltage, θ is the real-time phase of the voltage, $k_{p\mathrm{PLL}}$, $k_{i\mathrm{PLL}}$ are parameters of PI in PLL, coefficients λ, k_1, k_2 depend on $k_{p\mathrm{PLL}}$, $k_{i\mathrm{PLL}}$, and U, of which the specific definitions refer to [30]. The impact of PLL delay would cause recoupled terms between dq current control as expressed in (18), a variant of (9).

$$\frac{\mathrm{d}^2 i_{d,q}}{\mathrm{d}t^2} + \frac{R + k_p}{L}\frac{\mathrm{d}i_{d,q}}{\mathrm{d}t} + \frac{k_i}{L} i_{d,q} \pm \overbrace{\Delta\omega \frac{\mathrm{d}i_{q,d}}{\mathrm{d}t}}^{\text{Recoupled Terms}} = \frac{k_i}{L} i^*_{d,q} \tag{18}$$

where $\Delta\omega$ is the frequency error caused by PLL tracking delay. By substitution decoupling, IIG transient current considering PLL delay can be deduced as:

$$\begin{aligned} \tilde{i}^{FTS}_{d,q}(t) = {} & A_{d,q}\cos(\beta t + \mu_1)\mathrm{e}^{\eta_1 t} \\ & + B_{d,q}\cos(\delta t + \mu_2)\mathrm{e}^{\eta_2 t} + i^*_{d,q} \end{aligned} \tag{19}$$

where the specific introductions of the involved coefficients refer to [30]. It indicates that dq-recoupling caused by SRF-PLL delay would lead to the form change in current attenuation terms.

For DSOGI-PLL, designed for asymmetrical operations, a considerable delay effect of DSOGI results in more complex transient behavior of IIG. Fig. 6 illustrates the structure of DSOGI-PLL. The positive and negative sequences are separated through SOGI, which is a second-order function.

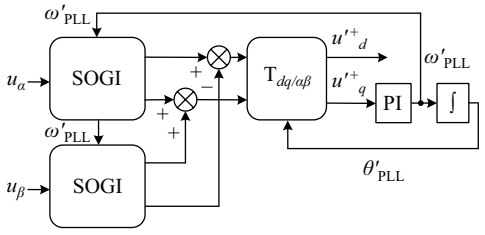

Fig. 6. Schematic diagram of DSOGI-PLL.

Literature [29] analyzed the transient current of IIG equipped with DSOGI-PLL. The conclusion is that the delay of SOGI would lead to coupling among dq currents in positive

and negative sequences, which makes it difficult to obtain an explicit solution for the current.

$$\boldsymbol{I}=\frac{G_{\mathrm{PI}}(s)\boldsymbol{I}^{*}+\boldsymbol{H}\boldsymbol{U}-\boldsymbol{U}}{sL+R+G_{\mathrm{PI}}(s)\boldsymbol{H}+\boldsymbol{E}-\omega L\boldsymbol{J}\boldsymbol{H}\boldsymbol{I}} \tag{20}$$

where the bold symbols represent the matrix, of which the specific definition refers to [29]. Compared to (8), it's evident that the delay introduced by DSOGI-PLL causes the current references and voltage components to jointly determine the output current. By using the balancing-free square-root algorithm [66], a simplified current solution is deduced in [29].

$$\begin{aligned}\tilde{i}_{d,q}^{FTS}(t)=&\,i_{d,q}^{*}+C\sin(\omega_n t)\mathrm{e}^{-\eta_3 t}\\&+u_{d,q}\left[D\mathrm{e}^{-\eta_4 t}+F\sin(\omega_n t)\mathrm{e}^{-\eta_5 t}\right]\end{aligned} \tag{21}$$

where the current formula shown in (21) is used to illustrate the transient current composition, with a detail explanation being omitted. Compared with (10) and (19), (21) indicates that delay effect of DSOGI-PLL would bring a much more complex composition of IIG transient current. The different sequences of d,q currents, as well as voltage, collectively determine the IIG output characteristics.

2) DFIG-Type RES

DFIG may trigger different actions according to the degree of voltage dips, including RSC LVRT control, crowbar, and chopper. Among them, the chopper is used to suppress the DC-link voltage, which contributes little to the DFIG output. The first two actions would alter the rotor-side circuit, causing the vital change of DFIG fault characteristics. The fault transient features of DFIG are determined by the RSC control and crowbar control.

RSC Control: During the fault ride-through, RSC control is analogous to the IIG control, which is executed via the inner current loop. Literature [46] pointed out that RSC control cannot act faster than the initial fault current spike in view of the controller bandwidth. Within the fault transient stage, the process of RSC reference tracking would be superimposed on the transition of the rotor-side circuit, further influencing the stator current. The closed-loop transfer functions of the short circuit current were developed in [48]–[51] to derive the approximate expressions for time constants and current solutions. The excitation voltage controlled by RSC can be expressed as (22).

$$u_{\mathrm{r}}=k_p(i_{\mathrm{r}}^{*}-i_{\mathrm{r}})+k_i\int(i_{\mathrm{r}}^{*}-i_{\mathrm{r}})\mathrm{d}t+\mathrm{j}\frac{\omega_p}{L_{\mathrm{s}}}(1-L_{\mathrm{m}}^{2})i_{\mathrm{r}} \tag{22}$$

where u_{r}, i_{r} and i_{r}^{*} are the dq-frame quantities. By incorporating (22) with the DFIG circuit equation (3), the transient current of DFIG with RSC control can be derived as:

$$i_{\mathrm{s}}^{FTS}(t)=A_{\mathrm{sR}}\mathrm{e}^{\mathrm{j}\omega_{\mathrm{s}}t}+B_{\mathrm{sR}}\mathrm{e}^{-\tau_{\mathrm{s}}t}+C_{\mathrm{sR}}\mathrm{e}^{\mathrm{j}\omega_{\mathrm{r}}t}\left(\beta_2\mathrm{e}^{\beta_1 t}-\beta_1\mathrm{e}^{\beta_2 t}\right) \tag{23}$$

where A_{sR}, B_{sR}, and C_{sR} refer to [48]–[50], β_1 and β_1 are relative to the parameters of the RSC controller and circuits. Compared with (6), dynamics of the RSC controller would introduce additional rotor-speed decaying components, of which the decay rates are relative to the RSC controller.

Crowbar Control: The crowbar is used to protect RSC from overcurrent for the severe voltage dip condition. During the crowbar operation, the DFIG acts like a classical induction machine. As is illustrated in Fig. 7, the equivalent circuit almost remains the same as Fig. 5, except for the crowbar resistance replacing the excitation voltage. Literatures [52]–[57] had analyzed DFIG fault current with the crowbar being activated. The stator current with crowbar being activated can be depicted as (24).

$$\hat{i}_{\mathrm{s}}^{FTS}(t)=A_{\mathrm{sC}}\mathrm{e}^{\mathrm{j}\omega_{\mathrm{s}}t}+B_{\mathrm{sC}}\mathrm{e}^{-\tau_{\mathrm{s}}t}+C_{\mathrm{sC}}\mathrm{e}^{\mathrm{j}\omega_{\mathrm{r}}t}\mathrm{e}^{-\tau_{\mathrm{rC}}t} \tag{24}$$

$$\tau_{\mathrm{rC}}=R_{\mathrm{rC}}L_{\mathrm{s}}/(L_{\mathrm{s}}L_{\mathrm{r}}-L_{\mathrm{m}}^{2}) \tag{25}$$

where A_{sC}, B_{sC} and C_{sC} refer to [52], [53], τ_{rC} is the time constant of the rotor circuit after the crowbar protection is acted upon, $R_{\mathrm{rC}}=R_{\mathrm{r}}+R_{\mathrm{C}}$. It can be seen from (25) that the decay of the rotor-speed frequency attenuation component would be faster with a larger crowbar resistance.

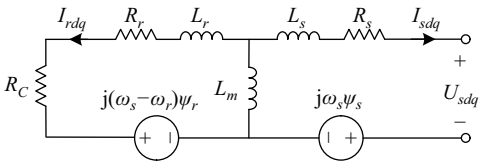

Fig. 7. Equivalent circuit of DFIG-type RES with the crowbar activated.

C. Fault Characteristics in Steady Stage

With the completion of fault control command tracking, RES output enters the quasi-steady stage. Within the duration of LVRT (150 ms $\sim$ 2 s stipulated in grid codes [67]–[69]), the fault steady state current of RES is determined by current limitation and the specific control strategy.

For the fault steady stage characteristics analysis, both IIG- and DFIG-type RESs, can be modeled as controlled current sources for different control modes. In modeling studies, current limitation and LVRT strategy are well-considered. RES current is generally limited as 1.2–2 p.u. to protect the fragile semiconductors of the inverter. The current limitation is exerted at the reference value of the current feedback loop, i.e., $|i_d^{*}+ji_q^{*}|\le I_{\mathrm{th}}$. The ratio of i_d^{*} and i_q^{*} determines the IIG output power during LVRT. Literatures [33], [34] provided analyses on the U-I relationship of RES during fault and established equivalent current source models. [35]–[37] refined the equivalent model, considering the relationship between PCC voltage drop and RES reactive current output.

For the case of an asymmetrical fault, the flexible sequence decoupled control strategy to achieve particular control objectives related to the current harmonics and power oscillations is proposed in [19]–[32]. Literatures [38]–[42], [58]–[61] proposed positive and negative sequence voltage source models to characterize the RES output subjected to the asymmetric fault. Thereinto, [42] contained the field test analysis of asymmetrical fault in an 850 MW PV power plant.

Fault characteristics of RES within the fault steady stage is predictable for its controllability. Various control strategies, such as reactive power support, negative sequence restrain, would help characterize RES fault steady stage characteristics. The brief summary of the published RES fault characteristics research focusing on various fault stages and impact factors are listed in Table I.

TABLE I
SUMMARY OF THE PUBLISHED RES FAULT CHARACTERISTICS RESEARCH

Fault Stage	RES Type	Literature	Considered Factors	Impact on RES Fault Current
Sub-Transient Stage	IIG	[20]	Filter dynamic	Initial current spike within brief period (5).
	DFIG	[43]–[45]	Transition of stator and rotor circuits	Induced DC and rotor speed frequency attenuation component (6).
Fault Transient Stage	IIG	[21]–[25]	Parameters of PI controller in current loop	Exponential attenuating current components (10).
		[26]–[28]	Windup of PI controller	Restricted current changing rate; Distinct staged response (15).
		[29], [30]	Phase tracking delay of PLL	Recoupling among different control loops; Additional exponential attenuating current components (19)(21).
	DFIG	[46]–[51]	RSC controller	Additional rotor-speed decaying components relative to RSC control parameters (23).
		[52]–[57]	Crowbar resistance	Changing amplitudes of transient current and decay rates of the rotor-speed frequency attenuation component (24).
Fault Steady Stage	Both	[33]–[37]	Current limitation and reactive power support	Limited fault-steady-state current amplitude.
		[19]–[32], [38]–[42], [58]–[61]	Decoupled sequence control	Predictable fault steady output for various control objectives.

IV. CURRENT CHALLENGES AND RESEARCH PROSPECTS

Though the study on RES fault characteristics of different stages is daily inclusive, the deduced formulas of RES fault current in published research is incapable of direct application for protection design. This is due to two assumptions commonly used in the existing research:

Assumption 1. Voltage of PCC step descends after fault occurrence without any appreciable transient component.

Considering that voltage drop can be seen as the input of the RES control, transforming the fault current analysis to step function response of the control loop would greatly simplify the deduction progress, achieving neat formulas. But this assumption only stands for the fault case of the metallic short circuit at the RES output line with integration to an infinity system. Thevenin impedance of the integrated system, as depicted in Fig. 8, can simply indicate how fast the transient component of the voltage waveforms will decay [17] ($\tau_{\text{th}} = L_{\text{th}}/R_{\text{th}}$ is the time constant of the voltage drop). For the forthcoming power system with high penetration of RES and other power electronic devices, the integrated system will be weak, resulting in voltage drop with the non-negligible transition. This would lead to complications in RES fault analysis.

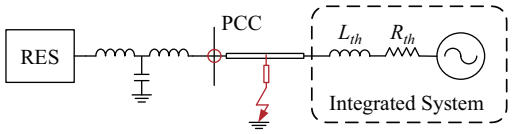

Fig. 8. Diagram of single RES integrated to the weak power system.

Assumption 2. RES output phase during fault is assumed available.

In view of the fault current deduction of RES is generally carried in dq-axis for convenience of calculation, the output phase locked by PLL is still needed for transforming the dq current components into three-phase quantities, as is shown in Fig. 9. A common way of dealing with this problem is to assume an available phase, which is unpractical for engineering applications. This will result in the existing derived fault current formulas not being directly cumulative to solve for the fault current at the protection installation, making it difficult to provide the theoretical basis for protection design.

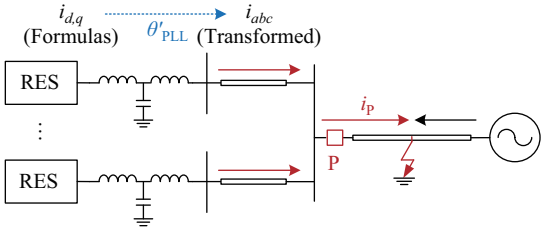

Fig. 9. Application of deduced RES fault current formulas for protection design.

Therefore, to achieve the final goal of RES fault analysis, i.e., establishing protection design, the above two restrictions should be solved in a future study. A possible solution is the fault calculation of the integral RES-grid system, taking both voltage transition and the unavailable RES output phase into consideration.

Actually, a branch of research has already identified this problem, making efforts on the fault calculation of a multi-RES system. The iterative method, proposed in [70], realized the fault steady state calculation of the multi-RES network. Further, [71] and [72] studied the sequential shutoff of each RES after fault occurrence, developing a more particle method to estimate fault characteristics of the multi-RES network. However, network calculation research regarding the fault sub-transient and transient stages remains absent, which is to provide the fault current peak values for protection design. In the writers' opinion, there are two main research difficulties in the future RES fault analysis:

- *Interaction influences the RES fault characteristics.* After disturbance of the fault, complicated interaction among RESs comes into play via the AC networks. Meanwhile, the dynamic of the DC side of RES also affects its output. Dissecting the interaction within the chaos system would be challenging.

- *High-order feature of the multi-RES system.* Due to the high order structure of the RES, the integrated RES-grid system can be much more complicated, for which the order-reduced analysis approach is needed. Necessary approximation tools and decoupling analysis approaches will help in the fault calculation of the integral system.

V. Conclusion

Fault characteristics analysis of RES is important for the forthcoming RES-dominating power system. In view of the cascaded structure and sequential activated control, the fault response of RES presents staged features, where different parts involved in RES contribute to its fault characteristics. On the basis of the review on fault analysis of the two commonly applied types of RESs, the staged fault characteristics of RES can be concluded as follows.

Sub-Transient Stage: RES control has not yet reacted in time for this brief moment because of the relatively low bandwidth. Therefore, RES fault characteristics are primarily determined by the hardware dynamics, i.e., the winding circuits and inverter filter;

Fault Transient Stage: LVRT control starts to take effect and the RES output starts to adjust toward the pre-determined reference value. For IIG, the most influential factors come from the PI controller and PLL; For DFIG, in addition to the armature reflection of the generator, the crowbar resistor and RSC controller have a vital impact on the output of DFIG under grid faults for different degrees;

Fault Steady Stage: RES output in the fault steady stage is predictable by the grid code and its own control reference value designed in FRT.

Although the research of RES fault analysis is almost inclusive, the deduced formulas cannot be directly used for protection design due to the simplified assumption of voltage drop and RES output phase. To determine the existing research problems, fault calculation of the integral RES-grid system is offered as the research prospect. The main difficulty is indicated as the solution of RESs interaction and order-reduced analysis approaches.

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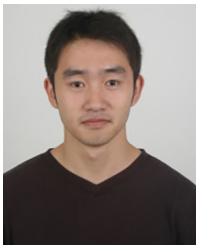

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