# Data Center Power System Stability – Part I: Power Supply Impedance Modeling

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***Abstract*—This two-part paper presents methods to predict, characterize and ensure the stability of data center power systems based on impedance analysis. The work was motivated by recent power system resonance incidents in new data centers. Part I presents new input impedance models for single-phase power supply units (PSUs) to enable this application. Existing impedance models of single-phase PSU cannot meet the requirements of this application because they exclude DC voltage control that affects system stability at low frequency, or are in a dq reference frame that cannot handle the complexity of data center power systems. The developed new models include DC bus dynamics and are directly in the phase domain to simplify system stability analysis, avoiding the need for multiple-input-multiple-output (MIMO) system models and the generalized Nyquist criterion that are difficult to apply but necessary with dq-frame models. Both the converter and system level models also include the coupled current response that is characteristic of AC-DC converters and important for system stability at low frequency. The simple form of the models and system stability analysis directly in the phase domain also make it possible to develop new PSU design methods and performance specifications that together will ensure the stability of new data center power systems. The developed models are validated by laboratory measurements and are used in Part II of the work to study data center power system stability.**

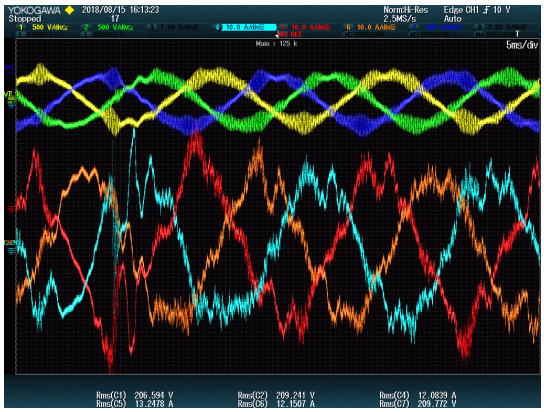
***Index Terms*—Data center power systems, frequency-domain methods, impedance modeling, system stability, system resonance.**

## I. Introduction

A large number of new data centers are being built to support the rapidly growing mobile communication, social media, cloud computing, internet of things (IoT), and other industries. A modern data center may consume over 100 MW electric power and uses an advanced power distribution system to ensure reliability and power quality [1]. With virtually every watt of electricity processed by power converters at least 2–3 times, data centers have a very high concentration of power electronics, surpassing that of large wind and PV farms and approaching that of high-voltage DC (HVDC) converter stations. As a result, data center power systems are also prone to the type of instability and resonance problems that have confronted the renewable energy and HVDC industry in recent years [2], [3].

In 2017, an almost identical resonance phenomenon was observed in multiple Meta data centers. Fig. 1(a) shows a set of representative current and voltage measurements recorded during such an event. An oscillation at 11 Hz is seen in the amplitude of both the current and voltage measured at the tap box to a server rack. Fourier analyses indicated strong harmonics at 49 Hz and 71 Hz in all three phase currents and voltages. In some other data centers, high frequency resonances in the 5–10 kHz range were also encountered, as illustrated in Fig. 1(b). This two-part paper describes part of the work to find the root cause and develop solutions to these problems.


(a)




(b)

Fig. 1. Measured resonances in data center power systems; (a) low-frequency resonance; (b) high-frequency resonance.

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Meta data centers are designed to use the Open Compute Project (OCP) architecture [1]. The electrical system employs 480/277 V or 208/120 AC distribution, with a 48 V DC battery backup unit (BBU) integrated with a server power supply. The 480/277 V AC is fed from the utility grid through a distribution network that starts from a substation and includes medium-voltage (13.2 kV) pad-mounted transformers (PTX), backup generators, and several layers of switchboards and protection panels. Each power supply unit (PSU) receives a single-phase AC input and produces a 12 V or 48 V DC output. A PSU employs an AC-DC converter with power factor correction (PFC) and an isolated DC-DC converter. AC UPSs are also used in some parts of the data center, but the majority of PSUs are supplied directly from the building power system. This direct distribution architecture, albeit much more reliable, resembles residential and commercial distribution systems. Therefore, resonances in these data centers are also indicative of stability challenges in future utility power systems when most loads become power electronics based.

Both the low- and high-frequency resonances shown in Fig. 1 happened in the power distribution system. The low-frequency resonance affected all PSUs supplied directly from the building power system and the resonance current could be measured all the way up to the substation transformer. The high-frequency resonance, on the other hand, was limited to the 480/277 network and only affected PSUs on certain parts of the data center. These problems are similar to instability and resonance problems in renewable energy generation systems, such as PV and wind farms. In particular, the low-frequency resonance phenomenon resembles those reported for type-III and type-IV turbines [3]–[5]. The high-frequency resonance is similar to resonances in HVDC transmission systems using modular multilevel converters (MMC) [6], [7].

### A. Impedance-Based Modeling and Analysis

Impedance modeling and analysis is an effective method to characterize electrical system resonance. The method has drawn much attention in recent years because of growing stability challenges in renewable energy and HVDC systems [8]. However, to apply the method to data center power systems, new developments are required in two areas:

#### 1) Server Power Supply Modeling

Server PSUs represent the most significant and important loads in a data center and contribute directly to the system resonance. An input impedance model is required for each PSU in order to build a system impedance model for stability analysis. An input impedance model was presented in [9] for single-phase PFC converters and used in [10] to study the interactions with input EMI filters. The model was developed by treating the PFC output as an ideal DC voltage source, which is valid above the second harmonic frequency where the DC bus capacitor impedance is negligible. Below the second harmonic frequency, this model predicts a purely resistive impedance, which would not form any resonance with a passive distribution network, hence cannot be used to study the low-frequency resonance shown in Fig. 1(a). The PSU model becomes nonlinear when DC voltage dynamics are included and a much more elaborated process is required to model the input impedance. Ref. [11] outlined such a method and provided numerical results, but no analytical models were developed.

#### 2) Power System Modeling

Most recent works on converter-grid system stability are concerned with large-scale renewable generation and HVDC transmission. Converters used in these systems are all three phase (without neutral) and the network they connect to is highly symmetrical. This allows system stability to be studied based on positive- and negative-sequence impedances. To apply the method to a wind or PV farm, the output impedances of individual wind turbines and PV inverters are combined with the farm network impedance to form an aggregated farm-level impedance model and used against the grid impedance to determine system stability [12]. These three-phase system modeling and aggregation methods cannot be applied directly to data centers:

- Because individual converters (PSUs) in data centers use single-phase inputs, system modeling has to bridge between single-phase load models and three-phase source (data center distribution network) models. The system model also has to consider possible zero-sequence instability that does not exist in power systems without neutral connection.
- Unlike wind and PV farms that are usually located at remote areas and integrated to the grid by long lines, data centers are sited for strong grid connection and the grid impedance is insignificant compared to the distribution system impedance in the data center. Aggregating the data center into a single impedance and using it against the grid impedance to determine system stability will miss the problem and hide its root cause.

### B. Related Prior Work

Another application in which single-phase AC-DC converters have been found to cause instability is electric railway traction systems. Swiss Federal Railways (SBB) experienced high-frequency resonance and instability problems first in the then-new converter-based locomotive Re 450/460 in the 1990s and conducted a series of studies to characterize and solve the problems based on impedance modeling and analysis [13]. The developed solutions include the requirement for the converter input admittance to be "passive" above certain frequency depending on the length of the network [14].

Low-frequency resonance in electric railway systems was first reported in 2006 [15]. The subject drew renewed interests in recent years [16]–[20]. It was recognized that stability analysis in the low-frequency range has to include the effects of the phase-lock loop (PLL) and DC output voltage control of the single-phase AC-DC front-end converter. Ref. [16] presented the development of such admittance models in a dq reference frame. Refs. [17], [18] expanded this method and examined the relationship and characteristics of different elements in the dq-frame impedance matrices.

Impedance modeling of converters operating with AC input or output faces a fundamental challenge, in that the converter models cannot be linearized by conventional small-signal

method because of the presence of variables that change at the fundamental frequency. Impedance modeling in the dq reference frame is one method to overcome this difficulty but has several disadvantages [21], most noticeably:

- Inseparable dynamic coupling between d- and q-axis, which requires the generalized Nyquist criterion for system stability analysis;
- Difficulties to measure impedance in a rotating dq reference frame and to interconnect the models of different converters each developed in its own dq reference frame.

Single-phase power system modeling and analysis in the dq reference frame inherits these general disadvantages but also suffers from some additional problems. To allow the use of dq transformation, a fictitious second phase has to be added, which artificially doubles the order of the model. This, combined with the coupling between the resulting d- and q-axis dynamics, significantly complicates the converter model and system stability analysis. Additionally, power flow from AC to DC at the second harmonic frequency and the resulting second-harmonic voltage on the DC bus, which are inherent in single-phase AC-DC converters, must be ignored in order for the transformed dq-frame model to be time-invariant such that it can be linearized. The method has some merits for railway systems considering the use of PLL and dq-frame current control of the converters [16], [17] and the simple system. It is too complicated for data center power systems, which may use 100,000 or more single-phase PSUs powered through a complex radial distribution network of three phases in Y or $\Delta$ configuration.

Impedance-based stability modeling and analysis of AC power systems directly in the phase domain [21] does not have the limitations of dq-frame methods but requires different methods to model converter impedance. For electric railway system stability analysis [19], [20], presented the measurement and modeling of converter and network impedance in the phase domain. The analytical modeling method presented in [20] followed the general principle of harmonic linearization [21] and included the coupled current response. The derivation involves manipulation of a number of algebraic equations, leading to lengthy models at the end that are difficult to interpret and use. The coupled current response was also considered in the measurement of converter impedances in [20]. On the other hand, the system models proposed in [19], [20] were still in a matrix form by treating the coupled current as an independent dynamic variable. This requires again the use of the generalized Nyquist criterion and has similar limitations as the dq-frame method. Treating a coupled current response as an independent dynamic variable also has a more fundamental problem that will be discussed in Subsection III.C.

### *C. Objective and Approach of This Work*

The objective of this work is to develop practical solutions to data center power system stability problems. This includes not only determining the stability of a system, for which there are a number of options, including time-domain simulation, but also identifying common modes of instability, understanding their root causes, and developing mitigation methods. The final goal is to establish new data center design guidelines and power supply performance specifications that will ensure power system stability. To that end, the modeling method should be scalable such that it can handle the complexity of practical data center power systems, and the stability condition should have a simple and direct relationship to key design parameters, such that it can be used to design a system, not just to assess the stability of systems that have already been designed.

Our overall approach is based on impedance modeling and analysis in the phase domain. The generalized Nyquist criterion is a valid method to determine stability when all parameters of a system are given. However, since the criterion applies to eigenvalues or the determinant of the system matrix, it usually can only be applied in a numerical form, which is difficult to develop insights from and to use as a design tool. Considering that, we will limit the system model to single-input-single-output (SISO) such that the original Nyquist criterion can be used. New modeling methods have been developed at both the converter and the system level to meet these requirements. The main contributions of the work include:

- New impedance models are developed for single-phase power supplies directly in the phase domain. The models include DC bus dynamics such that they can be used to study new low-frequency stability problems in data centers.
- The new models are developed by first characterizing the converter with independent perturbations at the AC and DC terminal. The intermediate transfer functions have clear physical meaning and are useful in their own right. The final models have an intuitive structure and are easy to use.
- The coupled current responses are automatically included in the modeling process. Their effects on PSU-source system stability are accounted for in a new system model in SISO form to avoid the complexity and disadvantages of the generalized Nyquist criterion.
- Based on the analytical PSU models and simple SISO system model, the relationship between each of the resonance problems described at the beginning of this section and characteristics of the source and PSU controls is identified. The general understanding and insights gained from these analyses provide a basis for the development of practical and systematic solutions.
- A systematic method is developed to model a three-phase data center power system in SISO form. Part II of the paper covers this topic and also presents the development of new product specs that can ensure system stability.

An early version of the work was presented at IEEE ECCE 2019 in two separate papers [23], [24]. They are joined together here because the topics are closely related and are integral parts of methods required for addressing a practical challenge, but kept in two parts because each deals with a distinctive aspect of the system. In addition to data center power system stability studies, the impedance models and SISO system stability analysis can be expanded to include PLL and dq-frame current control, and used to simplify the analysis of railway power systems. The three-phase system modeling

and stability analysis methods presented in Part II are also applicable to microgrids and other types of distribution systems with single-phase and unbalanced sources and loads. The impedance-based design guidelines and product performance specifications also have reference value for other industries.

The rest of Part I is organized as follows: Section II reviews PFC converter circuit and control that will be modeled in this work. A unified circuit model representing both boost and boost-derived PFC converters is defined along with a typical control system. The effects of DC bus dynamics are discussed to explain the limitations of the existing model and the principle of the new modeling method. Section III uses this method to develop different transfer function models that capture the complete small-signal behavior of the converter, including coupling effects caused by the nonlinearity related to DC bus. Section IV uses the developed models to study the stability of a simple system comprising one PFC converter and a single-phase source to explain the mechanism and root cause for low-frequency resonances. Section V explains the effects of control and PWM delays on PFC converter input impedance, presents a method to incorporate these delays in the impedance model, and uses the model to characterize high-frequency resonances. Section VI presents measurement results to validate the proposed models and discusses possible solutions to both types of resonance problems illustrated in Fig. 1. Section VII concludes the work.

## II. PFC Converter and Input Impedance Modeling

Power supplies used in data centers mostly use a two-stage design comprising a single-phase PFC front-end converter and an isolated DC-DC converter [26]. Three such power supplies are used together and connected in a star ($Y$) or delta ($\Delta$) configuration. Refer to [24] and Part II of this work [25] for a more detailed description of power system architectures in modern data centers.

### A. PFC Converter Circuit and Control

The PFC front-end may use a boost or dual-boost converter [26], as illustrated in Fig. 2. To avoid the need to model each circuit separately, we will first present a unified mathematic model to represent both converters. Using the variables defined in Fig. 2(a), we obtain the following switching-cycle averaged model for the boost inductor current in the boost PFC converter, where $d$ is the duty ratio of the switch:

$$v_{\rm a} > 0 : L\frac{{\rm d}i_{\rm L}}{{\rm d}t} = v_{\rm a} - (1-d)v_{\rm DC} \tag{1}$$

$$v_{\rm a} < 0 : L\frac{{\rm d}i_{\rm L}}{{\rm d}t} = -v_{\rm a} - (1-d)v_{\rm DC} \tag{2}$$

For the dual-boost PFC converter, the inductor current model is slightly different:

$$v_{\rm a} > 0 : L\frac{{\rm d}i_{\rm L}}{{\rm d}t} = v_{\rm a} - (1-d)v_{\rm DC} \tag{3}$$

$$v_{\rm a} < 0 : L\frac{{\rm d}i_{\rm L}}{{\rm d}t} = v_{\rm a} + (1-d)v_{\rm DC} \tag{4}$$

To develop a unified model for both converters that is valid over an entire line cycle, we define

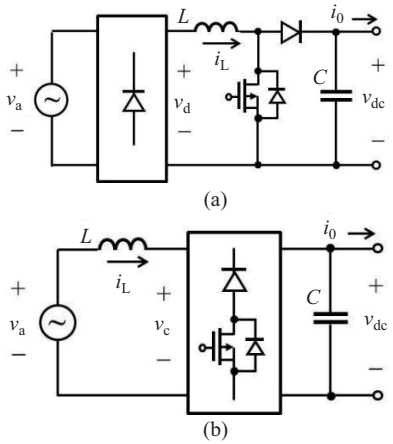


Fig. 2. Two different power stage topologies for the PFC front-end converter; (a) boost; (b) dual boost.

- $i_{\rm a} = {\rm sign}(v_{\rm a})i_{\rm L}$ and $d' = {\rm sign}(v_{\rm a})(1-d)$ for the boost PFC converter; and
- $i_{\rm a} = i_{\rm L}$ and $d' = {\rm sign}(v_{\rm a})(1-d)$ for the dual-boost converter.

Based on these definitions, (1)–(4) can be written in a unified form as follows to represent both circuits:

$$L\frac{{\rm d}i_{\rm a}}{{\rm d}t} = v_{\rm a} - d'v_{\rm DC} \tag{5}$$

An underlying assumption made in (1)–(5) is that the converter operates in the continuous conduction mode (CCM). The actual inductor current in a boost or dual-boost PFC converter becomes discontinuous near each zero-crossing point of the input voltage, which leads to a different averaged model. In the following, we assume that the discontinuous conduction mode (DCM) interval is short compared to a line cycle and can be ignored in small-signal modeling.

A PFC converter is usually equipped with two control loops: an inner current loop that regulates the input current, $i_{\rm L}$, and an outer voltage loop that controls the DC output voltage, $v_{\rm DC}$. A principle control diagram showing these two control functions is given in Fig. 3. Input impedance models developed in the rest of the paper will be based on this design. Consistent with the unified converter circuit model (5), it is assumed here that the AC input current ($i_{\rm a}$) is directly controlled. This requires the current controller and pulse-width modulator to be designed for bipolar (AC) operation, which may be different from actual control implementation. Functionally, however, they are equivalent as far as small-signal modeling is concerned. Note also that the PWM output is assumed to define the off-time duty ratio $d' = 1-d$.

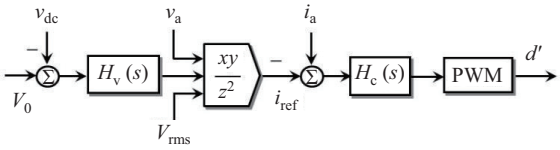


Fig. 3. Principle control diagram of a single-phase PFC converter.

### *B. Existing PFC Impedance Model*

Note that the inductor current model (5) is nonlinear in general because it includes a bilinear term between the control ($d'$) and the state (DC output voltage). Similar nonlinearity exists in the DC output voltage model (7) given in the next subsection. The PFC input impedance model presented in [9] avoided this difficulty by treating the DC bus as an ideal voltage source, denoted as $V_{\rm DC}$ hereafter. Under this assumption, the voltage compensator output is also constant and the reference current $i_{\rm ref}$ is proportional to the input voltage by a constant gain, $i_{\rm ref} = Gv_{\rm a}$. This renders the converter model linear and allows it to be represented by the simple block diagram given in Fig. 4. Note that the gain of the PWM block is assumed unity, such that the output of the current compensator can be equated with the duty ratio signal $d'$. Based on Fig. 4, the input impedance is found to be:

$$Z_{\rm am}(s) = \frac{v_{\rm a}(s)}{i_{\rm a}(s)} = \frac{sL + V_{\rm DC}H_{\rm c}(s)}{1 + GV_{\rm DC}H_{\rm c}(s)} \tag{6}$$

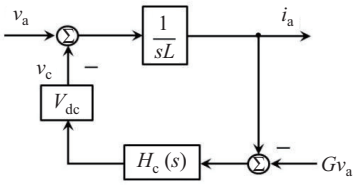


Fig. 4. Block diagram for development of impedance model (6).

This model was used in [10] to study PFC converter interactions with the input filter. At frequencies close to or below the fundamental, (6) predicts a purely resistive impedance, which cannot explain the low-frequency resonance shown in Fig. 1(a). The model also assumed analog control implementation. When digital control is used, the input impedance can be greatly affected by control and PWM delay at high frequencies, which (6) does not consider. For the purpose of this work, we divide the overall frequency range of interest for system stability analysis into three:

- *Low frequency*: From DC to about the second harmonic frequency ($2f_1$). The system resonance shown in Fig. 1(a) falls in this frequency range.
- *Medium frequency*: From the second harmonic frequency to half the current loop crossover frequency. Input impedance of the converter is dominated by current control in this frequency range and effects of control are insignificant.
- *High frequency*: Above the medium frequency range where control delay is the only factor left from different control functions. The system resonance shown in Fig. 1(b) falls in this frequency range.

Consistent with these definitions, the input impedance defined by (6) will be referred to as the medium-frequency model hereafter, as indicated by the letter $m$ in the subscript. Note that the boundary between medium and high frequency range is not a clear-cut and may vary with converter design. For power supplies and other low-power converters, it is usually in the range of 1–2 kHz. For high power converters such as wind and PV inverters, for example, the low switching frequency limits the current loop bandwidth to $\sim$ 200 Hz. In those cases, the medium frequency range may not be distinguishable from the other two.

### *C. DC Bus Dynamics and Coupling over Frequency*

The medium-frequency model (6) loses its accuracy at low frequency because it ignores DC bus dynamics and DC voltage control. To explain the effects of the DC bus and the method we apply to model it, refer to the overall converter circuit diagram depicted in Fig. 5. Ignoring power losses inside the converter, we can model dynamics of the DC bus by

$$C\frac{{\rm d}v_{\rm DC}}{{\rm d}t} = d'i_{\rm a} - i_0 \tag{7}$$

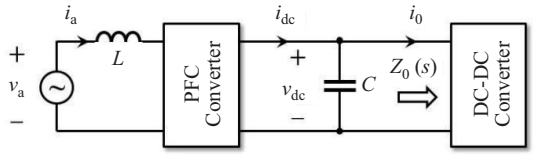


Fig. 5. Definition of variables for low-frequency impedance models.

Assume the converter is operating in a steady state and a perturbation at (an angular) frequency $\omega_{\rm p}$ is added to the input voltage. The input current responds to this voltage perturbation with a component at the same frequency. This current, when multiplied with the fundamental of the duty ratio through the first term on the right-hand side of (7), causes a perturbation in $v_{\rm DC}$ at frequency $\omega_{\rm p} + \omega_1$ as well as $\omega_{\rm p} - \omega_1$.

Turn now to the input current model (5), specifically, the bilinear term $d'v_{\rm DC}$ on the right-hand side. For each small-signal component in $v_{\rm DC}$ at frequency $\omega_{\rm v}$, its multiplication by the fundamental component of the duty ratio in the term identified above will produce a voltage at the terminal of the converter at $\omega_{\rm v} + \omega_1$ as well as $\omega_{\rm v} - \omega_1$. Each of these two voltage components will in turn drive a current through the inductor at the same frequency. Substituting $\omega_{\rm v}$ by $\omega_{\rm p} \pm \omega_1$, we see that small-signal response of the input current includes three new components:

$$(\omega_{\rm p} \pm \omega_1) \pm \omega_1 = \{\omega_{\rm p} - 2\omega_1,\ \ \omega_{\rm p},\ \ \omega_{\rm p} + 2\omega_1\} \tag{8}$$

The new component at $\omega_{\rm p}$ is in addition to the current response that the medium-frequency model (6) predicts and has the effect to lower the input impedance of the converter, hence needs to be included in system stability analysis.

The other two current components at $\omega_{\rm p} \pm 2\omega_1$ indicated in (9) will be referred to as *coupled currents* and the phenomenon is termed *coupling over frequency*. A similar behavior exists in three-phase converters but only one of the two components exists depending on the sequence of voltage perturbation [22]. The effects of the coupled currents on converter-grid system stability have drawn much attention in recent years and are included in the system models presented in [19], [20] by using a $2 \times 2$ matrix model. Section III.D will present a new method to include the effects of the coupled current while keeping the system model in the SISO form to avoid the need for the

generalized Nyquist criterion. To support this application, we will model each of the three currents by a transfer function.

For convenience, the perturbation frequency in the following development will be denoted by a complex variable $s = j\omega_{\rm p}$. To distinguish from the overall response of the current and voltage, we will denote a small-signal component by a "hat" above the corresponding variable and give its frequency inside a pair of parentheses next to it. For example, $\hat{i}_{\rm a}(s-j2\omega_1)$ is the input current small-signal response at frequency $s - j2\omega_1$ to a small-signal perturbation in the input voltage at frequency $s$. With these notations, the transfer functions that we will develop to model the three current components identified in (8) are defined as follows:

$$Y_{\rm a}(s) = \frac{\hat{i}_{\rm a}(s)}{\hat{v}_{\rm a}(s)} \tag{9}$$

$$Y_{c-2}(s) = \frac{\hat{i}_{\rm a}(s - j2\omega_1)}{\hat{v}_{\rm a}(s)} \tag{10}$$

$$Y_{c+2}(s) = \frac{\hat{i}_{\rm a}(s + j2\omega_1)}{\hat{v}_{\rm a}(s)} \tag{11}$$

where $Y_{\rm a}(s)$ is the PFC converter input admittance that one can measure when the converter operates with an ideal AC source. $Y_{c-2}(s)$ and $Y_{c+2}(s)$ will be referred to as transfer admittance [22]. The chain of reaction alluded to before is in fact endless, such that a voltage perturbation at $\omega_{\rm p}$ will lead to current responses at $\omega_{\rm p} \pm 2k\omega_1, k = 0, 1, 2, \ldots, \infty$. (This is a special property of single-phase converters and does not affect three-phase converters [22]). However, mathematically it suffices to model the current at $\omega_{\rm p} \pm 2\omega_1$ only, for two reasons:

- Current responses at $\omega_{\rm p} \pm 2k\omega_1$ with $k > 1$ can be obtained by cascading the transfer functions from the perturbation voltage at $\omega_{\rm p}$ to currents at $\omega_{\rm p} \pm 2\omega_1$.
- Current responses at $\omega_{\rm p} \pm 2k\omega_1$ with $k > 1$ will not cause appreciable response in the DC bus voltage due to the low impedance of the DC bus at high frequency.

## III. Model Development

The three admittances defined in (9)–(11) will be developed in this section. Each is rather complex transfer function as it depends on the full converter circuit model (5) and (7), both voltage and current control, as well as dynamics of the downstream DC-DC converter. Directly modeling the converter as a whole will lead to lengthy mathematical expressions that show no structure and are difficult to comprehend. To reduce the complexity and gain insights, we will apply the three-step method developed in [22] for three-phase converters:

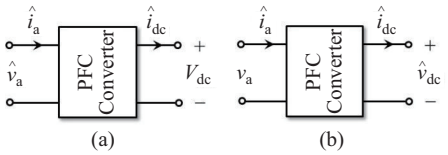


Fig. 6. Modeling by separate perturbation at AC and DC terminals.

1) Apply a perturbation to the AC input voltage while holding the DC bus voltage constant, and calculate the response of $i_{\rm a}$ and $i_{\rm dc}$ at different frequencies, see Fig. 6(a).
2) Apply a perturbation to the DC bus voltage while keeping the AC input voltage fixed, and calculate the resulting response of $i_{\rm a}$ and $i_{\rm dc}$ at different frequencies, see Fig. 6(b).
3) Build a complete small-signal model of the converter by connecting the transfer functions developed in the first two steps and use it to develop admittances (9)–(11).

### A. Modeling with an AC Voltage Perturbation

The DC bus in this case is replaced by a constant DC voltage. The setup is the same as that assumed for the development of (6). To capture the full dynamics, especially the coupling between the AC and DC side of the converter, four other transfer functions are modeled in addition to the input (impedance) admittance. They are defined below where $s$ is the frequency of the AC voltage perturbation:

- $Y_{\rm aa}(s)$: Transfer function from AC voltage perturbation to AC input current at the same frequency.
- $Y_{a0+}(s)$: Transfer function from AC voltage perturbation to DC output current at $s + j\omega_1 \triangleq s_{+1}$
- $Y_{a0-}(s)$: Transfer function from AC voltage perturbation to DC output current at $s - j\omega_1 \triangleq s_{-1}$
- $Y_{a+2}(s)$: Transfer function from AC voltage perturbation to AC input current at $s + j2\omega_1 \triangleq s_{+2}$
- $Y_{a-2}(s)$: Transfer function from AC voltage perturbation to AC input current at $s - j2\omega_1 \triangleq s_{-2}$

Keeping the DC bus voltage constant renders the converter model linear, such that the block diagram in Fig. 4 can be used to represent the converter. As part of the steady state, the DC bus voltage is assumed to contain a DC as well as a second harmonic, which is characteristic of single-phase PFC converters but ignored in the dq-frame models [16], [17].

Based on these considerations, the five transfer functions defined above are found as follows:

$$Y_{\rm aa}(s) = \frac{1 + V_{\rm DC}G_1(s)H_{\rm c}(s)}{sL + V_{\rm DC}H_{\rm c}(s)} \tag{12}$$

$$Y_{a0+}(s) = \frac{\boldsymbol{D}_1}{2}Y_{\rm aa}(s) + \frac{\boldsymbol{I}_1}{2}\left[Y_{\rm aa}(s) - G_1(s)\right]H_{\rm c}(s) \tag{13}$$

$$Y_{a0-}(s) = \frac{\boldsymbol{D}_1^*}{2}Y_{\rm aa}(s) + \frac{\boldsymbol{I}_1^*}{2}\left[Y_{\rm aa}(s) - G_1(s)\right]H_{\rm c}(s) \tag{14}$$

$$Y_{a+2}(s) = \frac{\boldsymbol{G}_{02}}{2}\frac{V_{\rm DC}H_{\rm c}(s_{+2}) + \left[Y_{\rm aa}(s) - G_1(s)\right]H_{\rm c}(s)}{s_{+2}L + V_{\rm DC}H_{\rm c}(s_{+2})} \tag{15}$$

$$Y_{a-2}(s) = \frac{\boldsymbol{G}_{02}^*}{2}\frac{V_{\rm DC}H_{\rm c}(s_{-2}) + \left[Y_{\rm aa}(s) - G_1(s)\right]H_{\rm c}(s)}{s_{-2}L + V_{\rm DC}H_{\rm c}(s_{-2})} \tag{16}$$

The asterisk in (14) and (16) indicates complex conjugate. New variables that appear in (12)–(16) that have not been used are defined in the following:

- $\boldsymbol{V}_1$, $\boldsymbol{I}_1$ and $\boldsymbol{D}_1$ each is a complex number representing the amplitude and phase of the fundamental component of the input voltage, input current and the duty ratio signal, respectively. They define the steady-state operation condition for which the small-signal models are developed.

- Transfer function $G_1(s) = GH_{\rm a}(s)$, $H_{\rm a}(s)$ being the small-signal response of the multiplier, including the circuit that is used to extract the input RMS voltage. This function replaces the constant $G$ in Fig. 4.
- $\boldsymbol{G}_{02}$ is defined by (17) where $\boldsymbol{V}_{02}$ is a complex number representing the amplitude and phase of the second harmonic voltage at the DC output. Note that both $Y_{a+2}(s)$ and $Y_{a-2}(s)$ reduce to zero if $\boldsymbol{V}_{02}$ can be ignored.

$$\boldsymbol{G}_{02} = -\boldsymbol{V}_{02} H_{\rm v}(j2\omega_1) \tag{17}$$

### *B. Modeling with a DC Voltage Perturbation*

In this case, a perturbation $\hat{v}_{\rm DC}$ is introduced at the DC terminal. DC bus capacitor and the DC-DC converter are excluded in the model, but DC bus voltage control is considered. Similar to the previous case, the converter is modeled by five transfer functions in this case:

- $Y_{0a+}(s)$: Transfer function from DC voltage perturbation to AC input current at $s + j\omega_1$
- $Y_{0a-}(s)$: Transfer function from DC voltage perturbation to AC input current at $s - j\omega_1$
- $Y_{00}(s)$: Transfer function from DC voltage perturbation to DC output current at the same frequency
- $Y_{0+2}(s)$: Transfer function from DC voltage perturbation to DC output current at $s + j2\omega_1$
- $Y_{0-2}(s)$: Transfer function from DC voltage perturbation to DC output current at $s - j2\omega_1$

A DC voltage perturbation affects the input current response in two ways. First, its multiplication with the fundamental of the duty ratio creates a response in the converter terminal voltage ($d' v_{\rm DC}$) at $s+j\omega_1$ as well as $s-j\omega_1$. Each of these voltage components will drive a corresponding component in the input current response. Second, the DC voltage perturbation causes a response in the voltage compensator output at $s$, which, when multiplied with the input voltage, also creates a response in the reference current ($i_{\rm ref}$) at $s + j\omega_1$ and $s - j\omega_1$.

To model the DC output current response, recall from II. C and Fig. 5 that $i_{\rm DC} = d' i_{\rm a}$. Based on this, a small-signal component of the duty ratio (or the input current) at $\omega$ interacts with the fundamental of the input current (or the duty ratio) will produce a DC current response at $\omega \pm \omega_1$. Therefore, once small-signal responses of the duty ratio and the input current are found, they can be used to determine the response of the DC current at each of the frequencies defined above. The resulting models are summarized below:

$$Y_{0a+}(s) = -\frac{1}{2} \cdot \frac{\boldsymbol{D}_1 + \boldsymbol{V}_1 V_{\rm DC} H_{\rm c}(s + j\omega_1) H_{\rm v}(s)}{(s + j\omega_1)L + V_{\rm DC} H_{\rm c}(s + j\omega_1)} \tag{18}$$

$$Y_{0a-}(s) = -\frac{1}{2} \cdot \frac{\boldsymbol{D}_1^* + \boldsymbol{V}_1^* V_{\rm DC} H_{\rm c}(s - j\omega_1) H_{\rm v}(s)}{(s - j\omega_1)L + V_{\rm DC} H_{\rm c}(s - j\omega_1)} \tag{19}$$

$$\begin{aligned} Y_{00}(s) = {} & \frac{\boldsymbol{D}_1^*}{2} Y_{0a+}(s) + \frac{\boldsymbol{I}_1^*}{2} H_{\rm c}(s_{+1}) \left[ Y_{0a+}(s) + \frac{\boldsymbol{V}_1}{2} H_{\rm v}(s) \right] \\ & + \frac{\boldsymbol{D}_1}{2} Y_{0a-}(s) \\ & + \frac{\boldsymbol{I}_1}{2} H_{\rm c}(s_{-1}) \left[ Y_{0a-}(s) + \frac{\boldsymbol{V}_1^*}{2} H_{\rm v}(s) \right] \end{aligned} \tag{20}$$

$$Y_{0+2}(s) = \frac{\boldsymbol{D}_1}{2} Y_{0a+}(s) + \frac{\boldsymbol{I}_1}{2} H_{\rm c}(s_{+1}) \left[ Y_{0a+}(s) + \frac{\boldsymbol{V}_1}{2} H_{\rm v}(s) \right] \tag{21}$$

$$\begin{aligned} Y_{0-2}(s) = {} & \frac{\boldsymbol{D}_1^*}{2} Y_{0a-}(s) \\ & + \frac{\boldsymbol{I}_1^*}{2} H_{\rm c}(s_{-1}) \left[ Y_{0a-}(s) + \frac{\boldsymbol{V}_1^*}{2} H_{\rm v}(s) \right] \end{aligned} \tag{22}$$

Most transfer functions developed above cannot be directly measured in a laboratory setup because of the imperfectness of practical AC and DC sources. To verify their mathematical correctness, detailed circuit simulation was performed and frequency responses corresponding to each transfer function were scanned numerically over frequency. The predictions by each transfer function match simulation results as expected. Because of that, no comparison is included in the paper. Since (12)–(16) and (18)–(22) are developed from (5) and (7) that are widely used and small-signal linearization is the only additional step that is applied, validation by numerical simulation is deemed appropriate and sufficient. Section VI reports lab measurements to validate the predicted behavior at the converter and system level.

### *C. Overall Small-Signal Models*

Transfer functions (12)–(16) and (18)–(22) were developed in two separate steps using independently injected voltage perturbations. In actuality, the DC bus is internal to the PFC converter and its voltage perturbation will not be externally applied but rather induced when the AC input voltage is perturbed. Based on this, the block diagram in Fig. 7 can be used to represent the overall response to a perturbation in the input voltage. Impedance $Z_{\rm DC}$ represents the impedance of the DC bus between the PFC converter and the DC-DC converter. It includes the DC filter capacitor as well as the input admittance $Y_{l0}(s)$ of the DC-DC converter, as defined below:

$$Z_{\rm DC}(s) = \frac{1}{sC_{\rm DC} + Y_{l0}(s)} \triangleq \frac{1}{Y_{\rm DC}(s)} \tag{23}$$

The diagram starts from the voltage perturbation $\hat{v}_{\rm a}(s)$ on the left and gives the responses of the three currents defined in (9)–(11), as highlighted in Fig. 7. Two important intermediate variables are the induced DC voltage perturbation $\hat{v}_{\rm DC}(s - j\omega_1)$ and $\hat{v}_{\rm DC}(s + j\omega_1)$, indicated by the two thick lines in the middle. Response of these voltages are defined by the following transfer functions:

$$G_{v0-}(s) \triangleq \frac{\hat{v}_{\rm DC}(s - j\omega_1)}{\hat{v}_{\rm a}(s)}, G_{v0+}(s) \triangleq \frac{\hat{v}_{\rm DC}(s + j\omega_1)}{\hat{v}_{\rm a}(s)} \tag{24}$$

To explain the diagram, consider its upper portion and recall the definition of each of the transfer functions given in the last two subsections. Through $Y_{a0-}(s)$, input voltage perturbation $\hat{v}_{\rm a}(s)$ produces a DC current response at $s - j\omega_1$. This current multiplied by the DC bus impedance $Z_{\rm DC}$ creates a voltage response $\hat{v}_{\rm DC}(s - j\omega_1)$ in the DC bus. As soon as this voltage is induced, it drives a current at the same frequency back into the DC port of the converter through the DC-port admittance $Y_{00}(s - j\omega_1)$. The voltage also produces three other currents:

- Current $\hat{i}_{\rm a}(s)$ at the AC port through $Y_{0a+}(s - j\omega_1)$

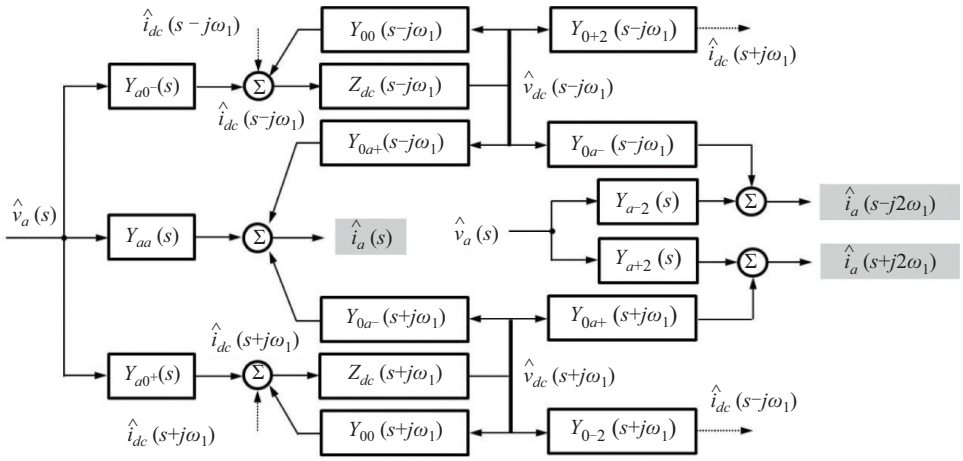


Fig. 7. A block diagram connecting different transfer functions to define the complete small-signal response of a single-phase PFC converter to a perturbation in the input voltage.

- Current $\hat{i}_{\rm a}(s-j2\omega_1)$ at the AC port through $Y_{0a-}(s-j\omega_1)$
- Current $\hat{i}_{\rm DC}(s+j\omega_1)$ at the DC port through $Y_{0+2}(s-j\omega_1)$, which is added to $\hat{i}_{\rm DC}(s+j\omega_1)$ on the lower portion of the diagram by the dashed arrow.

To define the three current responses of interest, the first step is to solve for the response of $\hat{v}_{\rm DC}(s-j\omega_1)$ and $\hat{v}_{\rm DC}(s+j\omega_1)$. Based on the diagram, transfer functions $G_{v0-}(s)$ and $G_{v0+}(s)$ that define these two voltages can be determined. The full model is rather lengthy but can be significantly simplified if we ignore the two relatively weak connections represented by the dashed arrows:

$$G_{v0-}(s) \approx \frac{Y_{a0-}(s)}{Y_{\rm DC}(s-j\omega_1) - Y_{00}(s-j\omega_1)} \tag{25}$$

$$G_{v0+}(s) \approx \frac{Y_{a0+}(s)}{Y_{\rm DC}(s+j\omega_1) - Y_{00}(s+j\omega_1)} \tag{26}$$

Based on the block diagram, the transfer functions defining these currents are found to be:

$$\begin{aligned} Y_{\rm a}(s) = {} & Y_{\rm aa}(s) + Y_{0a+}(s-j\omega_1)G_{v0-}(s) \\ & + Y_{0a-}(s+j\omega_1)G_{v0+}(s) \end{aligned} \tag{27}$$

$$Y_{c-2}(s) = Y_{a-2}(s) + Y_{0a-}(s-j\omega_1)G_{v0-}(s) \tag{28}$$

$$Y_{c+2}(s) = Y_{a+2}(s) + Y_{0a+}(s+j\omega_1)G_{v0+}(s) \tag{29}$$

### *D. Coupled Currents as Independent Dynamic Variables*

The coupled current responses defined by (28)–(29) were considered also in impedance modeling and measurement of locomotive front-end converters in [19], [20]. To include the effects of these currents, a system model in the matrix form was used in [19], [20]. The method is essentially to represent the converter by a $2 \times 2$ admittance matrix as follows:

$$\boldsymbol{Y}(s) = \begin{bmatrix} Y_{\rm a}(s) & Y_{c+2}(s-j2\omega_1) \\ Y_{c-2}(s) & Y_{\rm a}(s-j2\omega_1) \end{bmatrix}$$

This admittance matrix is multiplied with the source impedance matrix to define a MIMO system model. In this formulation, stability analysis requires the generalized Nyquist criterion, which is one of the disadvantages discussed in the Introduction. Here we point out a more fundamental problem with treating the coupled current as an independent dynamic variable.

Recall the definition of $\{\boldsymbol{V}_1, \boldsymbol{I}_1, \boldsymbol{D}_1, \boldsymbol{V}_{02}\}$ in Subsection III.A. Each is a complex number. For convenience, we write each in an exponential form:

$$\boldsymbol{V}_1 = V_1 e^{j\varphi_{v1}} \qquad \boldsymbol{I}_1 = I_1 e^{j\varphi_{i1}}$$
$$\boldsymbol{D}_1 = D_1 e^{j\varphi_{d1}} \qquad \boldsymbol{V}_{02} = V_{02} e^{j\varphi_{02}}$$

Note that the voltage phase angle $\varphi_{v1}$ depends on the starting point of measurement (or perturbation) and can be arbitrary. Other angles depend on both $\varphi_{v1}$ and operation conditions. For example, $\varphi_{i1} = \varphi_{v1}$ if the converter operates with unity power factor. Recall also that these phase angles have the effect to offset the phase response of transfer functions (13)–(16), (18)–(19) and (21)–(22) but not $Y_{\rm aa}(s)$ and $Y_{00}(s)$.

Assume that the starting point of measured is shifted over time, which causes the voltage phase angle to change and become $\varphi_{v1} + \Delta\varphi$. Accordingly, both $\varphi_{i1}$ and $\varphi_{d1}$ are offset by $\Delta\varphi$, and $\varphi_{02}$ changes to $\varphi_{02} + 2\Delta\varphi$. (The relationship between $\varphi_{02}$ and $\varphi_{v1}$ can be determined from steady-state operation of the converter.)

To see how the angle shift affects the "compound" models (27)–(29), note first that the angle of $G_{v0-}(s)$ and $G_{v0+}(s)$ is shifted by $-\Delta\varphi$ and $\Delta\varphi$, respectively. This is obvious from (25)–(26). Based on this and the observations made above, we can conclude that:

- The phase response of $Y_{\rm a}(s)$ is unaffected by $\Delta\varphi$
- The phase response of $Y_{c-2}(s)$ is changed by $-2\Delta\varphi$
- The phase response of $Y_{c+2}(s)$ is changed by $2\Delta\varphi$

Since the angle shift is merely a change in how the converter is measured or modeled, it should have no effects on the operation and characteristics of the converter. The invariance of $Y_{\rm a}(s)$ phase response reflects this. On the other hand, the dependency of $Y_{c-2}(s)$ and $Y_{c+2}(s)$ on $\Delta\varphi$ indicates that the relationship they describe is time-variant. It also indicates that a coupled current does not qualify as an independent dynamic variable in small-signal analysis. Therefore, it is mathematically inappropriate to treat (28)–(29) as regular transfer functions in stability analysis. The same conclusion

applies to three-phase converters. The system model presented in the next section avoids this problem while retaining the desired SISO form.

## IV. PSU-Source Modeling and Stability

Application of the developed PSU models in data center power system stability analysis has to consider the three-phase configuration of multiple PSUs as well as the complex distribution system architecture. This subject is treated in Part II of the work [26]. In this section, we consider an elemental system in which one PSU is powered from a single-phase AC power source directly, as illustrated in Fig. 8a), to demonstrate how to form a system impedance model for stability analysis based on the three transfer functions (27)–(29). As pointed out before, our goal is an SISO model that includes the effects of the coupled currents.

### A. Operation with Source Impedance

For convenience, the source impedance in Fig. 8(a) is given as an admittance and is denoted as $Y_{\rm s}(s)$. Assume that a small-signal perturbation $\hat{v}_{\rm a}(s)$ is applied at the terminal of the PSU converter. The three current responses defined by (9)–(11) and (27)–(29) and the relationship among them can be represented by the three equivalent circuits depicted in Fig. 8(c)–(d), as explained in the following:

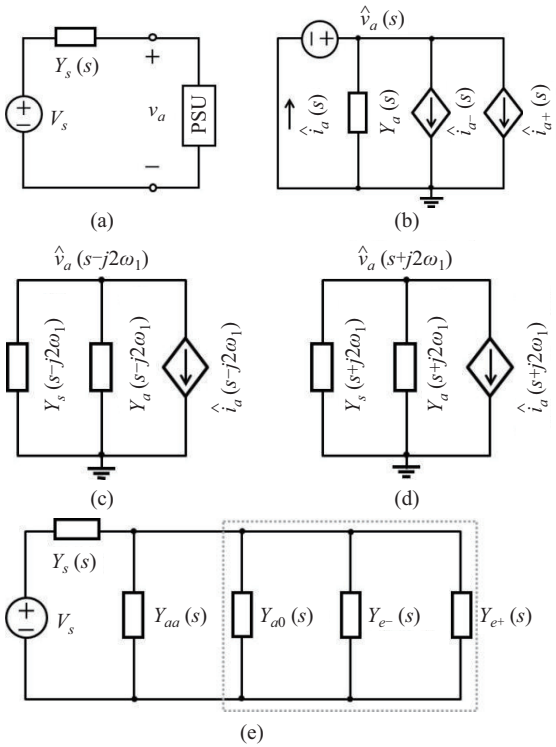


Fig. 8. (a) An elemental PSU-source system; (b) equivalent circuit at the perturbation frequency s; (c) equivalent circuit at $s-j2\omega_1$; (d) equivalent circuit at $s+j2\omega_1$; (e) final equivalent circuit at $s$.

- Fig. 8(b) is the equivalent circuit at the perturbation frequency $s$. The applied voltage perturbation appears at the terminal of the PSU and generates a current at the perturbation frequency through admittance $Y_{\rm a}(s)$ defined by (24). The two controlled current sources in parallel with $Y_{\rm a}(s)$ are defined as follows:

$$\hat{i}_{a-}(s) = \hat{v}_{\rm a}(s-j2\omega_1)Y_{c+2}(s-j2\omega_1) \tag{30}$$

$$\hat{i}_{a+}(s) = \hat{v}_{\rm a}(s+j2\omega_1)Y_{c-2}(s+j2\omega_1) \tag{31}$$

- Fig. 8(c) is the equivalent circuit at frequency $s-j2\omega_1$. It includes the source admittance $Y_{\rm s}$ and the PSU input admittance $Y_{\rm a}$ at frequency $s-j2\omega_1$. It also includes a controlled current source $\hat{i}_{\rm a}(s-j2\omega_1)$, which is coupled to the voltage perturbation $\hat{v}_{\rm a}(s)$ in Fig. 8(b) and is defined as follows:

$$\hat{i}_{\rm a}(s-j2\omega_1) = \hat{v}_{\rm a}(s)Y_{c-2}(s) \tag{32}$$

- Fig. 8(d) is the equivalent circuit at frequency $s+j2\omega_1$ and is similar to Fig. 8(c). It includes the source admittance $Y_{\rm s}$ and the PSU input admittance $Y_{\rm a}$ at frequency $s+j2\omega_1$. It also includes a controlled current source $\hat{i}_{\rm a}(s+j2\omega_1)$, which is coupled to the voltage perturbation $\hat{v}_{\rm a}(s)$ in Fig. 8(b) and is defined as follows:

$$\hat{i}_{\rm a}(s+j2\omega_1) = \hat{v}_{\rm a}(s)Y_{c+2}(s) \tag{33}$$

To understand (30)–(33), recall the definition of $Y_{c-2}$ and $Y_{c+2}$ given in (10) and (11). These controlled current sources couple the three equivalent circuits to each other. Our objective is to find the total current response of the converter at the perturbation frequency $s$. Based on Fig. 8(b), this current consists of three components:

$$\hat{i}_{\rm a}(s) = \hat{v}_{\rm a}(s)Y_{\rm a}(s) + \hat{i}_{a-}(s) + \hat{i}_{a+}(s) \tag{34}$$

The second and third component depends on the voltage of the circuit in Fig. 8(c) and Fig. 8(d), respectively. Based on the definition of the controlled current sources (32) and (33), these voltages can be calculated as follows:

$$\hat{v}_{\rm a}(s-j2\omega_1) = -\frac{Y_{c-2}(s)\hat{v}_{\rm a}(s)}{Y_{\rm a}(s-j2\omega_1)+Y_{\rm s}(s-j2\omega_1)}$$

$$\hat{v}_{\rm a}(s+j2\omega_1) = -\frac{Y_{c+2}(s)\hat{v}_{\rm a}(s)}{Y_{\rm a}(s+j2\omega_1)+Y_{\rm s}(s+j2\omega_1)}$$

These can be substituted into (30) and (31) to find $\hat{i}_{a-}(s)$ and $\hat{i}_{a+}(s)$. Based on the results and (34), the total input current response at the perturbation is found to be

$$\hat{i}_{\rm a}(s) = \hat{v}_{\rm a}(s)\cdot[Y_{\rm a}(s)+Y_{l-}(s)+Y_{l+}(s)] \tag{35}$$

$$Y_{l-}(s) = -\frac{Y_{c+2}(s-j2\omega_1)Y_{c-2}(s)}{Y_{\rm a}(s-j2\omega_1)+Y_{\rm s}(s-j2\omega_1)} \tag{36}$$

$$Y_{l+}(s) = -\frac{Y_{c-2}(s+j2\omega_1)Y_{c+2}(s)}{Y_{\rm a}(s+j2\omega_1)+Y_{\rm s}(s+j2\omega_1)} \tag{37}$$

The relationships developed and used above can be presented together by the block diagram in Fig. 9. (Recall that $s_{-2}=s-j2\omega_1$ and $s_{+2}=s+j2\omega_1$.)

### B. PSU-Source Impedance Model and Stability

The models developed in the last subsection can explain

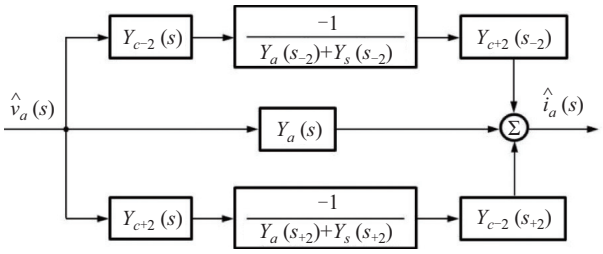


Fig. 9. Modeling of PSU total input current response at the perturbation frequency.

how coupled currents affect system stability – they effectively lower the input impedance in the presence of source impedance. The effects can be represented by the equivalent circuit given in Fig. 8(e) where $Y_{\rm a}(s)$ is purposely split into two parts: 1) $Y_{\rm aa}(s)$, which corresponds to the medium-frequency model $Z_{\rm am}(s)$ defined in (6), and 2) $Y_{a0}(s)$, which corresponds to the second and third term on the right-hand side of (27):

$$Y_{a0}(s) = Y_{0a+}(s_{-1})G_{v0-}(s) + Y_{0a-}(s_{+1})G_{v0+}(s) \quad (38)$$

In this form, the input impedance can be seen to comprise four parallel elements each associated with a physical origin, and it reduces to the medium-frequency model (6) if DC bus impedance is set to zero (that is, if $Y_{\rm DC}(s) = \infty$). The total input admittance is denoted as $Y_{\rm al}(s)$, where the letter $l$ in the subscript indicates low frequency:

$$\begin{aligned} Y_{\rm al}(s) &= Y_{\rm a}(s) + Y_{l-}(s) + Y_{l+}(s) \\ &= Y_{\rm aa}(s) + Y_{\rm a0}(s) + Y_{l-}(s) + Y_{l+}(s) \end{aligned} \quad (39)$$

For convenience, we also define the input impedance of the PSU with and without source coupling as

$$Z_{\rm al}(s) = \frac{1}{Y_{\rm al}(s)}, Z_{\rm a}(s) = \frac{1}{Y_{\rm a}(s)}. \quad (40)$$

It is evident from Fig. 8(e) that stability of the PSU-source can be determined by applying the Nyquist criterion to the following impedance ratio between the source and the PSU $[Z_{\rm s}(s) \triangleq 1/Y_{\rm s}(s)]$:

$$L(s) = \frac{Z_{\rm s}(s)}{Z_{\rm al}(s)} = Y_{\rm al}(s)Z_{\rm s}(s) \quad (41)$$

This concludes the development of the SISO system model. Recall from the discussion in Section II that the chain of harmonic interaction in a single-phase converter is actually endless, in the sense that a voltage perturbation at $\omega_{\rm p}$ will lead to current responses at $\omega_{\rm p} \pm 2k\omega_1, k = 0, 1, 2, \ldots, \infty$. In terms of the equivalent circuits in Fig. 8, this would mean that the voltage of Fig. 8(c) and (d) will each generate another current at $s - j4\omega_1$ and $s + j4\omega_1$, respectively, and so on. However, the coupling is very weak beyond $s \pm j2\omega_1$ and can be safely ignored for practical purposes.

Like the individual transfer functions (13)–(22), the three compound models (27)–(29) and the overall input impedance model (39) have all been verified by frequency response scan based on numerical simulation of a switching circuit model. Details are omitted here. Actual hardware measurements are presented in Section VI to verify the overall impedance model (39) and the system model (41).

### C. Effects of Source Impedance and Approximate Models

Quantitative results are presented in this subsection to show the main behavior predicted by the new models, the effects of the DC bus impedance, and possible ways to simplify the models. The results are provided for a representative single-phase PSU using the circuit and control depicted in Figs. 2 and 3, with the following parameters:

- Input voltage $V_{\rm in} = 277$ V (rms), voltage amplitude $V_1 = 392$ V, fundamental frequency $f_1 = 60$ Hz.
- Steady state DC bus voltage $V_{\rm DC} = 450$ V, DC bus capacitor $C_{\rm DC} = 1200$ μF.
- Input filter inductor $L = 400$ μH, input power $P = 1$ kW, switching frequency 70 kHz.
- Loop crossover frequency of input current control $f_{\rm c} = 5$ kHz, DC bus voltage $f_{\rm v} = 15$ Hz, both loops designed to have 45° phase margin.

The source impedance is modeled by an 81.5 mH inductor $L_{\rm s}$, which represents a short circuit ratio (SCR) of 2.5 at the fundamental frequency. The DC-DC converter is modeled as a constant-power load. The effects of the DC bus voltage control and DC-DC converter on the PSU input impedance will be further characterized in the next subsection.

Figure 10 compares the input impedance responses predicted by the new models $Z_{\rm a}(s)$ and $Z_{\rm al}(s)$ defined in (40) as well as the medium-frequency model $Z_{\rm am}(s)$ defined in (6). The models predict different responses below 100–150 Hz, in other words, below the second harmonic frequency. Above this frequency, all three models converge to the medium-frequency model (6), indicating that the effects of DC bus dynamics and coupled currents diminish at high frequency as assumed in [9]. For this reason, frequency responses in the rest of this section will be plotted up to 100–120 Hz.

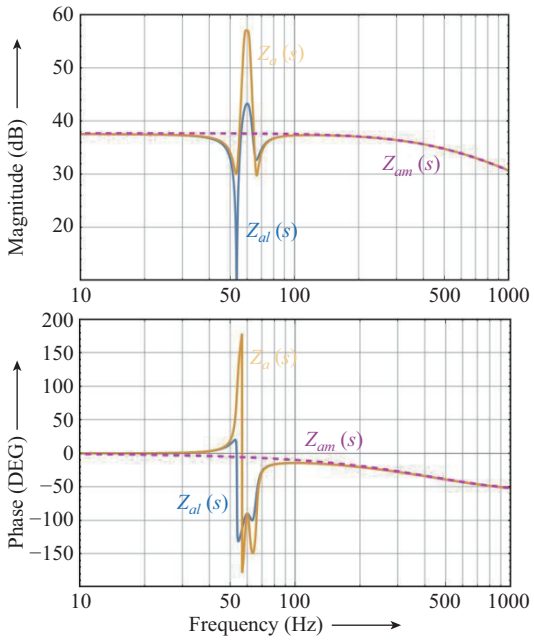


Fig. 10. Comparison of PSU input impedance responses predicted by different models.

As Fig. 10 shows, both $Z_{\rm al}(s)$ and $Z_{\rm a}(s)$ predict a large vari-

ation in the impedance magnitude and phase responses near the fundamental frequency. These variations are due to DC bus impedance and voltage control. In particular, $Z_{\rm a}(s)$ predicts a dipping of the impedance magnitude at two frequencies $f_{d1}$ and $f_{\rm d2}$ that are symmetrical about the fundamental, that is,

$$f_{\rm d2} - f_1 = f_1 - f_{d1} \quad \text{or} \quad f_{d1} + f_{\rm d2} = 2f_1$$

As will be explained later in this section, the distance from each dipping point to the fundamental frequency corresponds to the bandwidth of DC bus voltage control. The phase moves outside the $\pm 90^\circ$ range near each dipping point, indicating negative damping and potential for instability. Recall that $Z_{\rm a}(s)$ is the input impedance of the PSU converter when the converter operates with an ideal AC source.

The full model $Z_{\rm al}(s)$ includes the additional effects of the coupled current responses. It shows that the source impedance causes the input impedance to dip more at the first dipping frequency $f_{d1}$ but less at the second point $f_{\rm d2}$. The source impedance also makes $Z_{\rm al}(s)$ near the fundamental to be mostly capacitive, making it more likely to develop an unstable resonance with the inductive source impedance, especially near $f_{d1}$ where the converter impedance dips by large amount.

Source impedance also affects the phase response of $Z_{\rm al}(s)$. An intersection between the source and the PSU impedance in the magnitude response will not cause instability without at least one impedance being negatively damped. In the Bode plots, negative damping manifests itself in the phase response moving out of the $\pm 90^\circ$ range. Negative damping can be more directly seen by examining the real part of the impedance. For this purpose, responses of the real part of the three impedances compared in Fig. 10 are plotted in Fig. 11. It is interesting to note that inclusion of the source impedance actually reduces the amount of negative damping predicted by the model. Nonetheless, $Z_{\rm al}(s)$ is negatively damped in the same frequency range as $Z_{\rm a}(s)$ below the fundamental frequency. This coupled with the enlarged dipping in the magnitude creates the potential for instability.

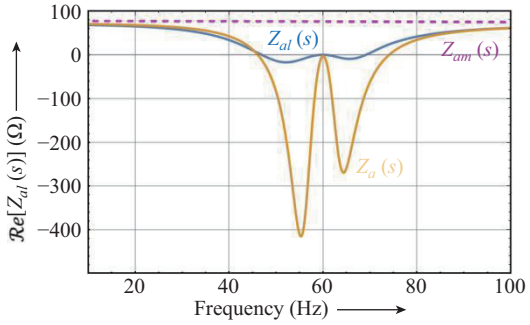


Fig. 11. Real part of the PFC converter input impedance $Z_{\rm al}(s)$ in comparison with other two models.

To see the contribution of each of the parallel admittance elements indicated in Fig. 8(e), Fig. 12 plots the magnitude response of each in comparison wit $Y_{\rm al}(s)$. The comparison shows that the term $Y_{l+}(s)$ due to the coupling of current $\hat{i}_{\rm a}(s + j2\omega_1)$ through the source impedance is much smaller than $Y_{\rm a}(s)$ and can be ignored without affecting the accuracy of the overall model $Y_{\rm al}(s)$. On the other hand, the term $Y_{l-}(s)$ is higher than $Y_{\rm a}(s)$ and dominates the overall input admittance near the fundamental frequency, especially around $f_{d1}$ and $f_{\rm d2}$ defined before, hence must be included in order to predict the low-frequency impedance correctly. Based on this, the following model can be used in place of the exact model (39):

$$Y_{\rm al}(s) \approx Y_{\rm a}(s) + Y_{l-}(s) \tag{42}$$

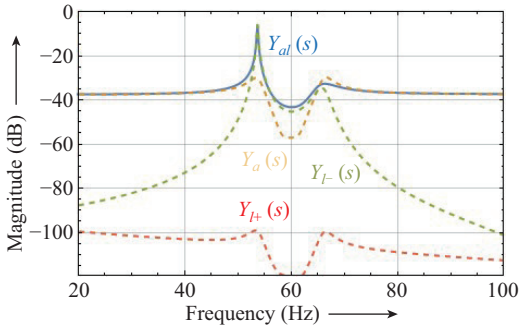


Fig. 12. Contribution of different terms in (39) to the overall input admittance $Y_{\rm al}(s)$.

There is also an interesting relationship between the two $Y_{c-2}(s)$ and $Y_{c+2}(s)$ that can be used to eliminate $Y_{c+2}$ in the definition of $Y_{l-}(s)$. Namely, $Y_{c+2}$ at frequency $s$ is equal to the complex conjugate of $Y_{c-2}$ at frequency $-s$, and vice versa:

$$Y_{c+2}(s) = Y^*_{c-2}(-s), \quad Y_{c-2}(s) = Y^*_{c+2}(-s) \tag{43}$$

Based on this and the simplified model (36), the input admittance of a PSU including DC bus dynamics and coupling through the source impedance can be written as follows to use only transfer admittance $Y_{c-2}(s)$:

$$Y_{\rm al}(s) \approx Y_{\rm a}(s) - \frac{Y^*_{c-2}(j2\omega_1 - s)Y_{c-2}(s)}{Y_{\rm a}(s - j2\omega_1) + Y_{\rm s}(s - j2\omega_1)} \tag{44}$$

### *D. Effects of DC Voltage Control and DC-DC Converter*

While the source impedance changes the amount of dipping and negative damping of the PSU impedance, the root cause for the dipping and negative damping is the DC bus impedance and voltage control. To understand this behavior, approximate models were developed for $Y_{\rm a}(s), Y_{l-}(s)$ and $Y_{l+}(s)$, and showed that each involves the following terms in the denominator, where $Y_{\rm DC}(s)$ is the DC bus admittance including the DC bus capacitor and the DC-DC converter, as defined in (23), and $H_{\rm v}(s)$ is the transfer function of DC voltage regulator:

$$Y_{\rm DC}(s \pm j\omega_1) + \frac{V_1^2}{2V_{\rm DC}} H_{\rm v}(s \pm j\omega_1) \tag{45}$$

Denoting $s \pm j\omega_1$ as $s'$ and assuming DC bus voltage control is performed by a PI regulator, that is, $H_{\rm v}(s) = K_{\rm p} + K_i/s$, we can interpret (45) as the admittance of a circuit consisting of the following elements in parallel:

- DC bus capacitor $C_{\rm DC}$,
- Input admittance of the DC-DC converter $Y_{l0}(s)$,

- An equivalent resistor $R_0 = V_1^2/(2V_{\rm DC}K_{\rm p})$ corresponding to the proportional gain of the voltage compensator, and
- An equivalent inductor $L_0 = V_1^2/(2V_{\rm DC}K_i)$ corresponding to the integral gain of the voltage compensator.

Based on this model, we can see that the term defined by (45) reaches a minimum at the parallel resonance frequency between the DC bus capacitance $C_{\rm DC}$ and the equivalent inductance $L_0$, at which $Y_{\rm a}(s')$, $Y_{c-}(s')$ and $Y_{c+}(s')$ peaks, causing the input impedance to dip. Measured in actual frequency $s$, the dipping occurs at two frequency points that are symmetrical about the fundamental, as observed in Fig. 10.

The minimum of (45) at the parallel resonance frequency identified above is

$$Y_{l0}(s \pm j\omega_1) + \frac{V_1^2 K_{\rm p}}{2V_{\rm DC}}. \tag{46}$$

Since dipping in the PSU input impedance makes it more likely to intersect with the source impedance and become unstable, it is desirable to minimize it through design of the PSU. To that end, note first that in the frequency range of interest, the DC-DC converter behaves like a constant-power load such that $Y_{l0}(s)$ can be approximated by a negative conductance $-G_1$. This has the effect to increase the dipping, but is almost unavoidable in practice. It is also worth pointing out that negative damping in the input impedance near the fundamental frequency, as discussed before in conjunction with Fig. 11, is not just caused by the constant-power behavior of the DC-DC converter and cannot be eliminated even if the load is purely resistive.

Based on (46), an effective method to reduce the dipping is to increase the proportional gain of the voltage compensator. When the crossover frequency is kept constant, increasing the proportional gain is equivalent to increasing the phase margin of the voltage loop. Section VI will present measurements to show the application of this method as a practical solution to low-frequency resonance.

We conclude this section with a couple final comments:

- Transfer function $H_{\rm a}(s)$ has been assumed unity in the quantitative analyses presented in this section. This function models the small-signal response of the RMS-voltage generation circuit. Depending on how this function is performed, a dynamic model may be needed/used to include its effects on the impedance.
- As pointed out in Subsection IV.C, the effects of DC bus dynamics and the coupled currents are important to consider only up to the second harmonic frequency. Above that frequency, the medium-frequency model (6) can be used in place of $Z_{\rm al}(s)$ defined in (40).

## V. Control Delay and High-Frequency Impedance

The models developed so far assumed analog control implementation. In recent years, digital control has become common for PSUs used in data centers. Digital control introduces delay that affects the impedance at high frequency. The purpose of this section is to incorporate the delay into the impedance model and discuss its effects on stability.

Since delay only affects the impedance at high frequency, it can be safely ignored in the low frequency models studied in the last three sections. Based on that, our starting point is the medium-frequency model (6). Based on the simplified diagram in Fig. 4, the effects of digital control and PWM delay can be accounted for by a lumped delay after the current compensator. To define this equivalent delay, however, one has to consider the variable duty ratio over a line cycle. To measure the true average and avoid switching noise, the PSU input current and voltage are usually sampled at the middle of the on-time of the switch. This causes the sampling delay to vary over a line cycle. The PWM delay also varies with the duty ratio when single-edge modulation is used [27]. This is illustrated in Fig. 13 where current and voltage measurements are taken at the middle of the on-time in the switching cycle that starts at $t = (k-1)T_{\rm s}$. The digital controller uses the rest of that cycle as well as possibly $n$ additional cycles to execute the control functions, and updates the PWM reference at $t = (k+n)T_{\rm s}$. With a trailing-edge modulation as assumed in the figure, the delay introduced by the PWM is equal to $T_{\rm d2} = dT_{\rm s}$, $d$ being the duty ratio of the switch. Based on this and Fig. 13, we have

$$T_{d1} = \left(1 - \frac{d}{2}\right) T_{\rm s} \tag{47}$$

and the total delay is

$$T_\Sigma = T_{d1} + nT_{\rm s} + T_{\rm d2} = \left(1 + \frac{d}{2} + n\right) T_{\rm s} \tag{48}$$

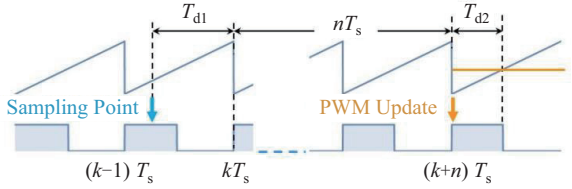


Fig. 13. Digital control and PWM delay in a PSU.

Note that $n$ would be zero if the controller finishes all control functions and updates the PWM reference within the cycle in which input samples are taken. This means that the minimal delay is $(1 + 0.5d)T_{\rm s}$. Since the duty ratio of a PFC converter varies with the input voltage, the total delay $T_{\rm d}$ changes periodically at twice the fundamental frequency. Such a time-dependent delay cannot be used in an impedance model. As an approximation, we propose to use the average of $T_\Sigma$ over half a line cycle in place of the variable actual delay:

$$T_{\rm d} = 2f_1 \int_0^{\frac{1}{2f_1}} T_{\rm s} \left[1 + \frac{{\rm d}(\tau)}{2} + n\right] {\rm d}\tau \tag{49}$$

This average lumped delay allows us to modofy (6) to account for the delay:

$$Z_{\rm ah}(s) = \frac{sL + V_{\rm DC} e^{-sT_{\rm d}} H_{\rm c}(s)}{1 + GV_{\rm DC} e^{-sT_{\rm d}} H_{\rm c}(s)} \tag{50}$$

Delay is known to cause converter impedance to be negatively damped at high frequency. Depending on current

compensator design and the amount of delay, the negative damping typically starts at 20–30% of the PWM sampling frequency. The effects of this negative damping on data center power system stability depend on the system impedance as well as other factors that may affect the PSU input impedance at high frequency.

One such factor is the PSU input filter. Since the first resonance frequency of the filter is usually outside the current control bandwidth, the filter does not need to be considered when the low- and medium-frequency models $Z_{\text{al}}$ and $Z_{\text{am}}$ are used. However, in the frequency range where delay cannot be ignored, the filter must be considered as well.

As an example, Fig. 14 shows the responses of $Z_{\text{ah}}(s)$ for the example converter studied in Section IV. The total (average) delay $T_{\text{d}}$ is assumed to be 38 μs. To account for the additional phase shift caused by delay, the current loop crossover frequency is reduced to 2 kHz, with the phase margin (without delay) increased to 60°. The EMI filter uses a typical two-stage design, each stage consisting of a 1.5 μF capacitor and an 10 μH inductor, with an additional 1 μF at the input.

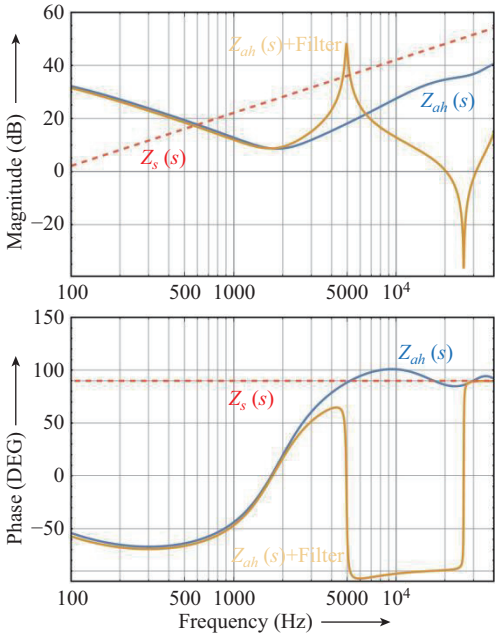


Fig. 14. Frequency responses of input impedance model $Z_{\text{ah}}(s)$ with and without input filter. Dashed lines represent output impedance of a strong source.

Without the filter, the input impedance is inductive above the current loop crossover frequency. The phase response moves above 90° near 5 kHz and stays above 90° until ∼ 20 kHz, indicating that the input impedance is negatively damped in this frequency range because of the delay. The EMI filter causes a parallel resonance at 5 kHz and the impedance becomes capacitive thereafter. With capacitive imaginary part of the impedance, negative damping causes the phase angle to go below −90°. Note that the impedance is also capacitive below the current loop crossover frequency (2 kHz). This is caused by the integral term of the current compensator that dominates the impedance and is equivalent to a capacitor. However, there is no negative damping in that frequency range.

Based on the typical high-frequency impedance responses illustrated in Fig. 14, we now examine how PSU may develop high-frequency resonances.

Below the current loop crossover frequency, the capacitive input impedance of the PFC converter may form resonance with an inductive source impedance. However, since the converter impedance is positively damped, a resonance in this frequency range is stable unless there is negative damping in the source impedance, e.g. when the PSU is powered from a UPS that exhibits negative damping.

Between the current loop crossover frequency and the first resonance (5 kHz in Fig. 14), the PSU input impedance is inductive, hence requires a capacitive source impedance to develop a resonance. A passive distribution network cannot be capacitive. However, a UPS output impedance can be capacitive because of the output filter capacitor. Control delay may also cause the UPS output impedance to be negatively damped in this frequency range, such that a resonance may form and become unstable even if the power supply impedance is passively damped, as in the case shown in Fig. 14.

Above the first resonance of the filter, the capacitive impedance of the PSU together with its negative damping creates a potential for unstable resonance with an inductive source impedance. As an example, Fig. 14 includes the impedance of an 2 mH inductor, which intersects with the PFC converter impedance at slightly above 5 kHz. This would lead to an unstable resonance because the PSU impedance is negatively damped starting from 5 kHz. On other hand, a 2 mH inductor would translate into an SCR of 100 for the PSU at the fundamental frequency, which is unreasonably high for any practical source. However, there are still possibilities for resonance in this high-frequency resonance in data centers:

- Between PSUs and a UPS: For power supplies, UPS output impedance becomes inductive again at high frequency because of the parasitic inductance of the circuit between the UPS and the power supply, including possibly that of a step-down transformer. Due to the short distance, this inductive impedance is low and may form resonance with the power supplies in the high-frequency range.
- Between two groups of PSUs: In a radial network as used in data centers, PSUs in different parts of the building may form a resonance with each other if the impedance of the network that separates them intersects with the PSU impedance in the range indicated above. This mode of resonance is different from other modes discussed above and requires a different system model. Part II of the work will present such a system model.

## VI. Laboratory Measurements

A number of commercial power supply products used in Meta data centers have been tested by the team in collaboration with the manufacturers to verify the impedance models and analyses presented in this work. Tests are performed on individual power supplies in both single- and three-phase configurations. The DC-DC converter stage is treated as an integral part of each power supply and is always measured

together the PFC front-end converter. The DC-DC converter also effectively isolates the PFC input impedance from the load impedance such that there is no need to consider the actual characteristics of server point-of-load regulators. The laboratory setup includes programmable AC sources, DC electronic loads, and a Venable frequency response analyzer for measuring the impedance responses over frequency [28].

Because of saturation of the injection transformer used in the automated impedance measurement system, measurement of input impedance below the second harmonic frequency is performed by programming the AC source to inject a harmonic voltage directly. To avoid unintended coupling through source impedance, the power rating of the AC power source is selected to be 10 times higher than the power of the unit under test.

In most cases, impedance measurement covers the frequency range from 1 Hz to 50 kHz. Given the focus of this work, however, we will present low- and high-frequency measurements separately, such that the characteristics in each frequency range can be better seen. Measurements from two power supplies are presented below and they will be referred to as PSU A and B for easy reference.

As a small-signal method, impedance-based stability analysis should be performed at different operation points of the system. To support that, PSU impedance measurement has also been taken with different power and input voltage, usually at 10% increment in power and at several typical input voltage levels that are specified based on actual data center operation conditions. For system stability in the low-frequency range, full-power operation is the most critical condition, hence will be the focus of discussion in this section.

Figure 15 shows the magnitude and phase responses of input impedance for PSU A in one operation condition. The triangles mark the measurements points while the continuous lines are calculated using the analytical model (27) developed in Section III. The analytical model correctly predicts the characteristic dipping in the impedance magnitude at two frequency points that are symmetrical about the fundamental. Negative damping near these dipping points are apparent and are captured well by the model. There is noticeable difference between the measured and modeled phase responses outside the two dipping points. They are attributed to several factors in the actual power supply design that are not considered in the model:

- Discontinuous conduction mode of the boost current, which occurs for over 40% of each fundamental cycle in this particular product because of its unique circuit design.
- Adaptive voltage compensator gain, a unique feature of the tested PSU that could be activated by the ripple caused by the injection.
- Dynamics of the RMS-voltage generation circuit that are not modeled [$H_{\mathrm{a}}(s) = 1$ is used in the model].
- Coupling through the impedance of the programmable source, which is low but not completely negligible.

Since the difference is in the frequency range where the power supply impedance is positively damped, it does not affect the ability of the model to predict low-frequency instability and resonance. Considering that, no further effort was made to model the additional complexity listed above.

To verify the system model and stability analysis method presented in Section IV, PSU A is also operated with an 130 mH inductor inserted between its input and the AC source. (In fact, the test was performed on three power supplies with a 43 mH inductor inserted on the common neutral return, which is equivalent to an 130 mH inductor in each phase. The reason for this test setup will be further discussed in Part II.) An oscillation in the input current and voltage is observed as captured by the oscilloscope waveforms in Fig. 16. Fourier analysis shows a pair of harmonics at 54 Hz and 66 Hz in both the voltage and current.

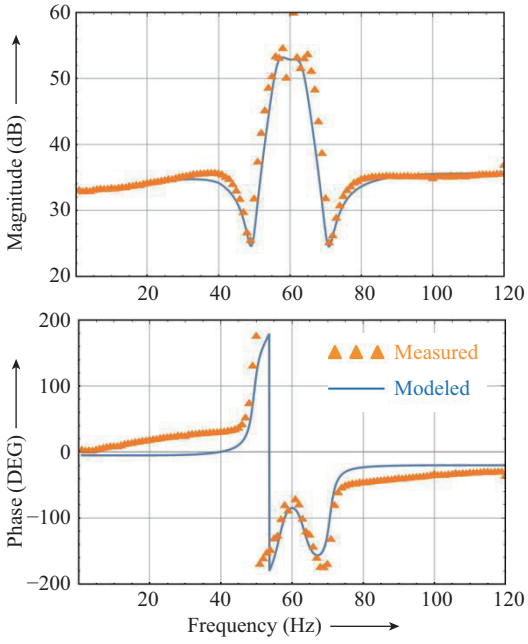


Fig. 15. Comparison of frequency response predicted by $Z_{\mathrm{a}}(s)$ with laboratory measurement of a power supply.

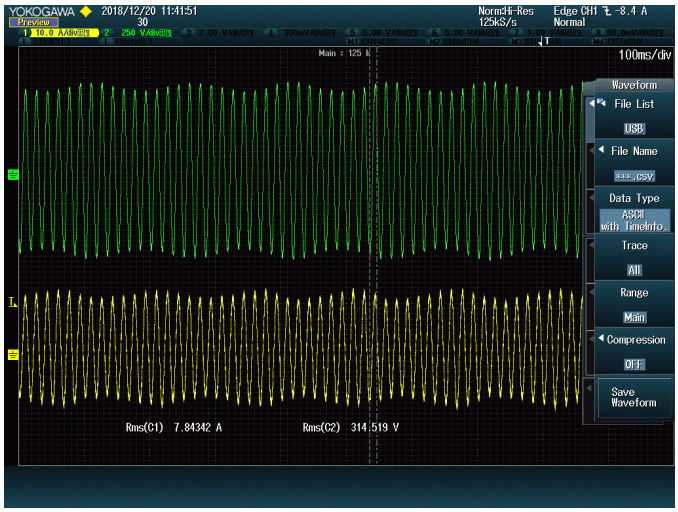


Fig. 16. Low-frequency resonance measured in a power supply operating with a high-impedance source.

To correlate this resonance with stability analysis based on

the SISO model, Fig. 17 shows the frequency response of the 130 mH inductor impedance against that of the equivalent input impedance $Z_{\rm al}(s)$ defined in (40). As can be seen, the two impedances form an unstable resonance near 66 Hz, which explains the observed resonance. The 54 Hz harmonic is created by the transfer admittance, as explained in Section III.

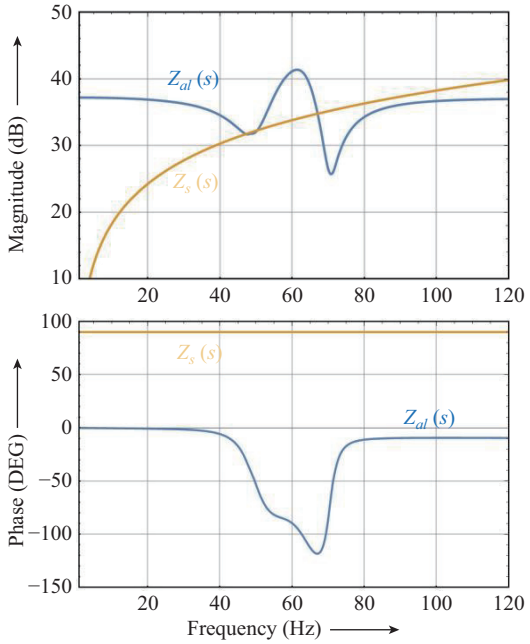


Fig. 17. Impedance analysis of the resonance presented in Fig. 16. $Z_{\rm s}(s)$: impedance of an 130 mH inductor.

As pointed out in Section IV, dipping in the impedance magnitude and negative damping in the associated frequency range are the consequences of DC bus voltage control. It is also a typical root cause for low-frequency resonance. Increasing the phase margin of DC bus voltage control has the effect to reduce the dipping in the impedance magnitude and often provides a simple but effective solution to low-frequency system resonance. To demonstrate that, DC bus voltage control of PSU A was modified to increase the phase margin by increasing the proportional gain of the PI regulator. Fig. 18 shows the input impedance measured after this modification and compares it again the prediction by the analytical model $Z_{\rm a}(s)$. As can be seen, the design change removed most of the dipping in the impedance magnitude. On the other hand, the negative damping near the fundamental frequency is still present. This was one of the methods implemented to mitigate the data center resonance problem described in Section I.

To verify the high-frequency impedance model developed in Section V, Fig. 19 compares the measured and calculated input impedance responses of PSU B that uses the variable sampling method described in Section V. The variable delay time is modeled by the average defined in (49). The measured impedance, marked by orange triangles, indicates negative damping between 7 kHz and 20 kHz, where the phase response drops below $-90^\circ$ while the magnitude shows capacitive response because of the filter capacitor. Prediction by the analytical model, which includes the input filter, follows the

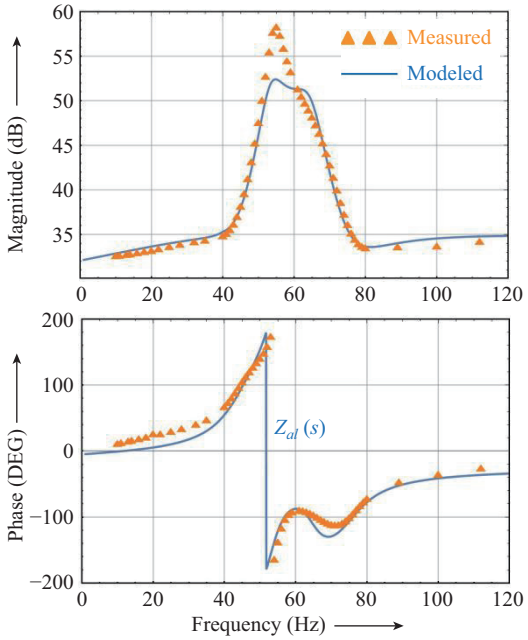


Fig. 18. Reduction of impedance dipping by modification of DC bus voltage control.

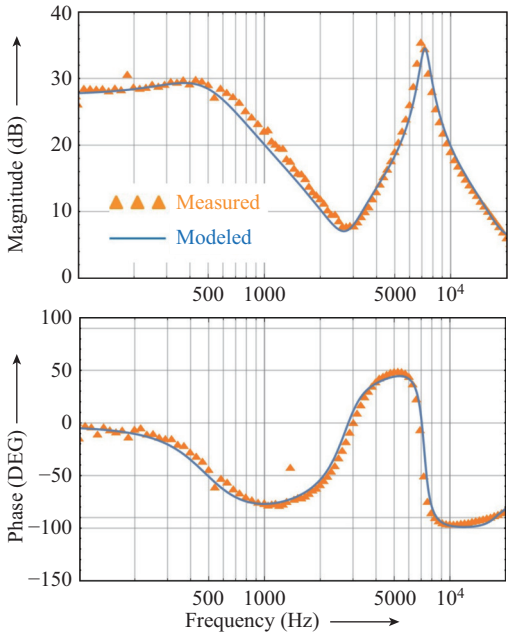


Fig. 19. High-frequency impedance responses and negative damping due to control delay.

measurements at all frequencies. The overall impedance responses are also similar to the general characteristics presented in Section V and exemplified in Fig. 15. Practical solutions to high-frequency resonance problems have been discussed in [7] and can be applied to power supplies as well.

## VII. Summary

New input impedance models are developed for single-phase PFC converters for stability modeling and analysis of data center power systems. The models are in the phase

domain and include DC bus dynamics as well as the coupled current responses. The modular approach makes the development process more trackable and facilitates the use of the models in their analytical forms to gain general insights. A new method is also presented to account for the effects of the coupled current response in system stability analysis while keeping the model in SISO form to avoid the complexity and disadvantage associated with the generalized Nyquist criterion.

The developed models indicate that DC bus impedance and voltage control dominate PSU input impedance below the second harmonic frequency and cause the impedance to dip at two frequencies that are symmetrical about the fundamental. This, together with the characteristic negative damping, is shown to be a common root cause for system instability and resonance below the second harmonic frequency, especially when source impedance is high.

Above half the current loop crossover frequency, digital control and PWM delay has strong effects on the PFC converter's input impedance. A high-frequency impedance model is presented to capture these effects, including the characteristic negative damping. Variation of delay over a line cycle is removed by using its average.

The table below summarizes the features and applicable frequency ranges of the new models developed in this paper relative to the medium-frequency model presented in [9]. The three frequency ranges correspond to the low-, medium- and high-frequency range defined in Section II. Part II of the work will present the application of the developed models in stability study of overall data center power systems.

TABLE I
SUMMARY OF FEATURES OF DIFFERENT IMPEDANCE MODELS

| Frequency Range | $f < 2f_1$ | $2f_1 \leq f \leq 0.5f_c$ | $0.5f_c < f$ |
|---|---|---|---|
| DC Voltage Control | Yes | No | No |
| AC Current Control | Yes | Yes | Yes |
| Control & PWM Delay | No | No | Yes |
| Input Filter | No | No | Yes |
| Impedance Model | $Z_{al}$–Eq. (40) | $Z_{am}$–Eq. (6) | $Z_{ah}$–Eq. (50) |

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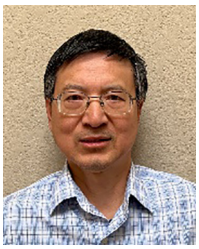

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