Single-stage Five-level Common Ground Transformerless Inverter with Extendable Structure for Centralized Photovoltaics

Vishal Anand\textsuperscript{\textcopyright}, Student Member, IEEE, Varsha Singh\textsuperscript{\textcopyright}, Senior Member, IEEE, Jagabar Sathik\textsuperscript{\textcopyright}, Senior Member, IEEE, and Dhafer Almakhles\textsuperscript{\textcopyright}, Senior Member, IEEE

Abstract—The paper presents a five-level common ground type (5L-CGT), transformer-less inverter topology with double voltage boosting. The proposed inverter uses eight switches and two capacitors, charged at input voltage level. The inverter in its basic form acts as a string inverter for low-power PV applications. However, it can be extended to work as a scalable multi-level inverter with higher power handling capability to act as a centralized inverter. The working of the inverter with the sizing of the components is presented with mathematical analysis. The efficiency of the proposed PV inverter is found using thermal losses associated with switches using PLECS software. A prototype of 1 kW has been designed, and experimentation has been carried out. Various loads with a lagging power factor up to 0.6 have been tested with the inverter to establish the usability of the proposed inverter in a worst-case emulated home-use scenario. The total harmonic distortion (THD) at the output has been recorded using a power quality analyzer with voltage and current THD values of 4.5\% and 2.5\%, respectively, which lies within the limits of IEEE 519 standards. The highest power conversion efficiency of the inverter has been recorded to be 96.20\%.

Index Terms—Active and reactive power, boost inverter, common mode voltage (CMV) grid-tied inverters, inrush current, leakage current, photovoltaics.

I. INTRODUCTION

SolAR Energy is a clean, renewable energy source with minimal environmental issues. This encourages developing economies to facilitate their usage of renewable power generation. It is motivated by western economies that strongly fulfill their 80\% of their energy demand using renewable energy sources. The critical constraint for the setup of a photovoltaic (PV) plant is a geographical location with irradiance greater than 600 W/m\textsuperscript{2} daily for at least 300 days in a year [1]. This is necessary to get returns for the non-recurring investment made on the installation and commissioning of the PV plant. However, PV installation is costly and requires optimal conditions to harness maximum power from the PV plant in adverse conditions. The key issues that impact PV power generation are power losses across power electronics converters, shading conditions, and leakage current. There are two configurations for a grid-connected PV inverter. Firstly, a two-stage power conversion requires a combination of a DC-DC converter and a DC-AC inverter. Secondly, a single-stage converter eliminates the requirement for a DC-DC converter. These optimal values for PV grid-connected inverters are characterized using leveled cost of electricity (LCOE) as expressed in (1).

$$\text{minimize}\quad \text{LCOE} = \text{minimize} \left[ \frac{C_i}{E_i} \right]$$ (1)

where $C_i$ and $E_i$ are the PV inverter cost and output power injected to the grid. The two-stage conversion has certain limitations found using LCOE regarding system cost, efficiency, power density, thermal management, and transformers. These limitations are turned out by single-stage conversion that does not require galvanic isolation, improving the power density, efficiency, and cost.

A critical review of single-phase PV inverters for grid-connected applications is presented in [2] and [3]. This technical review presents the application of different power converters for both stages using isolated and non-isolated power converters and single-stage conversation, with an analysis of the selection and sizing of components for the PV inverters. A proper characterization of the impact of dust on a grid-connected PV inverter to improve the techno-economic performance is presented in [4]. In [5] and [6], asymmetrical multilevel inverters using SVPWM for PV multilevel inverters harnessing solar energy for injecting power to the grid.

Figure 1 shows a grid-connected PV inverter with the possibility of leakage current caused due to parasitic capacitance $C_{PV}$ created between PV and the ground terminal. The common-mode voltage across the capacitor $C_{PV}$ and corresponding leakage current is expressed in (2) and (3), respectively.

$$V_{CM} = \frac{V_{an} + V_{bn}}{2} + \frac{V_{an} - V_{bn}}{2} \left( \frac{L_{f2} - L_{f1}}{L_{f1} + L_{f2}} \right)$$ (2)
Fig. 1. Common mode circuit for grid-connected inverter.

\[ I_{\text{leak}} = C_{PV} \frac{d(V_{CM})}{dt} \]  \hspace{1cm} (3)

where \( V_{an} \), \( V_{bn} \), are the voltages across terminals \( a \) and \( b \) with respect to neutral \( n \). The inductors \( L_{f1} \) and \( L_{f2} \) are grid filters, while \( C_f \) is the output capacitor across the grid. The topology presented in [7]–[9] has different ground potential for PV and grid. However, common-mode voltage and reduction in leakage current are addressed using a specific controller or pulse width modulation (PWM) strategy. The topology presented in [10] and [11] has lesser leakage current. However, voltage stresses on the switches are high. In [12]–[16], efficient single-stage transformerless inverters are presented with inductive loading capabilities with lesser leakage current suitable for grid-connected applications. However, inverter efficiency is low in the event of partial shading due to disturbance in the common-mode voltage (CMV). Resonance-based suppression of leakage current is adopted in [17] and [18]. However, the H-bridge used for polarity has high switching stresses. An additional switch is used to surpass the leakage current. A novel method is adopted in [19]–[21] to reduce CMV due to junction capacitance. However, this methodology requires a separate controller and passive components to contain the junction parasitic. The network topology presented in [22]–[24] offers CGT with switched capacitors replacing the requirement for an additional switch to suppress leakage current. However, high charging current is a big challenge in switched capacitor circuits. In [25], a costly two-stage transformerless inverter is presented. The structures presented in [26]–[30] for PV application use different control algorithms to reduce capacitor ripples. Moreover, uneven current stress on switches still prevails. A few existing 5L CGT transformerless inverters are exemplified in Fig. 2. These topologies either have H-bridge for polarity generation or uneven blocking voltages. This limits the extension of topologies for higher levels. The advantages for the topology proposed in this research are as follows:

1) Common ground type configuration cause less leakage currents.
2) Sensor less, natural voltage balancing of switched capacitors.
3) More charging states than other topologies provide stable capacitor voltage during a steady and dynamic state.
4) An extended structure suits the characteristics of the proposed inverter as a centralized inverter.
5) Voltage stress across the switch and capacitor remains uniform for extended structure, ensuring better power handling capability.

The presentation of the paper is as follows: Section II explains a system description for the proposed topology with its switching scheme, theoretical design consideration for selection, and sizing of the capacitors. Section III describes the mathematical modeling and control of a common ground-type PV inverter. Section IV discusses component selection for validating the proposed PV inverter. Later experimental validation and comparative assessment are discussed in Sections V and VI. Finally, Section VII concludes the article.

II. SYSTEM DESCRIPTION

This section overviews operation and control of grid connected PV inverter. The overall system is shown in Fig. 3, control of grid voltage, and current \( V_g \), \( I_g \). The CGT inverter and grid interface through two filters \( L_{f1} \), and \( L_{f2} \). The characteristics of PV are exhibited by using programmable DC sources, and the power circuit for the inverter comprises six IGBTs with reverse conducting capability and two IGBTs without anti-parallel diode, and two capacitors. Capacitors in
the proposed CGT topology helps to achieve twice voltage boost, making them suitable for single-phase transformerless application, in a way eliminating two-stage power conversion. Subsections for the detailed system are classified as a switching and modulation scheme for the proposed CGT PV inverter, filter design, and topology extension for higher voltage levels.

A. PV Array

The MPPT controller tunes the system continuously in such a manner that MPP always achieves nonetheless variation in load or meteorological conditions. The P&O control algorithm for MPPT is used to deal with the non-idealties related to variation in meteorological and irradiance conditions. The proposed CGT transformerless PV inverter uses a fixed DC link. $C_{\text{in}}$ is set to $V_{\text{MPP}}$ to maintain single-stage power operation of the converter. The MPP is extracted using a PV array. An important condition for the successful operation of the inverter is the voltage across the DC link, $C_{\text{in}}$ must be equal to the minimum power extracted using PV output.

B. Switching and Modulation Scheme for proposed CGT PV inverter

Modes of operation for attaining voltage levels is exemplified in Fig. 4.

Mode I- During this mode, both the capacitors $C_1$ and $C_2$ discharge by turning ON three switches, $S_4$, $S_6$, and $S_7$ to achieve $+2V_{\text{PV}}$ at the output terminals. The dc link capacitor, $C_{\text{in}}$ remains idle during this mode.

Mode II- During this mode, both the capacitors $C_1$ and $C_2$ are charged by turning ON five switches, $S_1$, $S_3$, $S_5$, $S_7$, and $S_8$ to achieve $+V_{\text{PV}}$ at the output terminals. The output of the DC link, $C_{\text{in}}$ is reflected across the output terminals.

Mode III- During this mode also, both capacitors $C_1$ and $C_2$ charge by turning ON four switches, $S_1$, $S_3$, $S_6$ and $S_7$ to achieve ZeroLevel at the output terminals. The short circuit path reflects zero level at the output that is created by simultaneous turning of switches $S_5$ and $S_7$.

Mode IV- During this mode, four switches $S_1$, $S_4$, $S_6$, and $S_8$ conduct to achieve $-V_{\text{PV}}$ at the output terminals. Capacitor $C_1$ charges with the DC link $C_{\text{in}}$, while the capacitor $C_2$ discharges to create the first negative voltage level which is also equal to $-(V_{C2})$.

Mode V- During this mode, both capacitors $C_1$ and $C_2$ discharges by turning ON three switches, $S_2$, $S_4$, and $S_6$ to achieve $-2V_{\text{PV}}$ at the output terminals which is also equal to $-(V_{C1} + V_{C2})$. The DC link capacitor, $C_{\text{in}}$ remains idle during this mode.

In order to limit the capacitor charging current ripples, a small inductor of 33 µH is used in series with source to achieve quasi-soft charging (QSC) of capacitors. This mechanism limits the capacitor charging current ripples to less than three times that of peak-to-peak load current. The proposed inverter is driven by an alternate-phase opposition disposition level shifted pulse width modulation scheme (APOD-LS-PWM) that uses four high-frequency carrier signals at 20 kHz, and the gate pulses across the switches are shown in Fig. 5(a) and (b) respectively.

C. Filter Design

Selection of filter for grid-connected inverters is subject to current ripple and the voltage drop. This indicates that a large filter inductor-size reduces the current ripple, at the same time voltage drop is high. Another challenge is to design the filter depending on the reactive power needed by the load. A large capacitance incorporated in the filter may lead to high current.
Fig. 4. Modes of Operation for attaining voltage levels. (a) Mode I (+2V_{PV}). (b) Mode II (+V_{PV}). (c) Mode III (Zero level). (d) Mode IV (−V_{PV}). (e) Mode V (−2V_{PV}).

Fig. 5. Modulation scheme for level generation. (a) Modulating and carrier signals. (b) Gate pulses across switches.
ripples across the inverter switches. It is necessary to choose the resonant frequency, which must satisfy the controllers. Industrial standards suggest the bandwidth of the controller to be \( \frac{1}{2 \pi f} \) of the switching frequency. The proposed CGT structure, is operated at unity power factor, and there is very less reactive power requirement. Thus, only the L filter is sufficient to tune the grid voltage. Additionally, a capacitor-based LC filter reduces the L value, but incorporates current ripples in switches. Thus, only the L filter is chosen for developing the prototype.

The selection of inductor is based on maximum peak-to-peak current across the load \( (i_o) \) in one fundamental cycle. The current ripple is considered to be 20% of the rated current. Peak current is nearly 6.14 A for a 1 kW experimental prototype. The maximum amount of ripple current is expressed as in (4).

\[
\Delta (i_{L, \text{max}}) = (20\%) i_o
\]
\[
= 0.2 \times 6.14 = 1.228 \text{ A} \quad (4)
\]

At 20 kHz, the computation of inductance is expressed as in (5).

\[
L = \frac{V_{PV}}{4 \times \Delta (i_{L, \text{max}}) \times f_{SW}}
\]
\[
= \frac{\frac{200}{4 \times 1.228 \times 20000}}{} = 2 \text{ mH} \quad (5)
\]

where the input voltage from the programmable DC source is 200 V. Thus, a 2 mH inductor is sufficient to limit voltage and current ripples in meeting THD standards prescribed by IEEE 519 guidelines.

D. Extension of CGT PV Inverter

The proposed topology can be extended for generation of higher voltage levels. This extension is achieved by an increase in the number of switches and capacitors. The generalized expression for extended structure presented in Fig. 6 is listed in Table I. Merits for the extended structure can achieve higher voltage levels with uniform voltage stress across the capacitors and switches. This feature ensures the characteristics of the proposed inverter as the centralized inverter, that possesses better power handling capability for high-power applications, with reduced voltage stress across the semiconductors and capacitors.

III. MODELING AND CONTROL OF CGT PV INVERTER

A. PLL Structure

Grid-connected inverters require a continuous and accurate measurement of frequency and voltage of the grid. Thus, estimation of grid angle is necessary for synchrony for injecting power to the utility. A phase-locked loop (PLL) is a closed loop system in which an internal oscillator is used to control the time and phase as shown in Fig. 7. The phase angle of the utility is critical information for the operation of power devices used in PV inverters. The error between the output signal and the reference signal is ensured to be minimum by using a PLL. It should ensure a clean phase lock and reject any sources of fluctuation or voltage dips in order to avoid phase mismatch or frequency variation in electrical utility.

\[
V_{d}^{\text{inv}} = i_d R_f + L_f \frac{d}{dt}(i_d) - \omega_s L_f i_q + V_g^{d}\quad (6)
\]

Since \( q \)-axis voltage of grid is zero,

\[
V_{q}^{\text{inv}} = i_q R_f + L_f \frac{d}{dt}(i_q) + \omega_s L_f i_d + 0\quad (7)
\]

\( V_{d}^{\text{inv}} \) and \( V_{q}^{\text{inv}} \) are the control parameters in DC domain obtained after Parks transformation. Inverter voltage along \( d \)
and q axis is given as \( v_d = V_{d}^{\text{inv}} - \omega_s L_f i_q - V_g \) and \( v_q = V_{q}^{\text{inv}} - \omega_s L_f i_d \). The open loop plant function is expressed as:

\[
G_p(s) = \frac{v_d(s)}{i_d(s)} = \frac{v_g(s)}{i_q(s)} = \frac{1}{L_f s + R_f} \tag{8}
\]

This first order system is controlled using a PI controller, and the value of \( K_p \) and \( K_i \) is set using pole zero cancellation. The open loop transfer function is expressed as:

\[
G_{ol}(s) = G_p(s) G_c(s) = \frac{1}{\frac{L_f}{R_f} s + 1} \frac{K_p s + K_i}{s} = \frac{K_p}{L_f s} \tag{9}
\]

The closed loop transfer function is expressed as:

\[
G_{cl}(s) = \frac{G_{ol}(s)}{1 + G_{ol}(s) H(s)} = \frac{\frac{L_f}{R_f} s + 1}{\frac{L_f}{R_f} s + 1} \tag{10}
\]

As mentioned in the filter design, the cut-off frequency of the closed-loop system is 10% of that of the switching frequency. The values of \( K_p \) and \( K_i \) are determined as:

\[
\begin{align*}
K_p &= \frac{L_f}{R_f} \\
K_i &= \frac{2\pi f_{SW} L_f}{10} \\
K_p &= \frac{2\pi f_{SW} R_f}{10}
\end{align*} \tag{11}
\]

Thus, \( K_p \) of \( K_i \) is determined using the closed loop transfer function.

C. DC Link Control

The input DC link capacitor \( C_{\text{in}} \) is large enough to be considered as a voltage source. Applying the power balance conditions at DC link, the differential equation is expressed as:

\[
P_{\text{PV}} = \frac{d}{dt} \left[ \frac{1}{2} (C_{\text{in}} V_{\text{DC}}^2) \right] + P_{\text{ac}} + P_{\text{loss}} \tag{12}
\]

PV output power acts as a feed-forward signal is less and handled by the controller. The transfer function of DC link voltage control is given as:

\[
G_{DC}(s) = \frac{V_{\text{DC}}^2}{P_{\text{ac}} - P_{\text{PV}}} = \frac{2}{C_{\text{in}} s} \tag{13}
\]

Here, the \( P_{\text{loss}} \) is neglected and it is handled by the controller itself as it has an integrator. This integrator ensures steady state error across the DC link to be zero. Transfer function for the DC link controller at desired crossover frequency is expressed as:

\[
G_c(s) G_v(s) = \left( \frac{K}{s} \right) \left( \frac{s + \frac{\alpha}{s + r}}{s + r} \right) \left( \frac{2}{C_{\text{in}} s} \right) \tag{14}
\]

where \( r = \omega \sqrt{\alpha}, \alpha = \frac{1 + \pi \sin(\theta_{\text{boost}})}{1 - \sin(\theta_{\text{boost}})}, \theta_{\text{boost}} = 45^\circ - 60^\circ \) and \( \omega_c = (0.3 - 0.1) \frac{2\pi f_{\text{SW}}}{10} \).

IV. COMPONENT SELECTION FOR VALIDATION OF CGT PV INVERTER

This section describes the criteria for selection of energy storing capacitors and power switches used in the power circuit of the CGT PV inverter.

A. Selection of Capacitors

Conventional PV inverters comprised virtual DC bus or pump charge based inverters fail to limit the inrush current across the capacitors. Charging current across the capacitor is limited only by the equal series resistance (ESR) of the capacitor. However, the issue of high charging current ripples occurs in proposed PV inverters. In order to limit charging current this a small inductor is connected in series with the source.

For the proposed inverter from Fig. 9, it is found that output voltage is quarter symmetry and maximum discharge period (MDP) of capacitor \( C_1 \) varies from \( \theta_2 \) to \( \theta_4 \). Similarly, for the
Capacitor $C_1$ charges during $\pm V_{PV}$ and zero level, whereas capacitor $C_2$ charges during $V_{PV}$ and zero level. Thus, the charging current for capacitor is dependant on equivalent resistance offered by load, switches and capacitors ($R_{eq}$) for each level formation.

\[
\begin{align*}
    i_{C1,max} &= \frac{P_0 T}{\pi C_1 V_{PV} V_m R_{eq}} \sqrt{4 - \frac{1}{V_m^2}} \\
    i_{C2,max} &= \frac{P_0 T}{\pi C_2 V_{PV} V_m R_{eq}} \sqrt{4 - \frac{1}{V_m^2}}
\end{align*}
\]

The current stress on switch $S_1$ is combination of capacitor charging current $i_{C1}$, $i_{C2}$ and load current, $I_m$ expressed as:

\[
i_{S1,max} = i_m + i_{C1,max} + i_{C2,max}
\]

Similarly, current stress on other switches is equal to load current expressed as:

\[
i_{S2,max} = i_{S3,max} = i_{S4,max} = i_{S5,max} = i_{S6,max} = i_{S7,max} = i_{S8,max} = I_m
\]

C. Power Loss Analysis

An overview of conduction and switching losses in semiconductors are given here. In conduction loss analysis, the ripple current is ignored. Furthermore, for bipolar devices like switches, conduction voltage drop is not significantly affected by conduction current and can be considered constant [20]. However, this inverter topology employs switched capacitors, thus, charging current has a very vital role in power loss of converter and will be discussed in this subsection.

1) Conduction Loss in Power Switches

Conduction loss across eight power switches is expressed as in (23).

\[
P_{\text{cond}} = \frac{1}{T} \int_0^T [V_{BI} d(t) i_O(t)] dt
\]

where $V_{BI}$ is voltage stress across an individual switch; $d(t)$ is the duty ratio for which switch is ON; $i_O(t) = I_m \sin(\omega t)$ is the load current. Voltage and current stress across each switch is mentioned in previous subsection. Considering 50% duty ratio, conduction loss across individual switches be expressed as in (24) to (26).

\[
\begin{align*}
    P_{S1,\text{cond}} &= \frac{i_{S1,max} V_{DC}}{\pi} \\
    P_{S3,\text{cond}} &= P_{S4,\text{cond}} = P_{S8,\text{cond}} = \frac{I_m V_{DC}}{\pi} \\
    P_{S2,\text{cond}} &= P_{S5,\text{cond}} = P_{S6,\text{cond}} = P_{S7,\text{cond}} = \frac{I_m 2 V_{DC}}{\pi}
\end{align*}
\]

As mentioned in the switching states, capacitors $C_1$, and $C_2$ are utilized during negative level generation. It is seen that $C_2$, discharges for complete negative levels. Thus, there is an additional charging current which is drawn from source, and stress on switch $S_1$ is highest as listed in (21). As listed in [20], average charge transported defines the power loss across capacitor and is expressed as in (27).

\[
P_c = \frac{V_{DC} \int_0^T |i_O(t)| dt}{T}
\]
2) **Switching Loss in Power Switches**

Parasitic in switches are neglected. Switching loss is the function of switching frequency which depends on carrier frequency and operates at fundamental frequency.

\[
P_{Sw} = \left(\frac{E_{on} + E_{off}}{\pi}\right) f_{Sw} \left(\frac{i_O}{i_{nom}}\right) \left(\frac{V_{BV}}{V_{nom}}\right) \tag{28}
\]

where \(i_O\) is peak current across the switch; \(i_{nom}\) is dynamic line current; \(V_{BV}\) is voltage stress across the switch; \(V_{nom}\) is dynamic voltage curve.

3) **Capacitor Ripple Loss**

The switched capacitors (SC) are charged in parallel and discharged in series to achieve voltage boost. The proposed common ground SCMLI are charged with under-damped RLC parameters as demonstrated in [31]. The voltage fluctuation during charging and discharging causes a power loss.

\[
P_{Loss(Ch)} = \sum_{j=1}^{m} \frac{C_j f_{Sw} \Delta V C_j^2}{\rho_j} \propto I_O R_{Ch} T_f T_{Ch} \tag{29}
\]

where \(C_j\) is the switched SC under loss test; \(R_{ch}\) is the ESR of capacitors in the charging path; \(\Delta V C_j\) is the voltage ripple across the switched capacitors; \(\psi\) is the RC time constant across the SC. When the charging is high for SC \(\rho \approx 1\).

\(T_f T_{Ch}\) is the ratio of fundamental output to charging period of switched capacitors.

Power loss across each component is shown in Fig. 10 using a PLECS simulation for a 1 kW system. It is observed that switches \(S_3, S_4, S_5,\) and \(S_6\) have higher conduction loss than other switches. However, the majority of loss occurs across SCs \(C_1\) and \(C_2\) due to charging and discharging. The small inductor \(L_r\) also contributes significantly in the loss of proposed inverter.

![Component Level Loss Distribution for 1kW Inverter](image)

**V. EXPERIMENTAL VALIDATION**

An experimental prototype for the proposed inverter is shown in Fig. 11(a). The characteristics of PV are implemented using a programmable DC supply to develop a 1 kW prototype at unity power factor. A polypropylene film type

![Experimental Validation](image)

(a) Experimental setup. (b) Inverter voltage, grid voltage and grid current during active power injection. (c) Capacitor voltage and current profile during active power injection. (d) THD of grid voltage. (e) THD of grid current.
capacitor DCL-41, 1700 µF, 600 V is used as DC link capacitor. The power circuit is comprised of two different variants of power switches from Infenion Technologies of rating 650 V, 40 A namely IGW40N65F5, an IGBT without reverse conducting characteristics and IKW40N65F5, an IGBT with reverse conducting behaviour. These IGBTs are driven by HPCL A-3120 gate drivers using Texas Instruments TMS320F28379D controllers. The waveform is captured on Keysight MS-X-2024A and THD is captured on a FLUKE 434 SERIES II energy analyzer. Aluminium electrolytics from ALCON, PG-6DI of 1000 µF and 1700 µF, 250 V are used. Capacitor charging current for capacitors $C_1$ and $C_2$ is limited using a quasi soft charging of capacitors provided by small inductors connected parallel with source and capacitors. The inductor in the circuit initially behaves as open circuit and does not allow sudden changes in current and limiting the source current up to two to three times that of load current. The other parameters for the experiment is listed in Table II.

As per application, a grid-connected PV inverter must process both active and reactive power. For this purpose, a current control mechanism is adopted using a PI controller in DQ reference frame. Fig. 11(b) shows operation of a grid connected inverter under unity power factor as the output current and voltage are in same phase. During this instance, peak-to-peak current is nearly 7 A and peak voltage varies upto 325 V from reference. Inverter voltage $V_{\text{inv}}$ is equal to 400 V, voltage boost is achieved by the capacitors. It is noted the proposed circuit has leakage current of nearly 200 mA. Fig. 11(c) shows capacitor voltage and current profile. Capacitor voltage is nearly equal to input source during steady-state condition, while the charging current of capacitors, $C_1$, and $C_2$ is nearly 10 A and 20 A, respectively. Fig. 11(d) and (e) shows the voltage and current THD which is found to be 4.5% and 2.5% respectively.

Figure 12(a) shows inverter output voltage remains the same 400 V while current lags the voltage by an angle of 60°.
The leakage current here also is 20 mA. Fig. 12(b) shows capacitor voltage is stiff during steady state, while the charging current for capacitor is higher for reactive power demand, in comparison to active power demand. Similarly, in Fig. 13(a) current leads the voltage by an angle of $30^\circ$.

Figure 14(a) shows the performance of the converter when the reference current is changed. This validates that the proposed PV inverter allows changes in current as per grid requirements. Correspondingly, variation of the capacitor charging current is also shown in Fig. 14(b). At last the blocking voltage across the switches $S_1$, to $S_4$ and $S_5$ to $S_8$ is shown in Fig. 15(a) and (b) respectively. It is observed that switches $S_2$, $S_5$, $S_6$, and $S_7$ have blocking voltage twice the input source, while other switches have blocking voltage equal to the input source.

VI. COMPARATIVE ASSESSMENT

A precise comparison among different parameters that quantifies the components used in the inverter design is exemplified in Table III. Other than this, few parameters like component size, operation of semiconductor devices at different frequencies characterize the power density and efficiency of the inverter. It is observed the number of power switches and their gate drivers is an important parameter that determines the cost of inverter. The proposed topology uses equal or a greater number of switches that other topologies. However, diode, an uncontrolled device that is characterized as cheaper in comparison with power switches. But, encounters a relatively higher forward conduction loss, making the inverter less efficient. The proposed topology uses no diodes. Most topologies except [7], [8], [11], [12], [16], [24], [27] and [28] use no diodes in the proposed inverter power circuit. Diodes being less efficient is still used because it does not require any gate driver circuits which maintain high power density.

A PV inverter requires a proper DC link capacitor and a proper combination of either switched/flying/floating capacitors to generate voltage levels. The size of capacitor mainly depends on the operating frequency. The topologies incorporating flying/floating capacitors require a large capacitor, whereas in case of switched capacitors, the primary requirement is the ability to handle high current ripples. The size of capacitor is the primary concern for the power density of the inverter. The proposed topology uses a polypropylene film capacitor in DC link while aluminum electrolytic capacitors for the switched capacitors. Another key factor that deter the size of capacitor is the voltage stress across the capacitors. High voltage stress on the capacitor marks relatively larger capacitors. In the proposed topology, both switched capacitors have voltage stress equal to the input source. However, the magnitude of capacitance is different 1.0 mF and 1.7 mF, as the later one is connected near load terminals. The maximum number of capacitors in this topology is 2, which is relatively smaller than other topologies.

Fig. 14. Performance of inverter under change in load. (a) Performance of inverter when peak to peak grid current changes from 7 A to 9 A. (b) Capacitor voltage and current profile when peak to peak grid current changes from 7 A to 9 A.

Fig. 15. Blocking voltages across switches in proposed inverter. (a) Voltage stress across switches $S_1$ to $S_4$. (b) Voltage stress across switches $S_5$ to $S_8$. 
of conducting switches and diodes is the responsible factor that determines the efficiency of PV inverter. The proposed topology uses, at most, five switches for achieving voltage level. Voltage stress across the power switches and diodes is a factor that helps in selecting components for the power circuit. The proposed topology has four power switches with voltage stress twice the input source. The power switches operating at high frequency, have high switching loss while power switches operating at low frequency have higher conduction loss. This factor also impacts the efficiency, and power density of the inverter. The proposed topology has four switches operating at high frequency, while the other four switches operate at low frequency. Maximum blocking voltage (MBV) across the power switches adheres to the rule for deciding the rating of inverters with considering a suitable margin of reliability indices. The MBV across four switches is found to be twice the input source.

Voltage gain is a feature which is achieved by energy storage elements like capacitors and/or inductors. It is observed that topologies with high voltage gain either have a large number of capacitors with less voltage stress or less capacitors with high voltage stress. Voltage gain also ensures requirements for power switches and diodes with higher voltage blocking capability. Despite few limitations in terms of cost, of power switches/diodes, and energy storage element, voltage gain helps in improving the overall power density and efficiency of the inverter. The proposed topology has twice the voltage gain achieved by using two switched capacitors. Transformer less PV inverters with common ground type (CGT) configuration is preferred as it facilitates no common mode voltage (CMV) and leakage current. The proposed topology exhibits a CGT configuration with twice voltage gain. Thus, the voltage gain and CGT configuration of PV inverter with no CMV and leakage current makes it feasible for grid connected applications. It is observed the inverter achieves peak efficiency of 96.2% at 500 W. Thus, The inverter has better efficiency, >96% for power range 100 W to 1 kW as shown in Fig. 16. The proposed inverter requires a 2 mH inductive filter, which is smaller in comparison with other SCMLI topologies. Thus, this validates

### Table III

Comparison with other Five Level PV Inverters

<table>
<thead>
<tr>
<th>Ref</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
<th>J</th>
<th>K</th>
<th>L</th>
<th>M</th>
<th>N</th>
<th>O</th>
<th>Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7]</td>
<td>8</td>
<td>0</td>
<td>4</td>
<td>V_{in}</td>
<td>1.5</td>
<td>4</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>6</td>
<td>V_{in}</td>
<td>1</td>
<td>No</td>
<td>5.3%</td>
<td>NR</td>
<td>NR</td>
</tr>
<tr>
<td>[8]</td>
<td>8</td>
<td>0</td>
<td>2</td>
<td>V_{in}</td>
<td>2.0</td>
<td>4</td>
<td>4</td>
<td>0</td>
<td>4</td>
<td>4</td>
<td>V_{in}</td>
<td>1</td>
<td>No</td>
<td>5.9%</td>
<td>95</td>
<td>1 mH, 2 ( \mu )F</td>
</tr>
<tr>
<td>[9]</td>
<td>6</td>
<td>3</td>
<td>2</td>
<td>V_{in}</td>
<td>0.3</td>
<td>5</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>V_{in}</td>
<td>2</td>
<td>No</td>
<td>4.8</td>
<td>NR</td>
<td>1 mH, 3 ( \mu )F</td>
</tr>
<tr>
<td>[10]</td>
<td>6</td>
<td>4</td>
<td>2</td>
<td>V_{in}</td>
<td>4.6</td>
<td>3</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>4</td>
<td>V_{in}</td>
<td>1</td>
<td>No</td>
<td>5.0</td>
<td>99.2</td>
<td>2 mH, 0.47 ( \mu )F</td>
</tr>
<tr>
<td>[11]</td>
<td>6</td>
<td>6</td>
<td>2</td>
<td>V_{in}</td>
<td>4.6</td>
<td>3</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>4</td>
<td>V_{in}</td>
<td>1</td>
<td>No</td>
<td>5.0</td>
<td>98.7</td>
<td>2 mH, 0.47 ( \mu )F</td>
</tr>
<tr>
<td>[12]</td>
<td>6</td>
<td>0</td>
<td>3</td>
<td>V_{in}</td>
<td>1.1, 1.1</td>
<td>3</td>
<td>4</td>
<td>0</td>
<td>2</td>
<td>4</td>
<td>V_{in}</td>
<td>2</td>
<td>No</td>
<td>NR</td>
<td>97.04</td>
<td>8 mH, 10 ( \mu )F</td>
</tr>
<tr>
<td>[13]</td>
<td>6</td>
<td>2</td>
<td>3</td>
<td>V_{in}</td>
<td>2.0, 0.3</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>4</td>
<td>V_{in}</td>
<td>1</td>
<td>No</td>
<td>1.57</td>
<td>NR</td>
<td>1.6 mH, 56 ( \mu )F</td>
</tr>
<tr>
<td>[14]</td>
<td>6</td>
<td>2</td>
<td>2</td>
<td>V_{in}</td>
<td>0.5</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>2</td>
<td>V_{in}</td>
<td>1</td>
<td>Yes</td>
<td>NR</td>
<td>97.8</td>
<td>1.5 mH, 0.5 mH, 1 ( \mu )F</td>
</tr>
<tr>
<td>[15]</td>
<td>9</td>
<td>1</td>
<td>2</td>
<td>V_{in}</td>
<td>1.5, 0.47</td>
<td>5</td>
<td>4</td>
<td>0</td>
<td>5</td>
<td>4</td>
<td>V_{in}</td>
<td>2</td>
<td>Yes</td>
<td>2.9</td>
<td>93.22</td>
<td>0.9 mH, 0.9 mH, 40 nF</td>
</tr>
<tr>
<td>[16]</td>
<td>7</td>
<td>0</td>
<td>2</td>
<td>V_{in}</td>
<td>2.2</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>4</td>
<td>V_{in}</td>
<td>1</td>
<td>Yes</td>
<td>2.3</td>
<td>97.04</td>
<td>3 mH, 6 ( \mu )F</td>
</tr>
<tr>
<td>[17]</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>V_{in}</td>
<td>2.2, 1.0</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>2</td>
<td>V_{in}</td>
<td>1</td>
<td>Yes</td>
<td>NR</td>
<td>96.2</td>
<td>NR</td>
</tr>
<tr>
<td>[18]</td>
<td>6</td>
<td>2</td>
<td>3</td>
<td>V_{in}</td>
<td>0.68, 1.2</td>
<td>5</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>V_{in}</td>
<td>2</td>
<td>Yes</td>
<td>3.5</td>
<td>98.10</td>
<td>3 mH</td>
</tr>
<tr>
<td>[19]</td>
<td>8</td>
<td>1</td>
<td>2</td>
<td>V_{in}</td>
<td>NR</td>
<td>5</td>
<td>4</td>
<td>0</td>
<td>5</td>
<td>4</td>
<td>V_{in}</td>
<td>2</td>
<td>No</td>
<td>2.2</td>
<td>96.8</td>
<td>8 mH</td>
</tr>
<tr>
<td>[20]</td>
<td>6</td>
<td>1</td>
<td>3</td>
<td>V_{in}</td>
<td>0.5, 2.0</td>
<td>4</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>2</td>
<td>V_{in}</td>
<td>1</td>
<td>Yes</td>
<td>3.5</td>
<td>98.5</td>
<td>2 mH, 3 ( \mu )F</td>
</tr>
<tr>
<td>[21]</td>
<td>6</td>
<td>2</td>
<td>2</td>
<td>V_{in}</td>
<td>1.5</td>
<td>3</td>
<td>4</td>
<td>0</td>
<td>2</td>
<td>4</td>
<td>V_{in}</td>
<td>2</td>
<td>No</td>
<td>2.45</td>
<td>92.0</td>
<td>NR</td>
</tr>
<tr>
<td>[22]</td>
<td>7</td>
<td>2</td>
<td>3</td>
<td>V_{in}</td>
<td>0.47, 1.0</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>V_{in}</td>
<td>2</td>
<td>Yes</td>
<td>1.63</td>
<td>98.1</td>
<td>2.3 mH</td>
</tr>
<tr>
<td>[23]</td>
<td>6</td>
<td>2</td>
<td>2</td>
<td>V_{in}</td>
<td>0.47</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>2</td>
<td>V_{in}</td>
<td>1</td>
<td>No</td>
<td>1.8</td>
<td>97.0</td>
<td>0.3 mH, 22 ( \mu )F</td>
</tr>
<tr>
<td>[24]</td>
<td>7</td>
<td>0</td>
<td>3</td>
<td>V_{in}</td>
<td>1.0, 1.0</td>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>V_{in}</td>
<td>1</td>
<td>Yes</td>
<td>3.8</td>
<td>97.10</td>
<td>NR</td>
</tr>
<tr>
<td>[25]</td>
<td>6</td>
<td>2</td>
<td>2</td>
<td>V_{in}</td>
<td>0.47, 1.0</td>
<td>4</td>
<td>3</td>
<td>1</td>
<td>4</td>
<td>2</td>
<td>V_{in}</td>
<td>2</td>
<td>Yes</td>
<td>2.0</td>
<td>95.5</td>
<td>NR</td>
</tr>
<tr>
<td>[26]</td>
<td>8</td>
<td>2</td>
<td>3</td>
<td>V_{in}</td>
<td>1.0, 1.0</td>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>V_{in}</td>
<td>1</td>
<td>No</td>
<td>NR</td>
<td>97.24</td>
<td>1.2 mH, 60 ( \mu )F</td>
</tr>
<tr>
<td>[27]</td>
<td>10</td>
<td>0</td>
<td>2</td>
<td>V_{in}</td>
<td>0.94, 0.47</td>
<td>6</td>
<td>2</td>
<td>0</td>
<td>6</td>
<td>4</td>
<td>V_{in}</td>
<td>2</td>
<td>Yes</td>
<td>2.2</td>
<td>98.20</td>
<td>2 mH, 100 ( \mu )F</td>
</tr>
<tr>
<td>[28]</td>
<td>9</td>
<td>0</td>
<td>3</td>
<td>V_{in}</td>
<td>NR</td>
<td>5</td>
<td>4</td>
<td>0</td>
<td>5</td>
<td>4</td>
<td>V_{in}</td>
<td>2</td>
<td>Yes</td>
<td>2.1</td>
<td>98.5</td>
<td>0.54 mH, 4 ( \mu )F</td>
</tr>
<tr>
<td>[29]</td>
<td>7</td>
<td>2</td>
<td>2</td>
<td>V_{in}</td>
<td>1.0, 1.0</td>
<td>6</td>
<td>4</td>
<td>0</td>
<td>3</td>
<td>4</td>
<td>V_{in}</td>
<td>2</td>
<td>No</td>
<td>NR</td>
<td>97.40</td>
<td>5 mH</td>
</tr>
<tr>
<td>[30]</td>
<td>8</td>
<td>2</td>
<td>4</td>
<td>V_{in}</td>
<td>1.0, 1.0</td>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>V_{in}</td>
<td>1</td>
<td>Yes</td>
<td>3.05</td>
<td>97.20</td>
<td>2 mH, 10 ( \mu )F</td>
</tr>
<tr>
<td>P</td>
<td>8</td>
<td>0</td>
<td>3</td>
<td>V_{in}</td>
<td>1.0, 1.7</td>
<td>5</td>
<td>4</td>
<td>0</td>
<td>4</td>
<td>4</td>
<td>V_{in}</td>
<td>2</td>
<td>Yes</td>
<td>2.5</td>
<td>96.20</td>
<td>2 mH</td>
</tr>
</tbody>
</table>

A - Number of switches; B - Number of Diodes; C - Number of Capacitors; D - Voltage Stress across Capacitors (in \( V_{in} \)); E - Magnitude of Capacitors (in nF); F - Maximum number of switches and diodes conducting; G - Number of switches with stress more than input source; H - Number of diodes with stress more than input source; I - Number of switches operating at high frequency; J - Number of switches operating at low frequency; K - Maximum Blocking Voltage across switch; L - Voltage Gain; M - Common Ground Configuration; N - THD (%) in grid current; O - Efficiency (%); P - Proposed inverter; NR - Not Reported

Fig. 16. Comparison of simulation and experimental efficiency.
safe and robust operation of inverter with inrush current with prescribed limits. Voltage and current THD is found to be 4.5% and 2.5% respectively, that obeys the IEEE-519 and VDE-0126-1-1 guidelines.

VII. CONCLUSION

This article presents a single-phase five-level transformerless inverter with reduced leakage current. The novelty of this inverter is the common ground structure for the PV input and the grid neutral terminal. Nevertheless, twice voltage boosting is achieved by capacitors that have potential equal to the input source. The quasi-soft charging mechanism of the capacitors ensures less inrush current across capacitors. Moreover, the inverter is capable of delivering both active and reactive power. Leakage current for the inverter is <5 mA as seen on 20 mA scale on oscilloscope. Efficiency for a 1 kW inverter is 96.20%. Experimental results and comparison satisfies the viability and feasibility of the proposed inverter.

REFERENCES


Vishal Anand (S’21) received the B. Tech degree in Electrical and Electronics Engineering from the College of Engineering, Bhubaneswar, India in 2015, and the M.E. degree in Power Electronics in 2018 from Birla Institute of Technology, Mesra, Ranchi, India. He is a research scholar in National Institute of Technology Raipur, India.

He is currently an Application Engineer in PWSIM Engineering Solutions, India. His research interest includes high frequency power conversion, power electronics control, multilevel inverter topologies, grid-connected inverters for renewable energy generation and wireless power transfer.

Varsha Singh (M’13–SM’20) received the Ph.D. degree from National Institute of Technology Raipur, India in 2018. She has more than 12 years of teaching experience with NIT Raipur where she is serving as an Assistant Professor with Electrical Engineering Department.

She has authored or coauthored 30 papers in journals and conferences. Her research interest includes application of soft computing techniques in power electronics, power converter design and multilevel converters. She is a frequent reviewers for the IEEE Journal of Selected Topics in Power Electronics, the IEEE Transactions on Power Electronics, and the IEEE Transactions on Industrial Electronics. Dr. Singh is a member of the IEEE Power Electronics Society and the IEEE Industrial Electronics Society.

Jagabar Sathik (M’15–SM’19) received the B.Eng. degree in Electronics and Communication Engineering from Madurai Kamaraj University, Madurai, India, in 2002, and the M.Eng. and Ph.D. degrees from the Faculty of Electrical Engineering, Anna University, Chennai, India, in 2004 and 2016, respectively. He is an Associate Professor with the Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Chennai.

He is currently a Postdoctoral Fellow with the Renewable Energy Laboratory, College of Engineering, Prince Sultan University, Riyadh, Saudi Arabia. He was a consultant of various power electronics companies for the design of power electronics converters. He has authored more than 60 articles publications in international refereed journals and conference proceedings. His current research interests include multilevel inverters, grid-connected inverters, and power electronics converters and its applications to renewable energy systems.

He received the certificate of recognition from IEEE Madras Section for paper published in the year of 2019-2021. He is serving as a Regular Reviewer for several journals, including the IEEE Transactions on Power Electronics, the IEEE Transactions on Industrial Electronics, the IEEE Journal of Emerging and Selected Topics in Power Electronics, and the IET Power Electronics.

Dhafer Almakhles (SM’20) received the B.E. degree in Electrical Engineering from the King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia, in 2006, and the master’s (Hons.) and Ph.D. degrees from The University of Auckland, New Zealand, in 2011 and 2016, respectively. Since 2016, he has been with Prince Sultan University, Saudi Arabia, where he is currently the Chairperson of the Communications and Networks Engineering Department and the Director of the Science and Technology Unit. He is also the Leader of the Renewable Energy Research Team and the Laboratory at Prince Sultan University.

He has authored more than 140 refereed journals in the area of power electronics and control system. He served as a reviewer for many journals including IEEE Transactions on Fuzzy Systems, Control of Network Systems, Industrial Electronics, Control Systems Technology and IEEE Control Systems Letters and International Journal of Control. His research interests include the hardware implementation of control theory, signal processing, networked control systems, nonlinear control design, unmanned aerial vehicle (UAV) and renewable energy.