An Adaptable Interface Circuit with Multi-Stage Energy Extraction for Low Power Piezoelectric Energy Harvesting MEMS

S. Chamanian, Student Member, IEEE, H. Uluşan, Student Member, IEEE, A. Koyuncuoğlu, A. Muhtaroğlu, Senior Member, IEEE, and H. Külah, Member, IEEE

Abstract—This paper presents a self-powered interface circuit to extract energy from ambient vibrations for powering up microelectronic devices. The circuit interfaces a piezoelectric energy harvesting MEMS device to scavenge acoustic energy. Synchronous electric charge extraction (SECE) technique is deployed through the implementation of a novel multi-stage energy extraction (MSEE) circuit in 180nm HV CMOS technology to harvest and store energy. The circuit is optimized to operate with minimum power losses when input power is limited, and adapts well to operating conditions with higher input power. The highly accurate peak detector was validated for a wide piezoelectric frequency range from 20 Hz to 4 kHz. A charging efficiency of about 84% has been achieved for 4.75 V open circuit piezoelectric voltage excited at 390 Hz input vibration under nominal input power range of 30-80 μW. Power optimizations enable the circuit to maintain a conversion efficiency of 47% at input power level as low as 3.12 μW. MSEE provides up to 15% efficiency improvement compared to traditional SECE, and maintains power efficiency as high as possible for a wide input power range.

Keywords—Self-powered, vibration, piezoelectric energy harvester, IC, MSEE, power efficiency.

I. INTRODUCTION

Piezoelectric energy harvesters (PEH) have recently attracted interest as a solution for self-powered microelectronic devices such as implantable micro-devices and wireless sensor networks (WSNs). Piezoelectric transducers provide higher power density than the electrostatic harvesters, and provide ease of integration, planarity and higher output voltage in comparison with electromagnetic counterparts [1]. PEHs can supply power from μW to mW using ambient vibrations. Besides, there has been tremendous development in microfabrication processes [2], [3] and power density of MEMS transducers [4]. The MEMS harvesters gain importance in volume and weight constrained applications such as bio-implantable devices [5], [6], and [7] where battery replacement is impractical and costly. For example, a MEMS piezoelectric harvester has been utilized to generate rms output power range up to 160 μW under different vibration levels [8].

PEHs supply AC power with significant output impedance; consequently, an interface circuit (IC) is required to efficiently extract and convert piezoelectric AC voltage to usable DC voltage. Two conventional rectifiers, full bridge rectifier and voltage doubler are the most common AC-DC converters, which have been demonstrated in several works [9], [10]. Passive and active rectifiers [11], [12] suffer from low extraction efficiency due to significant power losses during intermittent vibrations. The main reason for the low efficiency is that the rectifier has to charge and discharge the piezoelectric capacitor (Cp) of the piezoelectric harvester each cycle, which dissipates considerable power. A maximum power point sensing circuit [13] is utilized to match load impedance of the full bridge rectifier to the real part of the source impedance, which improves power efficiency. The piezoelectric open-circuit voltage (VOC) sensing method is implemented to fix output voltage of the full-bridge at half of VOC. The circuit nevertheless wastes most of the generated charge at the piezoelectric capacitance. Furthermore, this method is only effective for periodic vibrations.

Beside standard rectification, switching approaches based on non-linear processing of the voltage across PEH are used to enhance the extracted power, including synchronized switching [13], [14], single supply pre-biasing [15], and synchronous electric charge extraction (SECE) [16], [17] techniques. Synchronized switch harvesting on inductor (SSHI) [18], [19] benefits from charge inversion on Cp through recycling inductor. In this way, opposite charge generation is initiated close to conduction threshold of the rectifier. In this method, the...
power improvement strongly depends on the output load. Pre-biasing and energy recycling methods boost extracted power through investing portion of the stored energy into the piezoelectric capacitor to step up electrostatic force of the piezoelectric actuator. Optimization of invested energy requires high battery voltage and cumbersome adjustments.

Operation principle, power gain and efficiency analysis of switching techniques are detailed in [20]. It is shown that the harvested power can be increased up to 400% through the SECE [21] scheme, wherein the generated charge at peak displacement is transferred to the output buffer through LC resonant circuits. SECE is an efficient approach among switching techniques for facilitating charge delivery and achieving load matching at the same time. The main challenge in this approach is extracting maximum power for a wide input power and frequency range. Energy extraction and transfer in several successive charge packages enables reduction in the size of off-chip electromagnetic components and increased power efficiency [22]. The SECE circuit implemented in [22] is efficient only for mechanical frequency range below 100Hz, and depends on digital inputs for establishing critical time constants associated with piezoelectric and output storage capacitances, to regulate extraction and transfer durations. High input voltage and low input frequency operation necessitates a large harvester, which is impractical for deployment in implantable micro-devices.

The aim of this work is to realize an autonomous harvesting circuit that is compatible with MEMS energy harvesters used to power-up biomedical devices. This paper presents a power optimized SECE interface circuit that improves the minimum required input power and frequency range of MEMS PEHs with low voltage output. In particular, an original multistage energy extraction technique has been implemented through a unique energy-based multistage generator circuit in an integrated SECE converter system to simultaneously achieve low cost and high power conversion efficiency. Interface circuit introduced briefly in [23], is optimized, prototyped and evaluated in this study. The principle of circuit operation, power optimization approach, and implementation details are presented in the following section. Section IV summarizes test setup and experimental results. Finally, the study is concluded in Section V.

II. INTERFACE CIRCUIT DESIGN

SECE is an effective topology to interface piezoelectric harvesters operating at low voltages. Low power and high mechanical frequency of MEMS PEH requires careful design of the AC/DC interface circuit to achieve high efficiency. In [22], a fly-back SECE uses multistage technique to handle highly charged PEH with a package inductor, but the high series resistance of the relatively large inductor constrains power conversion efficiency. The proposed MSEE on conventional SECE architecture allows shrinking the external inductor without affecting power conversion efficiency. The multistage extraction can efficiently transfer the harvested energy over a relatively low-profile inductor (100 µH-1 mH). In the previously reported multistage circuits, timing is calculated by multiplying digital inputs set by user and predefined coefficients, which requires measurements and hand-calculations. Compromises between mechanical frequency and power consumption cannot be avoided. Although the core configuration of the circuit in this paper is similar to SECE integrated circuits in [17], [24], our design is adaptable to minimize power losses with the help of the multistage technique that does not require explicit calculation of extraction time duration. The circuit enhancements, which include a high accuracy peak detector and ultra-low power control, play a significant role in extracting power more efficiently from MEMS PEH with few microwatts of capacity and high excitation frequency compared to previous approaches. Furthermore, implementation of the multistage generator with energy sensing capability eliminates efficiency and cost limitations arising from high mechanical frequency, additional digital inputs and timing problems.

A. Operation Principle

The proposed circuit comprises a control unit and three processing stages including a negative voltage converter (NVC), active extraction, and energy storage with start-up circuit as shown in Fig. 1. The positive voltage from NVC charges the storage capacitor, C储能, at wake-up, through a diode and a control switch. The startup circuit decouples the supply voltage of the control unit (VDD) and storage voltage (V储能) as long as V储能 < V trig, and switches the storage voltage to power up the active components in the control unit (VDD=V储能) when V储能 > V trig. The power extraction stage is designed based on the synchronous electric charge extraction (SECE) technique. Active power extraction is realized through three phases managed by switch control circuitry as shown in Fig. 2. In the first phase, all switches in Fig. 1 are turned OFF to bias the PEH at open circuit condition until its output peaks. After peak detection, energy stored on the PEH capacitor is transferred to the inductor through C储能-L resonant circuit by turning S1 and S1 ON. The third phase is entered when PEH voltage reaches zero. At this point, S1 and S1 are turned OFF, S2 and S2 switches are turned ON, and the stored energy on the inductor is transferred to the storage capacitor, C储能. Charging of the capacitor continues until the inductor current reaches zero.

Fig. 1. System architecture of the integrated PEH interface circuit; modified version of [23].
is measured through a current sensing and energy converting circuit to determine the magnitude of the energy packet. Eventually, the current magnitude in each stage is reduced by √(1/N). Therefore, the conduction loss of the power switches and the inductor is decreased in proportion to the current reduction passed through inductor-switch network. In addition, this approach allows utilizing a low volume inductor with small series resistance, which is desired for reduced system footprint and cost. Power analysis is discussed in next part.

B. Power Optimization

The energy generated on piezoelectric capacitor, \( C_p \), as the beam vibrates, due to mechanical excitation of the harvester, is obtained as:

\[
E_{\text{Coupled}} = \frac{1}{2} C_p V_{OC}^2 .
\]

The coupled energy is extracted through discharging the piezoelectric capacitor and transferred to output buffer capacitance. The pure energy harvested, \( E_{\text{Harv}} \), are calculated as:

\[
E_{\text{Harv}} = E_{\text{Coupled}} - E_{\text{loss}}
\]

There are four sources of power dissipation in the switching circuit: Resistive conduction losses in the inductors and MOSFET switches (\( P_{\text{cond}} \)); charge redistribution losses at MOSFET parasitic capacitances during phase changes (\( P_{\text{cond}} \)); capacitive switching losses at the gates of power switches (\( P_{\text{sw}} \)), and leakage current associated with any MOSFET in OFF state (\( P_{\text{leak}} \)).

\[
P_{\text{loss}} = P_{\text{cond}} + P_{\text{sw}} + P_{\text{driv}} + P_{\text{leak}}
\]

With regard to circuit configuration and stage number, four dynamic power losses are expressed as follow:

\[
P_{\text{cond}} = (R_{\text{ind}} + R_{\text{sw1,sw2}}) \times \sum_n \frac{1}{\omega_p} \int_0^{T_{p,n}} i_{p,n}^2 dt + (R_{\text{ind}} + R_{\text{sw2,sw4}}) \times \sum_n \frac{1}{\omega_p} \int_0^{T_s,n} i_{s,n}^2 dt
\]

\[
P_{\text{driv}} = (Q_{gs,sw2,sw4,sw1,sw2}) f_{\text{exc}} + Q_{gs,sw1,sw2} f_{\text{exc}}
\]

\[
P_{\text{sw}} = C_{ds,sw2} V_{gs,n}^2 f_{\text{exc}} + C_{ds,sw3} V_{stor}^2 f_{\text{exc}}
\]

\[
P_{\text{leak}} = i_{\text{leak}} w_{\text{sw1,sw2}} V_{OC} + i_{\text{leak}} w_{\text{sw4,sw2}} V_{stor}
\]

During \( T_{s,n} \), the energy of the inductor is transferred to the buffer capacitor. This period can be obtained by solving LC resonant circuit with initial the capacitor and the inductor values. \( T_{s,n} \) is approximated as follows by assuming \( C_{\text{stor}} >> C_p \):

\[
T_{s,n} = \frac{\text{peak}_{,n}}{V_{\text{stor}}}
\]

In our proposed approach, energy packet size is determined with energy sensing method that does not require explicit calculation of extraction time duration. The generated energy in the first phase is sensed through a downsampling circuit, and is divided by \( N \) with the help of a capacitor network. It is then compared with the energy extracted in the second phase, which
length at zero bias. PB is drain bottom junction built-in voltage, \( PB_{sb} \) is drain sidewall junction built-in voltage, \( M_s \) is drain bottom junction grating coefficient, \( L_D \) is lateral diffusion length, and \( M_{sb} \) is drain sidewall junction grating coefficient. The above equations indicate that on-resistance and gate-charge of the switch \( S_2 \) vary with input piezoelectric voltage, while the same parameters are sensitive to the storage voltage for the other switches. The substitution of equations (12-14) into equations (8-11) shows that all four power-dissipation sources depend on power switch size, input piezoelectric voltage, and storage voltage \( (V_{stor}) \).

In implemented technology, 180nm HV CMOS, N-MOSFET and P-MOSFET power switches tolerate up to 12 V and 17 V at their terminals, respectively. The MSEE chip requires minimum supply voltage of 1.1 V to drive power switches and achieve proper operation of the MSEE. The maximum storage voltage is limited to 3.3 V, which is defined by 3.3 V MOSFETs utilized in control unit. After thorough investigation of losses, within 180nm HV CMOS, the total power loss is obtained as a function of N-MOSFET power switch sizes and corresponding aspect ratio of the P-MOSFET switches, as shown in Fig. 3. Since efficient extraction in low-power outputs of the MEMS PEHs are intended, minimum input voltage is set to 1.5 V and storage voltage is set to maximum allowable value, \( V_{stor} = 3.3 \) V. The power switch \( (S_1-S_4) \) sizes have been optimized, as \( W = 4 \) mm for a minimum power loss of 0.86 μW at just above the lowest allowable PEH voltage, \( V_{oc} = 1.5 \) V. This optimization improves power efficiency for the low input power scenario, while maintaining the control of the higher input power levels through MSEE.

Piezoelectric voltage to current, \( I_s \), where Node \( V_X \) is reset to the ground, previously. Negative feed-back action on \( M_{S0} \) and \( M_{P0} \) forces Node \( V_X \) to be charged just around the threshold voltage of the \( M_{S0} \) MOSFET. As PEH voltage peaks, \( I_s \) crosses zero, and voltage drop of the node \( V_X \) over \( M_{P0} \) turns \( M_{S0} \) OFF. As \( M_{S0} \) turns OFF, the node \( V_Y \) is pulled up by mirroring reference current through the node. Common source amplifier and digital inverters in the output stage deliver a high edge rate. Fig. 5 illustrates the operation of the peak detector through the voltage and current simulation waveforms. The accuracy of the peak detector is critical in viewpoint of power conversion efficiency. The previous current-mode peak detectors suffer from offsets due to reference-current level and device mismatch of the current comparator. The proposed circuit resolves above issues using an active switch \( (M_{S0}) \) instead of the current comparator. With increasing piezoelectric voltage, switch \( M_{S0} \) turns ON, and consequently \( M_{P0} \) starts conducting to regulate voltage at node \( V_X \) due to feedback between \( V_X \) and \( V_Y \). When \( I_s \) reaches zero, \( M_{P0} \) dissipates accumulated charge at node \( V_X \) turning off \( M_{S0} \). The applied method alleviates the sensitivity of the circuit to process variation and mismatches in MOSFETs. The proposed circuit pulls up node \( V_X \) through \( I_{null-up} \) without contending with peak \( I_s \), which results in significant improvement in response time. The upper limit of the input frequency determines the reference current value, while the minimum detectable amplitude determines the value of the series capacitor, \( C_{PK} \). \( D_{out} \) goes high to connect node \( V_X \) to ground as the extraction phase is entered. This suppresses \( I_s \) oscillation that is caused by the resonant switching in the second phase.

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**Fig. 3.** Total power losses vs. power switch sizes @ \( V_{oc} = 1.5 \) V.

**Fig. 4.** Schematic of the implemented Peak Detector.

**Fig. 5.** Voltage and current waveforms of the peak detector.
2) Multi-stage generator circuit: The multi-stage generator, depicted in Fig. 6(a), relies on energy drain without any calibration requirement. This circuit comprises of two energy sensing circuits and a comparator. The energy generated on piezoelectric capacitor is sensed by the energy sensing circuit called energy stored in piezoelectric (ESP) in the first phase. The ESP utilizes a capacitor to convert piezoelectric voltage to current with the help of Flipped Voltage Follower (FVF). The FVF provides almost constant voltage on negative terminal of the capacitor through feedback connection of two cascaded transistors. Through two current mirrors, the sensed voltage is regenerated over sensing capacitors. The number of extraction steps (N) determines the capacitors connected in parallel to divide sensed energy by N. Four equally sized capacitors are controlled to obtain desired value, 

\[ C_{\text{op}} = C_{\text{S}} \times \frac{M_1 + M_2 + M_3 + M_4}{4} \]

with minimum voltage downscaling of \( C_{\text{S}}/C_{\text{op}} \). When PEH voltage peaks, ESP circuit switches to hold state by lowering enable signal in order to save the measured voltage. During the second phase, energy transferred to the inductor is sensed through energy transferred on inductor (ETI) circuit based on the same principle, and the same size of the capacitances, \( C_{\text{SP}} = C_{\text{ETI}} \) and \( C_{\text{DP}} = C_{\text{ETI}} \). Finally, sensed energy with ETI through \( V_{\text{ETI}} \) is compared with N-divider of generated energy, determined through \( V_{\text{ESP}} \), using hysteresis comparator to determine energy packet size transferred to the inductor. This guarantees constant energy extraction at each stage as shown in Fig. 6(b). Multi-stage output signal initiates the third phase to harvest the generated energy, and \( C_{\text{DP}} \) is reset for next extraction. The operation principle and related signals are illustrated in Fig. 6(b). The number of extraction stages is controlled through M[1-4], generated from 2 digital bits (labeled N in Fig. 1) and a decoder.

3) Charge depletion detector (CDD): Depletion of stored energy in the inductor to storage capacitance is controlled by a charge-depletion comparator as shown in Fig. 7, with a relatively high bandwidth. The comparator monitors the voltage across \( S_4 \) switch to detect the end of inductor discharging. The CDD is only activated in the fourth phase to save power.

III. EXPERIMENTAL RESULTS

The interface circuit is designed in 180 nm HV CMOS technology from X-FAB company. The interface circuit is implemented in an active area of 2 mm² within 1.5 mm×1.5 mm die. The setup for experimental measurements is shown in Fig. 8 with micrograph of the chip. A custom MEMs piezoelectric harvester [25], fabricated in METU_MEMS center, is mounted on holding board. The MEMS harvester with footprint of 9 mm×4 mm has a capacitor of 4 nF. The MEMS harvester is excited at its resonance frequency with a shaker table consisting of a control unit, an amplifier, a feedback accelerometer, and an interface computer.

Fig. 6. (a) Implemented Multi-stage generator: (b) Operation principle and related signals.

Fig. 7. Charge depletion detector.

Fig. 8. Test setup for experiments, based on an IC, test board, and MEMS piezoelectric energy harvester.

Fig. 9. Measured input and output waveforms of the peak detector for (a) 500 Hz, (b) 1 kHz, and (c) 4 KHz input frequencies.
The maximum operation frequency of the MSEE is determined by the peak detector. A delay in detecting peak instant may cause significant energy loss as the energy transfer is initiated at lower piezoelectric voltage. The accuracy of implemented peak detector has thus been experimentally evaluated as a function of the input frequency. Fig. 9 shows piezoelectric and peak detector output waveforms for three different excitation frequencies. The accuracy of the peak detector is obtained as $(|V_{\text{max}} - V_{\text{meas}}|)/V_{\text{max}}$, which has been illustrated in Fig. 10 up to 4,000 Hz, which is the maximum design frequency of the MSEE circuit. Peak point is detected with more than 98% accuracy for excitation frequency range of 20 to 4,000 Hz with $I_{\text{pull-up}}=30$ nA. High accuracy of the peak detector alleviates degradation of the power efficiency due to peak detection latency. The peak point can be detected with higher precision and operation frequency range can be extended by increasing the reference current.

The performance of the interface circuit has been measured using a MEMs piezoelectric harvester with $C_p=4$ nF attached to a shaker table. An inductor ($L=1$ mH/5.1 $\Omega$) is connected to the chip to charge a 1 $\mu$F storage capacitance in parallel with a variable load resistance. Minimum piezoelectric peak voltage of 700 mV is required for operating start-up of the circuit. Fig. 11 depicts operation of the circuit for an excitation frequency of 390 Hz with 17 $\mu$W input power, and 290 k$\Omega$ load resistance. The storage capacitance is initially charged through the start-up circuit. Then energy is extracted from PEH in three stages (N=3). The voltage waveform during charging of the storage capacitor in three stages is shown in Fig. 11. Fig. 12 illustrates measured piezoelectric voltage and inductor current waveforms when different number of stages are used in the circuit. The magnitude of the current passing through inductor and switches is divided by the square-root of the number of stages. Consequently, conduction power loss is decreased with the current reduction. As seen in Fig. 12, there is a harvesting time variation among different number of stages. This variation is partly related to the extraction time duration, $T_{\text{ex}}$, which depends on the number of stages as in equation (2). Another variation comes from the difference in storage voltage $V_{\text{stor}}$, which makes charge transfer duration, $T_{\text{ch}}=L\times I_{\text{peak}}/V_{\text{stor}}$, variant. Summing the extraction and transfer durations determines total time, which is distinct for different N.

Initially, the output power extracted within a single stage has been measured as a function of the storage voltage. Fig. 13 depicts the outcome for several values of $V_{oc}$. The dependence of the extracted output power on storage voltage is low, as expected, due to SECE technique. Ratio of $V_{oc}$ to $V_{stor}$ affects efficiency at lower storage voltage levels, as it takes longer to transfer energy to storage. Losses due to switching at higher storage voltage is more dominant for lower input power. For lower storage voltage as ratio of $V_{oc}$ over $V_{stor}$ increases, the output power dependence on the storage voltage, $V_{stor}$, is shown in Fig. 14 and Fig. 15 for $V_{oc}=1.5$ V and $V_{oc}=3.5$ V, respectively as the number of stages is varied. Single charge extraction shows the best performance for lower power limit, since excess switching dissipates dramatically higher power especially at higher output voltage. For higher input power, multi-stage extraction increases the output power due to the reduction of conduction losses on switches. Moreover, influence of the multi-stage extraction degrades with increase of the output voltage due to high switching loss and increase of quiescent current.
The charging efficiency, $\eta$, is obtained as ratio of the effective power delivered to the storage capacitance over the average input power. The effective power is calculated as energy increment on the storage capacitance over the charging time.

$$\eta = \frac{P_{\text{eff}}}{P_{\text{in}}} = \frac{\frac{1}{2}C_{\text{stor}}(V_{\text{final}}^2 - V_{\text{trig}}^2)}{\frac{1}{2}fV_{\text{OC}}P_{\text{piezo}}dt}$$

(15)

It is expected that multi-stage power extraction will improve power efficiency with increasing input power. The maximum power efficiency was measured at 84.4%. As it stands, the optimum stage number can be determined through input power or corresponding open circuit piezoelectric voltage. The stage number, N can be adjusted automatically through input power measurement at the end of the first phase of the extraction. The power efficiency can consequently be maximized for all input power levels in an autonomous manner.
Table I compares the experimental results of the implemented interface circuit with recent integrated SECE converters. The maximum operation frequency of the previous studies has been limited to achieve high conversion efficiency for harvester energy. This has resulted in the use of large piezoelectric harvesters with low resonance frequency, which is not practical in integrated and implantable electronic devices. Additional volume restriction follows from the size of the external inductor. Hehn [17] utilized 10 mH inductor with large package (630 mm$^3$) to constrain the oscillation current. Dini [24] utilized a 560 µH inductor in addition to 10 mH to remove residual charge effect. Gasnier [22] used two off-chip MOSFETs in addition to small sized inductor (125 mm$^3$), however high series resistances of the inductor (72 Ω) adversely affected the power conversion efficiency. Our system benefits from both wide frequency operation range that is capable of harvesting energy from MEMS piezoelectric harvesters, and small size inductor (66.8 mm$^3$). As a result of optimization, minimum dynamic power loss has reduced below 1 µW. The multi-stage extraction circuit has limited oscillation current, while improving the power efficiency to 84.4%.

IV. CONCLUSION

An autonomous CMOS interface circuit has been designed and fabricated for efficient utilization of PEH resources. An adaptable multi-stage energy extraction circuit has been proposed to enhance the efficiency of the circuit for wide range of inputs. 98% accuracy has been measured up to 4 kHz for peak detector circuit. The performance of the IC has been evaluated through MEMS piezoelectric harvester with 9mm$^2$×4mm footprint. The charging efficiency of the IC goes above 47% for an input power of 3.12 µW, while the maximum charging efficiency is recorded as 84.4% for an input power of 78 µW. The presented PEH interface IC delivers the means to supply power to microelectronic devices more efficiently, regardless of the variation in the available PEH energy.

ACKNOWLEDGMENT

This work is supported by ERC FLAMECONC project, funded by ERC Consolidator Grant 2015.

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