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FPGA-Based Space Vector PWM and Closed Loop Controllers Design for the Z Source Inverter

ALI RIZA YILMAZ AND BURCU ERKMEN
Department of Electronics and Communications Engineering, Yıldız Technical University, 34220 Istanbul, Turkey
Corresponding author: Burcu Erkmen (bkapan@yildiz.edu.tr)

ABSTRACT In this study, an iterative reduction based heuristic algorithm (IRHA) based closed loop control and space vector PWM (SVPWM) control of the Z-source inverter are implemented in hardware. The third harmonic addition method is used to realize the SVPWM structure in programmable embedded environment. The control parameters are optimally determined by IRHA to overcome the problem of instability. The controllers are implemented in single Field-Programmable Gate Array (FPGA) chip using hardware description language without help of any IP core units which increases speed, accuracy, compactness and cost efficiency. Furthermore, power consumption of the controllers is lower than a conventional ones which is prominent advantage of employing FPGAs. The effectiveness and accuracy of the control structure are verified by experimental results.

INDEX TERMS Z-source inverter, space vector PWM, PID, FPGA, heuristic algorithm.

NOMENCLATURE

ZSI	Z source inverter.
$SVPWM$	Space vector PWM.
D	Shoot through duty ratio.
M	Modulation index.
B	Boosting factor.
C	Capacitor of Z-source network.
L	Inductor of Z-source network.
U	Output of the controller.
k	Voltage space vector number$(1, 2, \cdots, 6)$.
V_{DC}	ZSI dc line voltage.
V_C	ZSI impedance network capacitor voltage.
V_g	ZSI dc input voltage.
V_{ref}	ZSI ac output voltage peak value (reference).
V_{out}	ZSI ac output voltage.
V_{DEA}	Number of the Variable (Gene) in DEA$(1, 2, \cdots, j)$
$x_j^{(u)}$	Upper limit values of variables.
$x_j^{(l)}$	lower limit values of variables.
NP	Population Size (number of the chromosomes) in DEA $NP \geq 4(1, 2, \cdots, i)$.
F	Mutation Control Parameter in DEA [0, 2].
CR	Crossover Control Parameter in DEA [0, 1].
G	Maximum Generation in DEA $(1, 2, \cdots, G_{max})$.
ΔI	Current ripple.
ΔV_C	Voltage ripple.
T_0	Shoot-through switching period.
T_1	Non shoot-through switching period.

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I. INTRODUCTION

In the past years, DC motors have been used extensively for industrial purposes [1]. Although the DC motor provides high starting torque, it has some disadvantages that require high maintenance and are not suitable for hazardous environments [2]. Recently, however, induction has replaced the labor force in the industry instead of the dc motor due to its robustness, less maintenance requirements, high efficiency, and low cost [3] , [4]. The efficiency of the induction motors is highly dependent on the drive circuit, the PWM strategy and the closed loop control structure. Motor drive circuits are one of the most important areas of power electronics. Conventional motor drive circuits are based on a Voltage Source Converter (VSC) and consist of a diode rectifier front end, a dc link capacitor, a dc inductor and inverter bridge. However, the performance and reliability of this structure is compromised due to faults in VSC structure, dead time and general mode voltage [5]–[7].

Z-Source inverter(ZSI) is one of the power converter topologies suitable for motor drive applications as in many power electronics fields [8]. The most important advantage

that distinguishes ZSI from other converter models is that it has the ability to buck and boost single-stage conversion with a shoot-through (ST) state added to the zero state. There are basically three different ST control structures in the literature, such as Simple Boost Control (SBC), Maximum Constant Boost Control (MCBC), and Modified Space Vector Modulation Boost Control (MSVMBC) [9], [10]. It is also possible to classify closed loop control structures as direct DC link control and indirect DC link control [11]. The peak dc-link voltage is kept constant in the direct measurement technique; However, the control scheme becomes more complex with additional circuits. To overcome this limitation, the highest dc-link voltage is estimated using Indirect DC-link control [11]. In Indirect DC-link control, there are two different methods based on measuring capacitor voltage V_C in the impedance source network and measuring V_C capacitor voltage and input voltage V_g to estimate peak dc-link voltage [12]. However, in this case the speed of the control unit becomes very important as the DC link voltage is controlled indirectly. Because the sudden changes in the input can lead to high voltage at the output, increasing the voltage stress on the switch and causing harmonic distortion [13], [14]. FPGA provides very low latency for input-output process. Owing to this reason, FPGA based palatforms have been broadly used for accelerating many systems. The unwanted voltage and current fluctuations that can be seen in the output can be minimized by reducing the delay between the output and the controller by using FPGA [15]. Apart from PWM and closed loop control, the determination of the circuit parameters of the ZSI is very important for the reliability of the drive circuit. In this case, the power consumption and harmonic distortion of the circuit are reduced by optimization studies performed with the help of heuristic algorithms [16], [17].

PID control and PWM control are conventionally implemented in general-purpose microprocessor systems. FPGA provides many advantages over the conventional approaches. In comparison with conventional PID realization, high speed controllers with low power consumption are obtained using FPGA. Furthermore, complex functionality is realized by executing concurrent operations in FPGA [18], [19]. Building SVPWM in FPGAs creates an opportunity to recompute the space vector timers multiple times during one switching period [20].

In this study, PWM control and indirect DC-link control structure is realized on a single FPGA based platform considering speed factor. In the PWM control structure, the Modified SVPWM structure is implemented on the FPGA hardware with the help of third harmonic injection method. PID structure used in closed loop is realized by optimization of control coefficients by IRHA optimization method. In addition, circuit parameters were determined by differential evolution algorithm, which is one of the genetic based optimization algorithms, and the results were determined by the deterministic method. The reliable and robust our proposed control strategy [21] has been adopted on hardware.

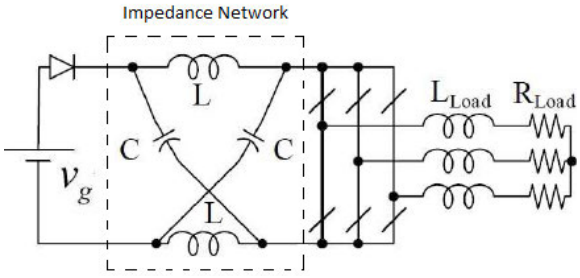

FIGURE 1. Z source inverter.

In closed-loop control, the importance of the speed factor was confirmed by reducing overshoot to about 4%. Finally, the experimental results are presented to the corroborate FPGA based control strategy of ZSI.

The remainder of this paper is organized as follows. z-source inverter design, control, dynamic behaviour analysis and design parameters are presented in Section II. It is followed by design of control parameters in Section III. In Section IV hardware implementation of PWM and Closed Loop Control are presented. In Section V, simulation and experimental verifications are conducted. Finally, Section VI concludes the paper.

II. Z-SOURCE INVERTER DESIGN

ZSI has a unique impedance network structure, as shown in Figure 1, which consists of two ''X-shape'' capacitors and two inductors.

As it is known, conventional VSIs have 8 different switching states. Unlike traditional VSIs, however, the ZSI has a total of 9 different switching states with 6 active, 2 zero states and 1 shoot-through. The ST states occurs when the load terminals are shorted by both the upper and lower switches of any phase. Since ZSI uses the traditional 8 state, common PWM methods such as sine PWM and SVPWM can be used with small changes in the zero state. The ST state can only be placed in the zero states, the active states remain the same, and therefore the AC output voltage of the inverter is similar to a conventional inverter. This change in state of zero gives the ZSI a unique boost or buck feature, depending on the change in power from the DC source [8].

A. Z SOURCE INVERTER

Despite the simple structure of ZSI, the correct modulation of the transducer is important for the converter dynamics in all operating modes. Depending on the switching conditions, we can distinguish ZSI in three different states described below;

Active states: The state in which the inverter bridge operates in any of 6 active states. In this state, the DC line voltage is seen on the impedance network, the capacity is charged and energy is transferred to the load via inductors.

Zero states: The state in which the inverter bridge operates in any of the two zero states. The DC source voltage is seen

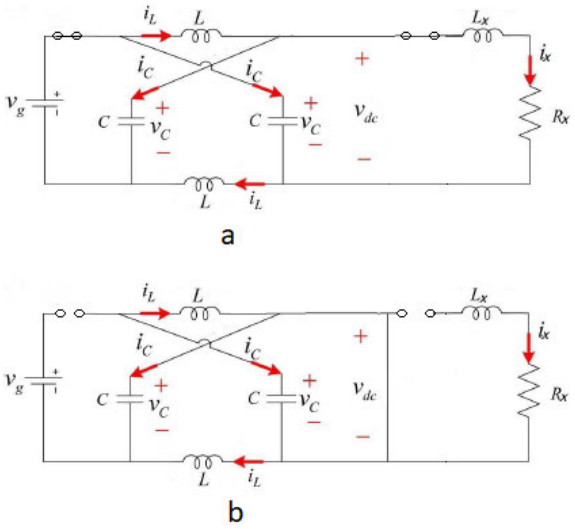

FIGURE 2. ZSI equivalent circuit in (a) nonshoot through state, (b) shoot-through state.

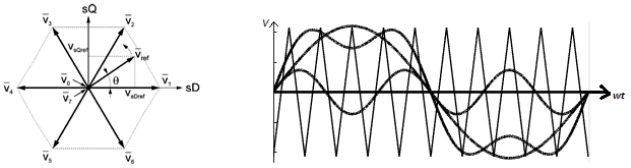

FIGURE 3. For three-phase ZSI a. Basic space vectors and sectors b. maximum boost control with third harmonic.

on the inductor and capacitor but there is no transmission to the load.

Shoot-through state: During this mode, no voltage is visible throughout the load as in the case of zero-state operation, but the DC voltage of the capacitor is increased to the required value according to the ST duty ratio. The ST range is added to the zero state in the specified range to boost the desired level. Figure 2 illustrates the operation states of the converter.

B. ZSI CONTROL : MAXIMUM BOOST CONTROL

Space vector PWM (SVPWM) techniques are widely used in industrial applications of the inverter, thanks to its advantages such as low current harmonics, and higher modulation index. SVPWM is suitable for controlling ZSI. However, unlike conventional SVPWM, the modified space vector PWM (MSVPWM) has an additional shoot-through time (T_0) to increase the dc link voltage of the inverter. Although this method is highly preferred, the hardware implementation of the MSVPWM method can be quite difficult, unlike the traditional SVPWM method. Therefore, it has been found that this method can be implemented with Maximum boost control with third harmonic injection especially in order to avoid the complexities and difficulties encountered in hardware [22].

Thanks to MSVPWM's unique switching arrangement, the capacitor voltage can be easily increased by shoot-through.

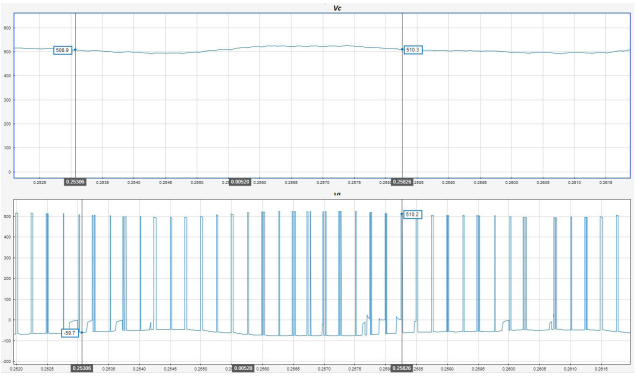

FIGURE 4. Simulation results of Z-source inverter: Enlarged view of capacitor voltage V_C and inverter voltage V_L.

The related equations are given as follow:

$$V_k = \left(\frac{2}{3}\right) V_g \tag{1}$$

$$V_{ref\,max} = V_{out_{peak}} = (\frac{\sqrt{3}}{2})V_k \tag{2}$$

$$V_{out_{peak}} = \frac{V_{dc_{peak}} m}{\sqrt{3}} \tag{3}$$

$$m = 1 - d \tag{4}$$

$$V_{dc_{peak}} = \frac{V_c}{1-d} \tag{5}$$

$$V_{out_{peak}} = \frac{V_c}{\sqrt{3}} \tag{6}$$

According to Equation 6, the MSVPWM offers the possibility to estimate the output voltage using only capacitor voltage feedback. Therefore, no output feedback is needed to control the ZSI output voltage. Thus, this method can be used, especially in grid-tied applications.

C. ZSI MODELLING: DYNAMIC BEHAVIOR ANALYSIS

It must be assumed that inductors L_1 and L_2 and capacitors C_1 and C_2 have the same value so;

$$\begin{aligned} V_{L1} &= V_{L2} = V_L \\ V_{C1} &= V_{C2} = V_C \end{aligned} \tag{7}$$

During shoot-through state;

$$\begin{aligned} V_L &= V_C \\ V_g &= 2V_C \\ V_{DC} &= 0(ST) \end{aligned} \tag{8}$$

During non-shoot-through state;

$$V_L \neq V_C, \quad V_g = V_{DC} = V_L + V_C \tag{9}$$

The output peak phase voltage from the inverter can be expressed as

$$\hat{V}_{AC} = \frac{M\hat{V}_{DC}}{2} = \frac{MBV_g}{2} \tag{10}$$

where B is the boosting factor

$$B = \left(\frac{T}{T_1 - T_0}\right) = \frac{T}{1 - (2T_0/T)} \geq 1 \tag{11}$$

$$T = T_0 + T_1 \tag{12}$$

In the ZSI modeling, the three states mentioned earlier are considered. In this model, inductance current ($i_L(t)$), capacitor voltage ($v_c(t)$) and load current ($i_x(t)$) are taken as state variables.

When three operating modes are considered, the state-space average model is obtained as in Equation13.

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_c \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & \frac{2d-1}{L} & 0 \\ \frac{1-2d}{C} & 0 & -\frac{m}{C} \\ 0 & \frac{2m}{L_x} & -\frac{R_x}{L_x} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \\ i_x \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{L}(1-d) \\ 0 \\ \frac{-V_{dc}}{L_x}m \end{bmatrix} \tag{13}$$

As shown in Equation 14, the steady-state equations of state variables can be derived from the state space model.

$$\begin{aligned} V_c &= \frac{1-D}{1-2D}V_g \\ I_L &= \frac{1-D}{1-2D}I_x \\ I_x &= \frac{V_c}{R_x} \end{aligned} \tag{14}$$

Small signal analysis was used to linearize the system around an equilibrium point. In this analysis, the general form of the variable is ($x(t) = X + \hat{x}(t)$), where X is the component at the equilibrium point, x is the variable in the state space model, $\hat{x}$ is the perturbation signal. Using these formulas for all variables, the state space model to be used for the dynamic model can be obtained as in Equation 15.

$$\begin{bmatrix} si_L \\ sv_c \\ si_x \end{bmatrix} = \begin{bmatrix} 0 & \frac{2d-1}{L} & 0 \\ \frac{1-2d}{C} & 0 & -\frac{m}{C} \\ 0 & \frac{2m}{L_x} & -\frac{R_x}{L_x} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \\ i_x \end{bmatrix} + \begin{bmatrix} \frac{1-D}{L} & \frac{2V_C - V_{in}}{L} & 0 \\ 0 & -\frac{2I_L}{C} & -\frac{I_x}{C} \\ -\frac{M}{L_x} & 0 & -\frac{2V_C - V_{in}}{L_x} \end{bmatrix} \tag{15}$$

State equations of small signal analysis of ZSI case are given in Equation 16.

$$s\hat{i}_L = \left(\frac{2D-1}{L}\right)\hat{v}_c + \left(\frac{2V_c - V_g}{L}\right)\hat{d}$$

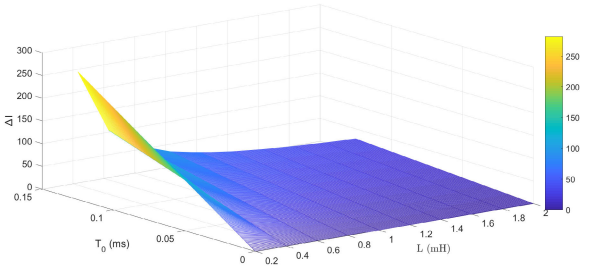

FIGURE 5. The effects of the variation of the inductance value and ST time to with respect to ΔI.

$$\begin{aligned} s\hat{v}_c &= \left(\frac{1-2D}{C}\right)\hat{i}_L - \frac{M}{C}\hat{i}_x - \frac{2I_L}{C}\hat{d} - \frac{I_x}{C}\hat{m} \\ s\hat{i}_x &= \frac{2M}{L_x}\hat{v}_c - \frac{R_x}{L_x}\hat{i}_x + \left(\frac{2V_c - V_g}{L_x}\right)\hat{m} \end{aligned} \tag{16}$$

It is possible to control the transfer function using small signal equations and steady state equations. Therefore transfer function of $\frac{\hat{v}_c(s)}{\hat{d}(s)}$ to control output has been given as a third-order transfer function in 18.

D. DESIGN PARAMETERS OF IMPEDANCE NETWORK

This section describes the parameter design of the Z source converter to drive the Induction motor.

1) DESIGN OF INDUCTANCES

In "Active state", the input voltage is visible through the capacitor and no voltage is visible through the inductor (only a pure DC current flows through the inductors). During ST state (boosting is involved), the inductor's task is to limit the current fluctuation during this boost mode. During ST, the inductor current increases linearly and the voltage on the inductor is the same as the voltage at the capacitor. In the traditional eight state, the inductor current decreases linearly, and the voltage on the inductor is the difference between the input voltage and the capacitor voltage.

Average current through the inductor;

$$\hat{I}_L = \frac{P}{V_g} \tag{17}$$

When there is a maximum ST, the maximum fluctuation appears on the inductor. For this reason, the maximum current fluctuation must be considered when selecting the inductor (18), as shown at the bottom of the next page.

Inductor maximum and minimum currents;

$$\begin{aligned} \hat{I}_L &= I_L + 30\% \\ \check{I}_L &= I_L - 30\% \end{aligned} \tag{19}$$

Calculation of inductor value;

$$L = \frac{V * T_0}{\Delta I} \tag{20}$$

The effects of changing the inductance value and ST ratio according to ΔI are shown in Figure 5.

As can be seen from Figure 5, as the inductance value increases, the current jumps are less visible during ST time.

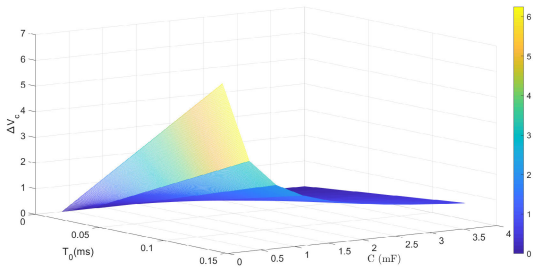

FIGURE 6. The effects of the variation of the capacitance value and ST time to with respect to ΔV_C.

TABLE 1. Parameters of ZSI.

Circuit Parameter	Value
L	$987.36\ \mu H$
C	$456.58\ \mu F$
Switching Frequency	$2\ kHz$
Shoot through time	$0.1\ ms$
Load Resistance	$12.5\ \Omega$
Load Inductance	$340\ \mu H$

However, since this directly affects the yield, an optimum design must be made.

2) DESIGN OF CAPACITORS

Limiting the capacitor voltage fluctuation (ΔV_C) to about 3% at maximum power (usually used in most applications for ZSI), the capacitor can be roughly calculated;

$$C = \frac{I_L * T_0}{\Delta V_C} \tag{21}$$

It is evident from the Figure 6, the selected capacity value directly affects the voltage jumps during shoot through times. For this reason, the selection of the circuit parameters must be optimally determined.

III. DESIGN OF CONTROL PARAMETERS

Although the PID control method is effective, the success of the controller depends on the control parameters to be used. In power electronics systems, controller design, i.e. optimization of control parameters, requires fine tuning process. Therefore, in this study, the previously proposed and analysed [21] IRHA optimization method is utilized. The genetically based optimization is described under modified differential evolution algorithm (MDEA).

In the process of designing closed-loop control parameters for ZSI, the stability of the system must be checked at every iteration. This control is based on DEA with IRHA model.

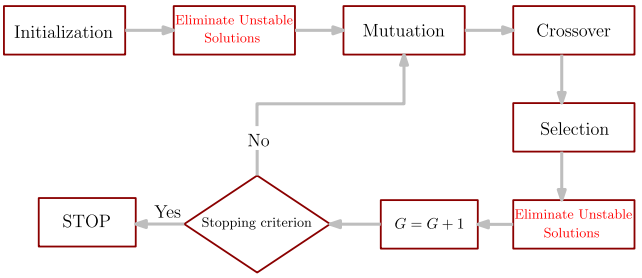

FIGURE 7. Flow chart of modified differential evolution algorithm.

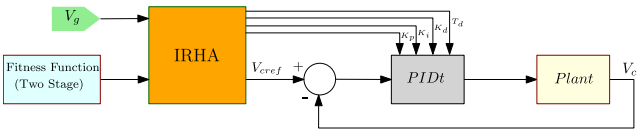

FIGURE 8. IRHA based control system [21].

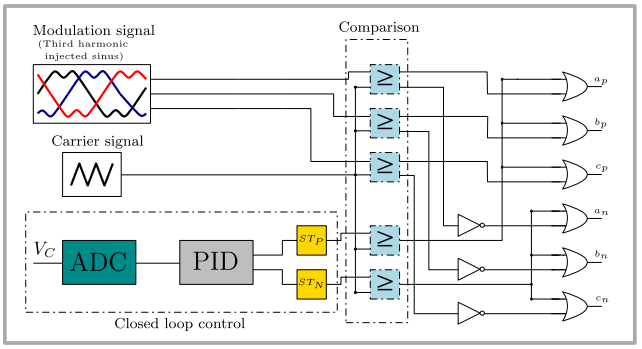

FIGURE 9. FPGA based control system design for both SVPWM and PID controls.

As seen in Figure 7, unlike the traditional DEA structure, during optimization, each set of iterations eliminates the unstable solution sets and optimizes this way.

As seen from the Figure 7, the traditional algorithm, DEA, is modified by elimination of unstable solution sets. Moreover, the parameters of DEA are $x_j^{(l)} = 0$,$x_j^{(u)} = 0.1$, $NP = 2000$, $V_{DEA} = 4$, $F = 0.8$, $CR = 0.5$, $G = 50$.

As a well-known method utilizing in optimizing PID parameters is minimizing integral mean square of the performance output which is generally taken as difference between reference input and measured output as shown in the Figure 8.

IV. HARDWARE IMPLEMENTATION

In the our previous study [21] algorithmic based infrastructures have been prepared for the realization of the system,

$$G_{\hat{v}_c\hat{d}}(s) = \frac{\hat{v}_c(s)}{\hat{d}(s)} = \frac{\left(-2I_L L_x L\right)s^2 + \left(2L_x V_c - L_x V_g - 4DL_x V_c + 2DL_x V_g - 2I_L L R_x\right)s}{CL_x Ls^3 + CLR_x s^2 + \left(4L_x D^2 - 4L_x D + 2LM^2 + L_x\right)s + \left(4R_x D^2 - 4R_x D + R_x\right)} + \frac{\left(2R_x V_c - R_x V_g - 4DR_x V_c + 2DR_x V_g\right)}{CL_x Ls^3 + CLR_x s^2 + \left(4L_x D^2 - 4L_x D + 2LM^2 + L_x\right)s + \left(4R_x D^2 - 4R_x D + R_x\right)} \tag{18}$$

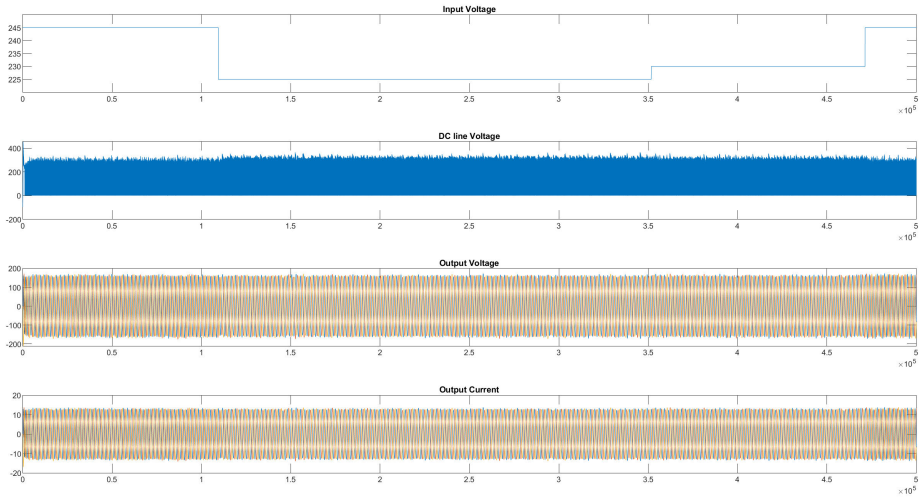

FIGURE 10. DC link voltage (V_{DC}), Output voltage (V_x) and Output current (I_x) response for different input voltages (V_g) in closed-loop system.

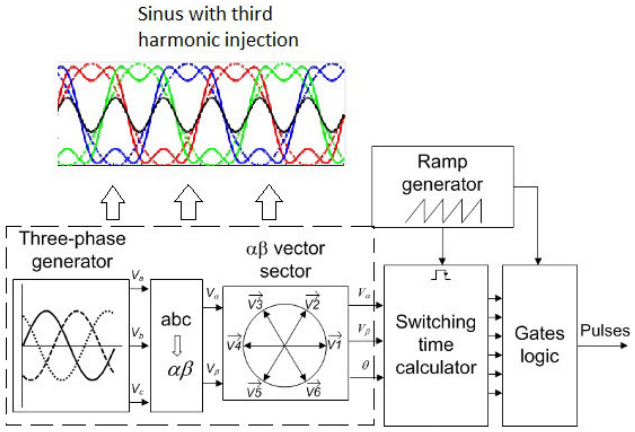

FIGURE 11. The space vector modulator block.

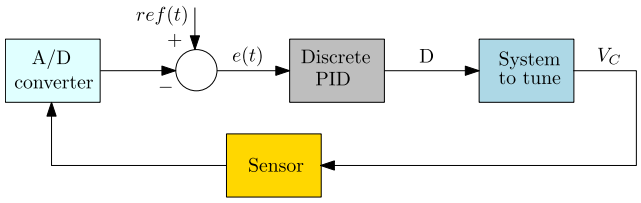

FIGURE 12. A PID based closed loop control system architecture.

which has proven robustness, in hardware. The implementation of PWM control and closed loop control methods in FPGA is explained extensively in this section. Figure 9 shows the hardware implemented structure.

A. PWM CONTROL IMPLEMENTATION

In order to generate an AC voltage of the required amplitude and frequency from a fixed DC source, the inverter switches are turn on and off using a modulating circuit. The efficiency of the inverters depends mainly on the PWM process to be used.

SVPWM is a widely used real-time modulation technique for voltage source inverters (VSI). Due to the complexity of this inverter model, it may be difficult to implement it on hardware. When examining the SVPWM generation steps, the physical limits in terms of maximum voltage output can be exceeded by the use of third harmonic injection as can be seen from Figure 11. Thus, we have avoided a lot of process complexities and the desired modulation has become possible in the FPGA environment.

B. CLOSED LOOP CONTROL IMPLEMENTATION

Speed is an important factor in closed-loop controls. Besides, having a programmable structure of the system directly affects the performance of the system.

In this study, FPGA based PID controller is used for closed loop control. The controller coefficients were designed offline using the IRHA optimization method and then integrated into the FPGA.

The digitized control law equation can be written as:

$$U_n = U_{n-1} + K_0 e_n + K_1 e_{n-1} + K_2 e_{n-2} \tag{22}$$

where;

$$\begin{aligned} K_0 &= K_p + K_i + K_d \\ K_1 &= 2(K_i + 2K_d) \\ K_2 &= K_d \end{aligned} \tag{23}$$

The control scheme is given in Figure 12.

V. RESULTS

In this section, simulation results and experimental results are discussed separately. With these results, it is aimed to prove the reliability of the proposed method.

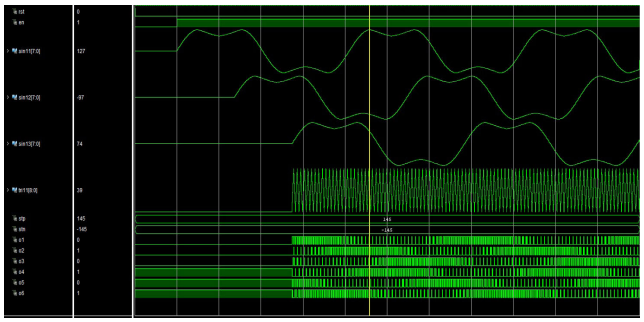

FIGURE 13. VHDL code simulation for MSVPWM control.

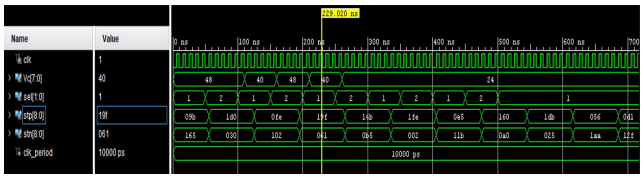

FIGURE 14. VHDL code simulation for PID control.

A. SIMULATION RESULTS

The complete design has been developed by using `Matlab/Simulink` for various operating conditions and then simulated and synthesized at `Vivado Design Suite /ISIM` for FPGA implementation. In this research, the switching frequency is fixed to 2 kHz for all criteria of the system.

Figure 10 shows the response of the output values as a result of changes in the input voltage. The operation of the proposed structure and its resistance to deterioration were demonstrated in the simulation environment.

Designed for the PWM control side, the model is realized by writing the VHDL (Very High Speed Integrated Circuits Hardware Description Language) code in `Vivado Design Suite` without help of any IP core to achieve a plain design. The study of the designed model was first observed in the simulation system with the help of ISIM (Figure 13). As shown in Figure 14, the PID control structure is written on the same FPGA platform as PWM control and its operation is verified by ISIM.

B. EXPERIMENTAL RESULTS

In order to demonstrate the effectiveness of the proposed control method on FPGA, the controller of the prototype Z source inverter was installed in the laboratory. DC voltmeter was used as A / D converter and the required PWM signal was generated using the capacitor voltage level. With the designed controller, the system has shown good reference tracking and distortion rejection features.

The programmable structure of the FPGA provides the flexibility to make the desired changes or adjustments to real-time control algorithms without the need for changes to hardware. The parameters of the set up are listed as follows: $L = 1\ mH$, $C = 1.32\ uF$, $L_x = 300\ mH$, $R_x = 200\Omega$.

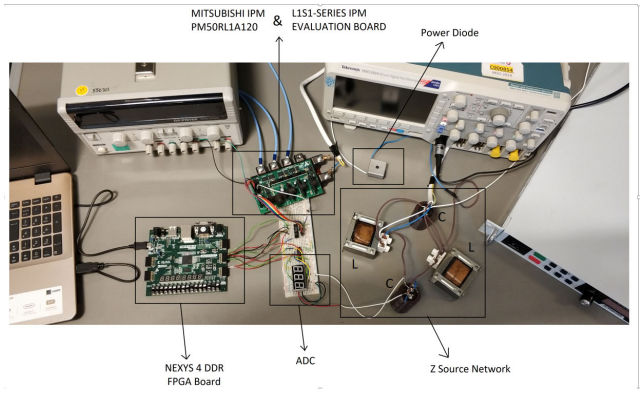

FIGURE 15. ZSI experimental setup.

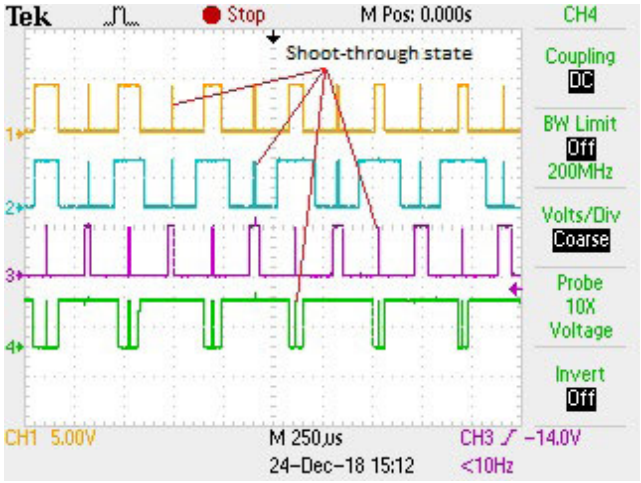

FIGURE 16. Experimental results of FPGA switching output.

Figure 16 shows the first 4 of the 6 switching signals obtained at the FPGA output. When the results were examined, it was seen that ST ratio was added to the period at the desired value appropriately. ST state is integrated into the system with maximum boost control method.

The three-phase voltage obtained at the IPM output with the applied switching signal is shown in Figure 17. At the output of the semiconductor switches triggered by SVPWM technique, the desired 3-phase signal is obtained.

In order to demonstrate the operation of the closed loop controller, the input voltage was increased by a certain ratio and the change of the DC bus voltage and phase-to-phase voltage was observed.

Figure 18 shows the experimental results against 20% increase in the input voltage. FPGA implementation in the closed loop has increased the feedback speed considerably, which means that the system has a good level of rejection.

Similarly, the effect of the 20% increase in the input voltage on the DC bus is shown in Figure 19.

When the Figure 20 is examined, it is seen that the 30% decrease in the input load corresponds to the DC line voltage.

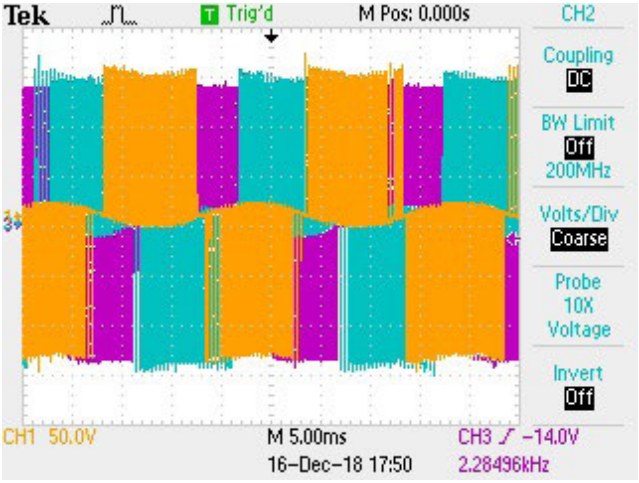

FIGURE 17. Experimental wave forms of the voltage between phases.

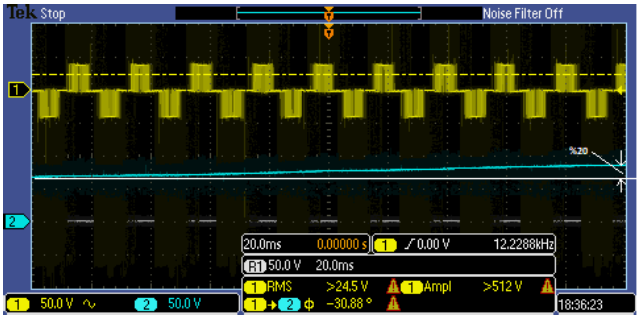

FIGURE 18. Simulated results for response of the Z-source inverter phase voltage subjected to step change in input voltage.

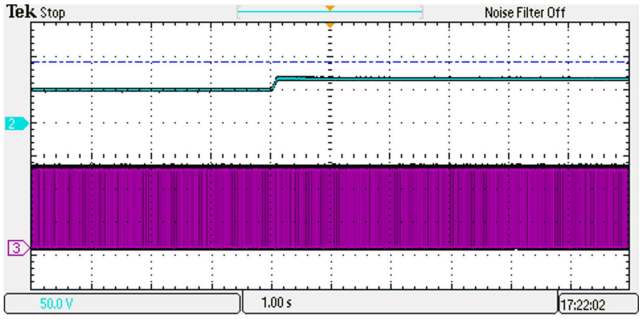

FIGURE 19. Response of the Z-source inverter DC link voltage subjected to step change in input voltage.

TABLE 2. Source information used in FPGA.

Resource	Estimation	Available	Utilization %
LUT	624	63400	0.98
FF	346	126800	0.27
DSP	1	240	0.42
IO	19	210	9.05

Figures 19 and 20 show that changes in the input signal are not reflected in the output. In this design, Xilinx Nexys 4 DDR development card is used and the resource information used is shown in Table 2.

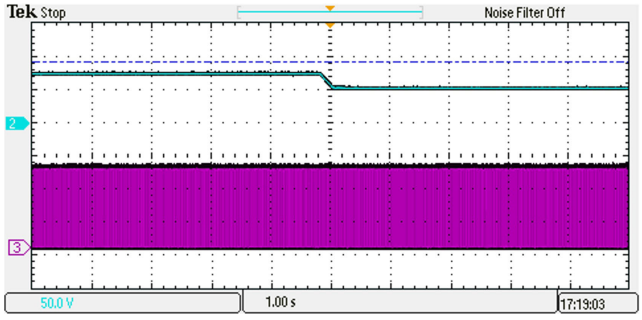

FIGURE 20. Response of the Z-source inverter DC link voltage subjected to step change in input voltage.

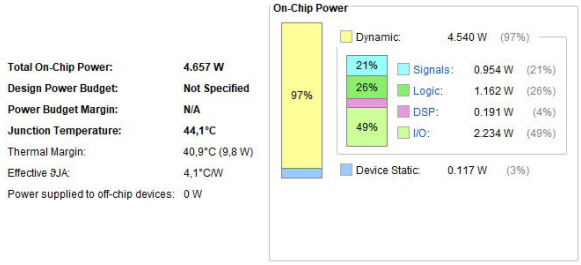

FIGURE 21. Power analysis from FPGA design.

The dynamic Power consumption of FPGA each resources used in this system is shown in Figure 21.

VI. CONCLUSION

In this study, a method for controlling DC line voltage and output voltage is proposed to overcome the ZSI power loss problems. Instead of directly measuring the output voltage, the capacity voltage is measured and the DC line voltage is estimated and thus the output voltage is controlled. For this purpose, the Z-source inverter is modeled by a state-space-average technique and the related transfer functions is derived.

PWM control and closed loop control units are implemented in FPGA environment without help of any IP core to increase performance in terms of resources and speed. The programmable structure of the FPGA provides both the flexibility and low latency demanded by control units. Power consumption is reduced considerably by implementing the controllers on a single FPGA platform.

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ALI RIZA YILMAZ received the B.S. degree in electrical and electronics engineering from Firat University, Elaziğ, Turkey, in 2010, and the M.S. degree in electronical and communications engineering from Yıldız Technical University (YTU), Istanbul, Turkey, in 2013, where he was a Research Assistant. He is currently a Research and Development Engineer with Turkish Technic. His research interests include FPGA, optimization algorithms, neural networks, and power electronics.

BURCU ERKMEN received the B.S., M.S., and Ph.D. degrees in electronics and communications engineering from Yıldız Technical University (YTU), Istanbul, Turkey, in 1999, 2001, and 2007, respectively. From 1999 to 2009, she was a Research Assistant with the Department of Electronics and Communications Engineering, YTU, where she has been an Associate Professor, since 2014. Her current research interests include power converters, optimization algorithms, artificial intelligence, and embedded systems.