A High Conversion Gain 210-GHz InP DHBT Sub-Harmonic Mixer Using Gain-Enhanced Structure

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ABSTRACT In this paper, we present a novel gain-enhanced sub-harmonic mixer based on 0.5-μm emitter width InGaAs/InP double heterojunction bipolar transistors (InP DHBTs). The proposed mixer consists of a transconductance stage and a gain-enhanced stage. A common-emitter transistor is used in the first stage to realize the sub-harmonic mixing while another common-emitter transistor is used in the second stage to remix the f_{LO+IF} and f_{IF} and also amplify the f_{2LO+IF}. For further verification, a transconductance mixer and a gain-enhanced mixer were designed and fabricated. Compared with the transconductance mixer, the gain-enhanced mixer exhibits a 6.8-dB higher conversion gain with 2-dB lower LO input power and a peak up-conversion gain of 9 dB at 213 GHz with $f_{IF} = 1$ GHz, $f_{LO} = 106$ GHz, and $P_{IF} = -26$ dBm $P_{LO} = 3$ dBm. To our best knowledge, the gain-enhanced mixing structure is proposed for the first time.

INDEX TERMS InGaAs/InP, DHBT, sub-harmonic mixer, gain-enhanced structure.

I. INTRODUCTION

InP double heterojunction bipolar transistors (InP DHBTs) are promising for terahertz application because of their superior electron transport properties, high breakdown voltage, and voltage handling capability [1]. As InP DHBTs have been demonstrated with maximum frequencies of oscillation (f_{max}) exceeding 1 THz [2], [3], many terahertz monolithic integrated circuits such as power amplifiers, mixers, complex integrated transmitter and receiver ICs have emerged [1]. Specially, there are many different technologies for terahertz monolithic integrated mixer operating above 100 GHz, and they can be classified into the following categories: single-ended, balanced, double-balanced, and image-reject mixers [4]–[12]. Besides, a batch of multifunctional chips including mixers integrated with amplifiers, LO drivers and antennas are reported [13]–[16].

Generally, harmonic mixers have been recognized as an interesting alternative to fundamental frequency mixers at high frequencies, which sharply reduce the requirement of high-frequency LO signal. However, there are fundamental frequency and harmonics at the output terminal, and these harmonics are usually filtered or counteracted by balanced structures in applications instead of being converted as wanted frequencies.

In order to address this issue and achieve a high conversion gain, high harmonic suppression and low consumption simultaneously, a novel gain-enhanced mixing structure is proposed in this paper. For further verification, a gain-enhanced mixer adopting two mixing stage was designed, abundant harmonics are generated from the first stage and converted in the second stage. For the purpose of comparison, another transconductance sub-harmonic mixer was designed. Final measurement results show that the gain-enhanced mixer exhibits a 6.8-dB higher conversion gain with 2 dB lower LO input power than the transconductance sub-harmonic mixer and a 9-dB peak conversion gain at 213 GHz. The improvement of the conversion gain was mainly from the high conversion efficiency of the unwanted harmonics.

This paper is organized as follows. The employed technology and devices are introduced in Section II. In Section III, the principle of the gain-enhanced mixing structure is introduced, and harmonic balance simulations are applied to verify the proposed idea. For further validation, a proof-of-concept

The associate editor coordinating the review of this manuscript and approving it for publication was Franco Fuschini.
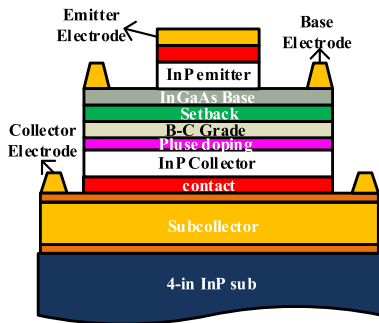
FIGURE 1. Cross-sectional view of an InP-based DHBT.

FIGURE 2. Principle of the gain-enhanced structure.

gain-enhanced mixer and a transconductance mixer were designed. Experimental results are discussed in Section IV. Finally, conclusion is drawn in section V.

II. DEVICE AND FABRICATION PROCESS

In our work, an advanced 0.5 μm InP DHBT technology is employed. The InP DHBT epitaxial structure is grown by using molecular beam epitaxy (MBE) on a 3-in semi-insulating substrate. The n^+InGaAs cap is highly doped for low emitter contact resistance. As shown in Fig.1, the base is 30 nm thick, the layer structure under the 150-nm-thick collector comprises a 50-nm-thick InGaAs collector contact, a 200-nm-thick InP subcollector and a 10-nm-thick InGaAs etch stop layer [17]. The transistors exhibit a current-gain cutoff frequency (f_t) of 350 GHz and a maximum frequency of oscillation (f_{max}) of 532 GHz. Passive circuit fabrication is implemented in a three-metal-layer interconnect system, where the top metal (M3) and the middle metal (M2) are available to support the signal transmission, and the bottom metal (M1) is used to be the ground plane. The bottom metal and the middle metal have identical thickness of 1.5 μm, and the top metal is 3 μm for a high-current capability. The three metal layers are separated by benzocyclobutene (BCB) with dielectric constant of 2.7. The thin-film NiCr resistors (25 Ω/square) and the metal-insulator-metal (MIM) SiN capacitors (0.24 fF/μm^2) are available.

III. CIRCUIT DESIGN AND PERFORMANCE

A. DESIGN THEORY DISCUSSION

Design of the mixer is based on a systematic characterization of InP DHBT devices and the gain-enhanced structure. As shown in Fig. 2, the proposed gain-enhanced mixer consists of a transconductance stage and a gain-enhanced stage. The principle of the proposed transconductance mixing stage is the same as the sub-harmonic mixer based on a common-emitter transistor [18]. However, for the gain-enhanced stage, it is difficult to analytically investigate its operation mechanism. Instead, harmonic balance simulations will be carried out in order to understand the contributions of each mechanism to the mixer's output. For the purpose of comparison, another transconductance mixing structure is simulated. The produced harmonics mainly
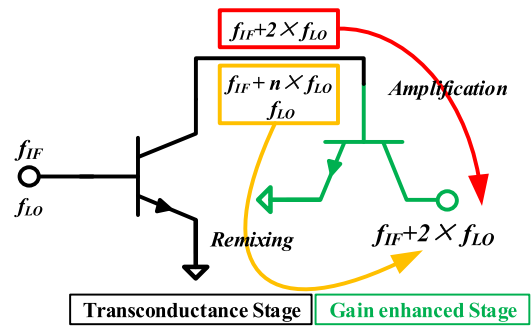
include f_{LO-IF}(103 GHz), f_{LO}(104 GHz), f_{LO+IF}(105 GHz), f_{2LO}(208 GHz), and f_{2LO+IF}(209 GHz). As shown in the Fig.3 (a), the transconductance mixing structure demonstrates a −23.8 dBm output power at 209 GHz (f_{2LO+IF}). Besides, the unwanted output powers at f_{LO-IF} (103 GHz), f_{LO}(104 GHz), and f_{LO+IF}(105 GHz) are −17.7 dBm, −4.2 dBm, and −17.3 dBm, respectively. For the gain-enhanced mixer, as all harmonics produced in the transconductance stage are inputted in the second stage, it delivers an output power of −16.7 dBm at 209 GHz (f_{2LO+IF}). Besides, the unwanted output powers at f_{LO-IF} (103 GHz), f_{LO}(104 GHz), and f_{LO+IF}(105 GHz) are −27.2 dBm, −14.6 dBm, and −26.4 dBm, respectively. Compared with transconductance mixing structure, the simulated conversion gain of gain-enhanced mixing structure is 7.1 dB higher. The f_{LO+IF} and f_{IF} are remixed with the f_{LO} to be converted to the f_{2LO+IF}, which is roughly equal to the sum of those obtained by the nonlinear converting (14 μw). Besides, the f_{2LO+IF} generated in the first stage and then amplified in the gain-enhanced stage is roughly equal to the sum of those obtained by the amplifying (3.2 μw). The harmonics are greatly reduced by adopting the gain-enhanced structure. The improvement of the enhanced conversion gain is traced to the conversion of the unwanted harmonics generated from the first stage.

B. CIRCUIT DESIGN

A proof-of-concept gain-enhanced mixer named as mx_2s and a transconductance mixer named as mx_1s were designed and fabricated in a 0.5-μm InP DHBT technology. The schematic of the mx_1s and mx_2s are depicted in Fig.4 (a) and (b), respectively. The single-stage transconductance mixer was designed using a 7-um emitter length common emitter DHBT, where class-B configuration was applied to achieve strong nonlinearity. Metal-insulator-metal (MIM) capacitors were applied in input and output stages for DC blocking. Moreover, the base and collector bias were designed using quarter-wave transmission lines and shunt capacitors, respectively. Besides, two extra series resistors 600 Ω and 300 Ω were used to suppress oscillations in the base and collector terminal, respectively. Modulating the transconductance by using the LO signal, both the LO and IF
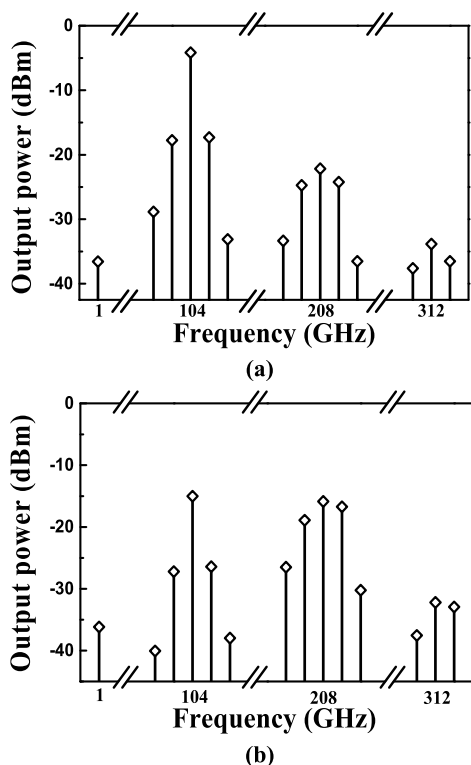
FIGURE 3. (a) Simulated output spectrum of the transconductance structure. (b) Simulated output spectrum of the gain-enhanced structure.

FIGURE 4. a) Schematic of the single-stage transconductance mixer. b) Schematic of the two-stage gain-enhanced mixer.

FIGURE 5. (a) Die microphotograph of the transconductance mixer. (b) Die microphotograph of the gain-enhanced mixer.

signals were applied to the base terminal and the wanted RF signal can be extracted from the collector terminal. The input matching network was designed for 50 ohm match to achieve highest conversion gain. The T-type matching networks were implemented using RF pad, MIM capacitor, microstrip transmission lines with different widths and open-circuited stubs. In the meantime, the parasitic effects of capacitors, GSG pads and interconnected via were also considered in the matching networks. Circuit configuration depicted in Fig. 4 (a) is constructed and simulated by using Ansoft High Frequency Structure Simulator (HFSS). Thereafter, full-wave electromagnetic simulation results are analyzed and optimized in Agilent Advanced Design System (ADS). Finally, the single stage transconductance mixer occupies a 0.7 mm × 0.5 mm die size, and the microphotograph of the transconductance mixer is depicted in Fig. 5 (a).

The first stage of gain-enhanced mixer was configured the same topology as transconductance mixer, where abundant harmonics were inputted in the second stage. Class-B configuration was applied to achieve strong nonlinearity including the harmonics remixing and amplification in the second stage. Similarly, two extra series 600 Ω and 300 Ω resistors were used to suppress oscillations in the base and collector terminal, respectively. The matching networks were implemented using RF pad, MIM capacitor, microstrip transmission lines with different widths and open-circuited. Using the same method, the layout of mx_2s was finally determined, it occupies a 1 mm × 0.5 mm die size, and the microphotograph of the gain-enhanced mixer is depicted in Fig. 5 (b).
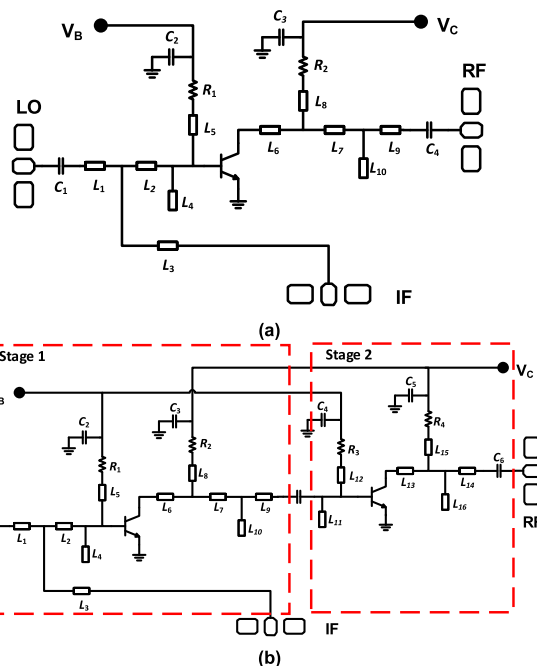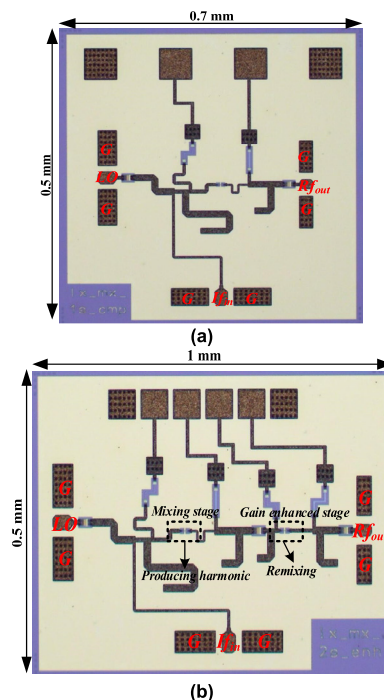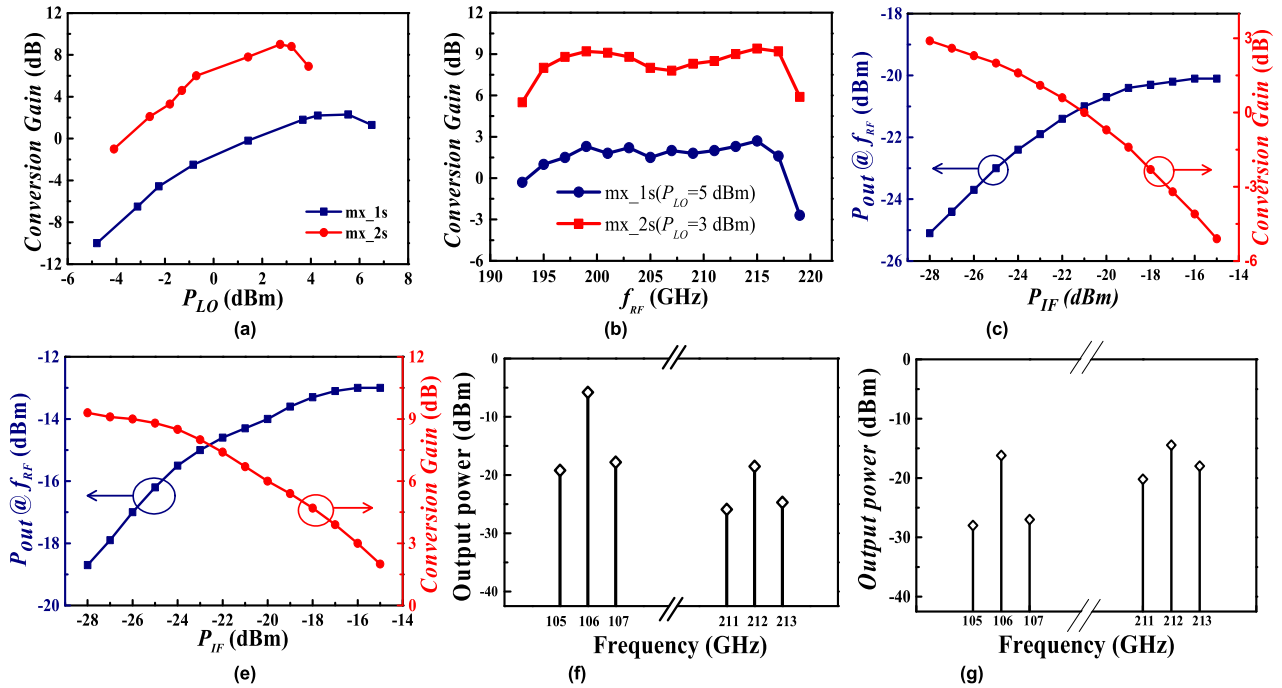
IV. MEASURED RESULTS

The fabricated mixer was measured by using a Cascade on-wafer probing system. IF and LO input signal at 106 GHz was generated by a signal source and a 90-110 GHz frequency multiplier module combined with a power amplifier block,

FIGURE 6. (a) Measured conversion gains of two mixers versus LO input power at 106 GHz. (b) Measured conversion gains of two mixers versus LO frequency (f_{IF} = 1 GHz, P_{IF} = −26dBm). (c) Measured output RF powers and conversion gains of the transconductance mixer with 5 dBm input LO power versus input IF power (f_{LO} = 106 GHz). (d) Measured output RF powers and conversion gains of the gain-enhanced mixer with 3 dBm input LO power versus input IF power (f_{LO} = 106 GHz). (e) Simulated output spectrum of the transconductance structure. (f) Simulated output spectrum of the gain-enhanced structure.

respectively. Besides, a spectrum analyzer with a Farran mixing modules was used to detect the output spectrum. The measured conversion gains versus LO input power and input LO frequency are depicted in Fig. 6 (a) and (b), respectively. The mx_1s and mx_2s achieve a 2.3-dB and a 9-dB peak conversion gain with f_{IF} = 1 GHz, f_{LO} = 106 GHz, P_{IF} = −26 dBm, P_{LO} = 5 dBm and P_{LO} = 3 dBm, respectively. Compared with the mx_1s, the mx_2s demonstrates a 6.8-dB higher conversion gain with a 2-dB lower LO input power, and the conversion gain characteristics of the mx_1s and mx_2s are −2.7 ∼ 2.3 dB and 5.5 ∼ 9 dB at the RF frequency range of 194-217 GHz, respectively. Besides, as the input LO powers are 5 dBm and 3 dBm at 106 GHz separately for mx_1s and mx_2s, the output power performance was measured by varying the input IF power, the saturated RF output powers of mx_1s and mx_2s are −20 dBm and −13 dBm, as shown in Fig. 6 (c) and Fig. 6 (d). The mx_2s achieves a 7 dB higher saturated output power compared with the mx_1s. Moreover, the main output spectrums around f_{LO} and f_{2LO} are measured as well, as shown in Fig. 6 (e) and (f), respectively. The measured spectrums agree well with the simulated results in Fig. 3 (a) and (b). Performance comparison between the gain-enhanced mixer and other works operating at frequencies above 100 GHz is given in Table 1. Obviously, the proposed mixer is featured by high conversion gain which owes to the high conversion efficiency of the gain-enhanced structure.

TABLE 1. Comparison of reported mixers above 100 GHz.

Ref	Process (nm)	f_{RF} (GHz)	f_{LO} (GHz)	Conversion gain (dB)	P_{LO} (dBm)	P_{sat} (dBm)	Mixer type
[4]	28 CMOS	129-140	124-134	-6	0	-	Gilbert
[5]	100 GaAs mHEMT	200-220	200-220	-8.7	1.5	-	Single Ended
[9]	250 InP DHBT	250-310	280	-5.2	-4	-14	Gilbert
[10]	40 CMOS	105-135	120	-4	-10	-7.5	Gilbert
[11]	Schottky Diode	199-238	101-119	7.84-12.4	4.9	-17.1	Single Balanced
[12]	130 SiGe BiCMOS	100-140	46-68	2.6	5	-7.2	Bottom LO trans.
[13]	65 CMOS	139-147	144	9.7	-	10.1	DSB +5stage PA
Our work	500 InP DHBT	194-217	106	9	3	-13	Gain-enhanced

V. CONCLUSION

In this paper, a sub-harmonic mixer using 0.5 μm InP DHBT technology is demonstrated. It is the first demonstration of a sub-harmonic mixer using gain-enhanced mixing structure. By using this structure, the unwanted harmonics can be converted into the RF output signal, the conversion gain is greatly improved with the same or even less LO input power, and

the unwanted output harmonics are simultaneously reduced compared with the transconductance mixer. The performance of the gain-enhanced mixer is believed to be better with regard to conversion gain and LO power level as compared to other earlier published mixers. The measurement shows that the gain-enhanced mixer exhibits a peak conversion gain of 9 dB with 3 dBm LO input power at RF frequency of 213 GHz. This concept is also effective for sub-harmonic down-conversion mixer, and it will be utilized in balanced mixer and transceiver front-end in the future.

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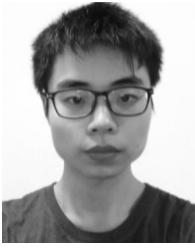
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