Linear Active Disturbance Rejection Control for Three-Phase Voltage-Source PWM Rectifier

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ABSTRACT Three-phase voltage-source pulse width modulation (PWM) rectifier has been widely employed in various industrial applications. For the traditional dual-loop PI control of three-phase voltage-source PWM rectifier, the voltage loop and current loop have poor disturbance rejection performance and long response time. A linear active disturbance rejection control (LADRC) strategy is proposed for three-phase voltage-source PWM rectifier in this paper. The coupling variable and external disturbance in the model of PWM rectifier are observed and compensated by linear extended state observer (LESO) in two-phase synchronous reference frame. The LADRC outer-voltage loop controller and LADRC inner-current loop controller of PWM rectifier are designed. The proposed control strategy is compared and verified with PI control and ADRC by MATLAB/Simulink. Simulation and experimental results confirm the superiority of proposed control strategy in dynamic performance and disturbance rejection.

INDEX TERMS Pulse width modulation (PWM) rectifier, linear extended state observer (LESO), linear active disturbance rejection control (LADRC), PI control, robustness.

I. INTRODUCTION

As a highly efficient and reliable power converter, the three-phase voltage source pulse width modulation (PWM) rectifier has the advantages of unit power factor operation, low input current harmonic content, controllable DC side voltage, and bidirectional flow of energy. It has found success in many applications in different fields such as renewable energy, high voltage direct current (HVDC) transmission, active power filter and so on [1-5]. In order to improve the control performance, the control system of PWM rectifier often adopts a double closed-loop cascade control structure composed of outer-voltage loop and inner-current loop [6], but the design of control system often focuses on the inner-current loop control issue, while the outer-voltage loop control has not yet attracted enough attention. Although the PI control strategy was always adopted in case of the controller for PWM rectifier, actually it was hard to satisfy with the PI control strategy for its slow dynamic response speed and sensitive to disturbances. Therefore, many new control strategies were surged in order to achieve high dynamic performance, disturbance rejection and strong robustness. These are internal model control (IMC)[7-8], proportional resonance control (PR)[9-10], model predictive control (MPC)[11-12], dead-beat control (DBC) [13-14], and active disturbance rejection control (ADRC)[15-22], etc.

In [7], IMC was applied to the inner-current loop control of PWM rectifier, and the conventional PI method was replaced by internal model controller. In [8], the design of a controller was proposed based on IMC applied to a grid connected single-phase PWM inverter, and 1-DOF IMC controller was presented and the decoupling of grid voltage was analyzed by a feed forward strategy. The IMC adopted in [7] and [8] has strong anti-interference ability, but the uncertainty of the model may lead to model mismatch. In [9] and [10], as to current vector error elimination, the optimized PR controller of the inner current loop was proposed with the zero-pole matching method to configure the controller, which achieves the static-free control of the sinusoidal signal and optimizes the structure of the system, however, the design of controller is more complicated. In [11-14], the proposed MPC method for three-phase PWM rectifier calculates the optimized voltage vector by analyzing the relationship of the virtual flux, active power, converter voltage, and filter parameters, and the predictive algorithm computes the power error that would be produced by applying each vector and selects the one that contributes the minimum error, which improves performance of the rectifier, however, it is difficult to satisfy high real-time requirement considering the large number of complex
computations. In [15] and [16], a mathematical model of PWM rectifier was introduced based on DBC in a two-phase stationary $\alpha-\beta$ coordinate system, which solves the problem of delay compensation caused by sampling and digital processing, and reduces the error caused by sampling, however, sampling period and the time-delay of calculation affect the performance of PWM rectifier.

ADRC is a control technique proposed by Prof. Han [17]. The central idea is to treat the internal uncertainties and external disturbances as a "lumped disturbance," and try to estimate in real-time by an extended state observer (ESO), and then use it in the feedback with the aim to compensate the disturbance quickly. The ADRC as a practical design method has been successfully applied in many engineering applications [18-22], and the performance of the controlled object is effectively improved.

ADRC has strong robustness against disturbance and does not depend on an accurate model of the controlled object, but the structure of ADRC is still complex and needs to tune a bunch of parameters, meanwhile, ADRC uses a lot of nonlinear functions, which lead to many system parameters and difficult adjustment [23-24]. To overcome the difficulty, [25] and [26] consider LADRC, where linear extended state observer (LESO) and linear state error feedback (LSEF) are used. The study in [27-28] shows that the parameterized LADRC not only gives much better performance, but also it is the easiest to tune. LADRC has better dynamic tracking performance and disturbance rejection, and has been successfully applied in many engineering applications [29-33].

In this paper the strategy of LADRC is proposed for PWM rectifier. The parameters perturbation and coupling variable of PWM rectifier model are regarded as system disturbance, and LESO is used to observe and compensate the disturbance. The LADRC voltage loop controller and LADRC current loop controller of PWM rectifier are designed, and the correctness and effectiveness of the control method are verified by simulation and physical experiment. Finally, Simulation and experimental results demonstrate that the proposed control strategy has better dynamic performance and robustness.

The rest of this paper is organized as follows: First, the mathematical model of three-phase voltage-source PWM rectifier is presented in Section II. Then the design of LADRC for PWM Rectifier is introduced in Section III. In Section IV, simulations and experimental results are presented. Finally, the conclusion is summarized in Section V.

II. MATHEMATICAL MODELE OF VOLTAGE-SOURCE
PWM RECTIFIER

The circuit of a three-phase PWM rectifier is shown in Fig.1, where the rectifier is connected to the grid through inductance $L$ and resistance $R$.

**FIGURE 1. The topology of three-phase voltage-source PWM rectifier.**

The mathematical model of three-phase PWM rectifier in $a$-$b$-$c$ stationary frame can be obtained:

$$
\begin{align*}
L \frac{di_a}{dt} &= e_a - R i_a - \frac{U_{dc} (2S_a - S_b - S_c)}{3} \\
L \frac{di_b}{dt} &= e_b - R i_b - \frac{U_{dc} (2S_b - S_a - S_c)}{3} \\
L \frac{di_c}{dt} &= e_c - R i_c - \frac{U_{dc} (2S_c - S_a - S_b)}{3} \\
C \frac{dU_{dc}}{dt} &= S_a i_a + S_b i_b + S_c i_c - i_L
\end{align*}
$$

(1)

where $e_a$, $e_b$, and $e_c$ are three-phase grid voltages, $i_a$, $i_b$, and $i_c$ are grid side currents, $L$ denotes the AC side inductor, $R$ denotes the equivalent internal resistance, $C$ denotes the DC bus capacitor, $U_{dc}$ denotes the DC bus voltage, and $i_L$ denotes the load current, $S_a$, $S_b$ and $S_c$ are switch function, respectively.

The voltage and current in $a$-$b$-$c$ stationary frame are time-varying sine wave, which makes it difficult to analyze. Therefore, the vector variables in $d$-$q$ synchronous rotating reference frame can be obtained from the $a$-$b$-$c$ stationary frame by the Clarke and Park transformation, which can be expressed as:

$$
\begin{align*}
L \frac{dI_d}{dt} &= e_d - R I_d + \omega L I_q - u_{rd} \\
L \frac{dI_q}{dt} &= e_q - R I_q - \omega L I_d - u_{rq} \\
C \frac{dU_{dc}}{dt} &= \frac{3}{2} (S_d I_d + S_q I_q) - I_L
\end{align*}
$$

(2)

where $\omega$ denotes angular frequency of the grid voltage, $u_{rd}$ and $u_{rq}$ are the $d$ and $q$ component of AC side voltage of PWM rectifier, $S_d$ and $S_q$ are the $d$ and $q$ components of the switch function, $e_d$ and $e_q$ are $d$ and $q$ component of three phases grid voltage, $I_d$ and $I_q$ are $d$ and $q$ component of the grid side current, respectively. The structure diagram of PWM rectifier in $d$-$q$ reference frame is shown in Fig. 2.
Ⅲ. CONTROL STRATEGY OF THE THREE-PHASE VOLTAGE-SOURCE PWM RECTIFIER

In order to improve the control performance of PWM rectifier, a control scheme of LADRC is proposed in this paper. The proposed LADRC scheme adopts a double closed-loop cascade control structure composed of outer-voltage loop and inner-current loop. The \( i_d \), \( i_q \) and \( U_{dc} \) are selected as the state variables of the system.

A DESIGN OF LADRC SCHEME

The structure of ADRC is shown in Fig.3, and it mainly consists of three parts: tracking differentiator (TD), extended state observer (ESO) and nonlinear state error feedback (NLSEF). ESO obtains the estimated value \( z_1, z_2, \ldots, z_n \) of the system state variable and the estimated value \( z_{n+1} \) of lumped disturbance. Differential signals \( x_1 \) and \( x_0 \) of transition process obtained by TD, and NLSEF calculates the control signal \( u_0 \) according to the state error \( e_1, e_0 \) of the system. ADRC is a nonlinear controller, which has strong robustness against disturbance and does not depend on an accurate model of the controlled object.

According to the principle of LADRC, the proposed control strategy is illustrated in Fig.5, which consists of three first-order LADRC, that is voltage loop, \( d \)-axis current loop and \( q \)-axis current loop. For the voltage loop, the measured \( U_{dc} \) is compared with the reference voltage \( U_{dc}^* \) to obtain the reference current \( i_d^* \) via a LADRC controller. The reference values of \( i_{rd} \) and \( i_{eq} \) are obtained by the controller of \( d \)-axis current loop and the \( q \)-axis current loop, which are sent to the space vector pulse width modulation (SVPWM) module. The SVPWM module is used in the main circuit of the rectifier.
While the switch loss of PWM rectifier is neglected, the \( \text{RECTIFIER} \) is balanced with the active power on the AC side. According to the LADRC theory, if the coupling terms are regarded as the internal disturbance of the system, the LESO is used to observe and compensate, then the complete decoupling control of \( d \)-axis and \( q \)-axis currents can be realized.

### B. DESIGN OF LADRC FOR VOLTAGE LOOP IN PWM RECTIFIER

While the switch loss of PWM rectifier is neglected, the active power on the AC side \( P_{\text{ac}} \) is balanced with the active power on the DC side \( P_{\text{dc}} \), the relationship between the \( P_{\text{ac}} \) and \( P_{\text{dc}} \) is:

\[
P_{\text{ac}} = P_{\text{dc}}
\]

The equations of \( P_{\text{ac}} \) and \( P_{\text{dc}} \) are expressed as:

\[
P_{\text{ac}} = \frac{3}{2} (e_d - R_{i_d}) i_d + \frac{3}{2} (e_q - R_{i_q}) i_q
\]

\[
P_{\text{dc}} = U_{\text{dc}} C \frac{dU_{\text{dc}}}{dt} + \frac{U_{\text{dc}}^2}{R_L}
\]

The equation (9) can be obtained from (7) and (8):

\[
\frac{3}{2} (e_d - R_{i_d}) i_d + \frac{3}{2} (e_q - R_{i_q}) i_q = U_{\text{dc}} C \frac{dU_{\text{dc}}}{dt} + \frac{U_{\text{dc}}^2}{R_L}
\]

Using grid voltage orientation vector control, then \( e_q = 0 \). In order to achieve unit power factor control of PWM rectifier, let \( i_q = 0 \), and \( w = (U_{\text{dc}})^2 \), so equation (9) is obtained as:

\[
du = \frac{-2u}{R_1 C} + \frac{3(e_d - R_{i_d}) i_d}{C}
\]

Equation (8) can be transformed from (10):

\[
du = b \cdot i_d + w_1(t)
\]

\[
b = \frac{3(e_d - R_{i_d})}{C}
\]

\[
w_1(t) = \frac{-2u}{R_1 C}
\]

where \( w_1(t) \) is lumped disturbance of the system, and it can be seen from equation (13) that \( R_1 \) is included in the \( w_1(t) \). If \( R_1 \) changes during the operation of the rectifier, LESO will estimate \( w_1(t) \) and make compensation in real-time, which can effectively suppress the impact of load changes.

The discrete equation of the LTD transition process in the voltage loop can be expressed as:

\[
\begin{align*}
x_1(k+1) &= x_1(k) + T \cdot x_1(k) \\
x_2(k+1) &= x_2(k) + T \cdot g(x(k) - v(k), x_1(k), r)
\end{align*}
\]

where \( v(k) \) is the input signal of the voltage loop LADRC, and \( v(k) \) corresponds to the given voltage \( (U_{\text{dc}})^2 \) of the voltage loop LADRC, \( x_1(k) \) tracks the input signal \( v(k) \), \( x_2(k) \) is the differential of \( x_1(k) \), \( T \) is the discrete control period, \( r \) is the adjustable parameter. The larger the \( r \), the faster the tracking speed, however, it also increases the amount of overshoot. The parameters can be adjusted according to the output waveform of LTD. The function \( g(x) \) can be presented as:

\[
g(x(k) - v(k), x_1(k), r) = \sqrt{r \cdot x_2(k)} - \sqrt{r \cdot x_1(k)} - v(k)
\]

Consider \( w_1(t) \) in equation (11) as the disturbance, and the discrete LESO equation in the voltage loop is constructed as followed:

\[
\begin{align*}
e(k) &= z_1(k) - y(k) \\
z_1(k+1) &= z_1(k) + T \cdot [z_2(k) - \beta_1 e(k) + b \cdot u_1(k)] \\
z_2(k+1) &= z_2(k) - T \cdot \beta_2 e(k)
\end{align*}
\]

where \( y(k) \) corresponds to the voltage feedback \( (U_{\text{dc}})^2 \) of the voltage loop LADRC, \( z_1(k) \) is the estimated value of \( (U_{\text{dc}})^2 \), and \( z_2(k) \) is the estimated value of the total disturbance of the system, \( \beta_1 \) and \( \beta_2 \) are the error correction coefficients of LESO output. The dynamic characteristics of the controlled object are largely determined by \( \beta_1 \) and \( \beta_2 \).

According to the output of LTD and LESO, the discrete equation for constructing LSEF in the voltage loop is expressed as:

\[
\begin{align*}
e_i(k) &= x_i(k) - z_1(k) \\
u_0(k) &= k_p e_i(k) \\
u_1(k) &= u_0(k) - z_2(k) / b
\end{align*}
\]
where \( u_1(k) \) is the output control quantity of the voltage loop LADRC, and \( u_1(k) \) corresponds to the active current command \( i_d' \) of the current loop in Fig. 5.

In order to stabilize the system, the poles of LESO are allocated at LESO bandwidth \( (\omega_o) \) while the poles of closed-loop are allocated at the controlled object bandwidth \( (\omega_c) \), and \( \omega_o = 3 - 5 \omega_c \). Therefore, the equations can be written as the following relation:

\[
\begin{align*}
    s^2 + \beta_1 s + \beta_2 &= (s + \omega_c)^2 \\
    s + k_p &= s + \omega_c \\
    \beta_1 &= 2 \omega_c, \quad \beta_2 = \omega_c^2, \quad k_p = \omega_c
\end{align*}
\] (18)

(19)

**C DESIGN OF LADRC FOR D-AXIS CURRENT LOOP IN PWM RECTIFIER**

The mathematical model of the d-axis current loop can be denoted by the following equation:

\[
\frac{d i_d}{dt} = b_1 \cdot u_{rd} + w_2(t) \tag{20}
\]

\[
b_1 = \frac{-1}{L} \tag{21}
\]

\[
w_2(t) = \frac{(e_d - R_i d)}{L} + \omega i_d \tag{22}
\]

The coupling term \( o i_d \) and the external disturbance \( (e_d - R_i d)/L \) in \( w_2(t) \) are regarded as the lumped disturbance of the system. The coupling term and external disturbance will affect the control performance of PWM rectifier. The LESO can be used to estimate and compensate \( w_2(t) \) in real-time. The discrete equation of the LTD transition process in the d-axis current loop can be obtained as:

\[
\begin{align*}
    x_1(k+1) &= x_1(k) + T \cdot x_1(k) \\
    x_2(k+1) &= x_2(k) + T \cdot g(f(x_2(k) - v_1(k), x_1(k), r])
\end{align*}
\] (23)

where \( v_1(k) \) is the input signal of the d-axis current loop LADRC, and \( v_1(k) \) corresponds to the given current \( i_d' \), which is output signal of LADRC in outer-voltage loop. The \( x_2(k) \) tracks the input signal \( v_1(k) \), and \( x_2(k) \) is the differential of \( x_1(k) \). The design of LESO and LSEF in the d-axis current loop is similar to the voltage loop, and the parameter tuning process is the same as the voltage loop.

**D DESIGN OF LADRC FOR Q-AXIS CURRENT LOOP IN PWM RECTIFIER**

The mathematical model of the q-axis current loop can be represented as:

\[
\frac{d i_q}{dt} = b_2 \cdot u_{rq} + w_3(t) \tag{24}
\]

\[
b_2 = \frac{-1}{L} \tag{25}
\]

\[
w_3(t) = \frac{(e_q - R_i q)}{L} \cdot \omega i_d \tag{26}
\]

Similarly, there is a coupling term \(-o i_d\) and an external disturbance \((e_q - R_i q)/L\) in \( w_3(t) \). Therefore, the q-axis current loop also uses LADRC, which design is similar to the d-axis current loop.

**III. SIMULATION AND EXPERIMENTAL RESULTS**

In order to evaluate the correctness and effectiveness of the proposed control strategy, the simulation and experiment are implemented for LADRC, ADRC and PI control.

**A SIMULATION RESULTS**

The control performances of PWM rectifier are analyzed and compared by MATLAB/Simulink. The parameters of the simulation are shown in Table 1. Fig.6 shows the simulation results of LESO. Fig.7 shows the simulation results when rectifier operates in the steady state. Fig.8 is the simulation waveforms when the reference of DC side voltage sudden changes in PWM rectifier. Fig.9 shows the simulation results when the load of PWM rectifier sudden changes.

**TABLE 1. The simulation parameters.**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Name</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( U_s )</td>
<td>AC voltage amplitude</td>
<td>380</td>
<td>V</td>
</tr>
<tr>
<td>( f_s )</td>
<td>AC voltage frequency</td>
<td>50</td>
<td>Hz</td>
</tr>
<tr>
<td>( L )</td>
<td>AC side inductor</td>
<td>3</td>
<td>mH</td>
</tr>
<tr>
<td>( U_{dc} )</td>
<td>DC side voltage reference</td>
<td>600</td>
<td>V</td>
</tr>
<tr>
<td>( C )</td>
<td>DC side capacitor</td>
<td>2000</td>
<td>μF</td>
</tr>
<tr>
<td>( f_c )</td>
<td>Switching frequency</td>
<td>10</td>
<td>kHz</td>
</tr>
<tr>
<td>( R_{t} )</td>
<td>System rated load</td>
<td>144</td>
<td>Ω</td>
</tr>
<tr>
<td>( P )</td>
<td>The output power</td>
<td>2.5</td>
<td>kW</td>
</tr>
<tr>
<td>( U_c )</td>
<td>Capacitor initial voltage</td>
<td>540</td>
<td>V</td>
</tr>
</tbody>
</table>

Fig.6 shows the simulation waveforms of \( z_1 \), \( z_2 \) and \( w_1(t) \), where \( z_1 \) is estimated value of state variable, \( w_1(t) \) is actual value of lumped disturbance and \( z_2 \) is estimated value of lumped disturbance observed by LESO. It can be seen from Fig.6 that LESO can accurately estimate disturbances when the load of rectifier sudden changes from 144Ω to 72Ω at \( t=0.2s \).

---

[FIGURE 6. \( z_1 \), \( z_2 \) and \( w_1(t) \) waveforms.]
Fig. 7(a), Fig. 7(b) and Fig. 7(c) show the voltage and current waveforms of a-phase of rectifier controlled by PI control, ADRC and LADRC respectively. It can be seen from Fig. 7(a), Fig. 7(b) and Fig. 7(c) (the voltage is reduced by 10 times in figure) that the grid side current is a sine wave, and the system operates in the unit power factor state. As shown in Fig. 7(d), the rectifier controlled by LADRC exhibits much faster and no overshoot of the starting process than the rectifier controlled by PI and ADRC. The FFT analysis results of the grid current are shown in Fig. 7(e), Fig. 7(f) and Fig. 7(g). The THD is 4.13% when rectifier is controlled by PI, the THD is 2.41% when rectifier is controlled by ADRC, and the THD is reduced to 2.03% when rectifier is controlled by LADRC.

The performance comparison shows that three control strategies are almost the same in power factor shown in Table 2. However, it is also obvious that the LADRC
strategy has faster recovery time and smaller harmonic contents than PI control and ADRC. These results imply that the LADRC control strategy can improve the steady state performance of the PWM rectifier.

### TABLE 2. Performance comparison of three control strategies under steady state.

<table>
<thead>
<tr>
<th>Performance</th>
<th>PI</th>
<th>ADRC</th>
<th>LADRC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid current THD/ %</td>
<td>4.13</td>
<td>2.41</td>
<td>2.03</td>
</tr>
<tr>
<td>Input power factor</td>
<td>0.998</td>
<td>0.998</td>
<td>0.998</td>
</tr>
<tr>
<td>Recovery time/s</td>
<td>0.15</td>
<td>0.12</td>
<td>0.08</td>
</tr>
<tr>
<td>Overshoot/ %</td>
<td>1.34</td>
<td>0.68</td>
<td>0.00</td>
</tr>
</tbody>
</table>

The simulation results are shown in Fig.8 when the DC-side voltage reference drops from 600 V to 550 V at 0.2s and other conditions remain unchanged. Fig.8(a), Fig.8(b) and Fig.8(c) (the voltage is reduced by 10 times in figure) are simulation waveforms of grid voltage and current when DC-side voltage reference sudden changed, and it can be seen that the a-phase current can quickly recoveries into sine wave in the case of a sudden change in DC-side voltage, and the PWM rectifier can operates at unit power factor state. It can be seen from Fig.8(d) that the recovery time is 0.15s with PI control, the recovery time with ADRC is 0.12s and the recovery time is reduced to 0.07s with LADRC. Fig.8(e), Fig.8(f) and Fig.8(g) show the THD of grid current with PI control is 4.43%, the THD with ADRC is 2.78%, and the THD with LADRC is 2.35%.
By comparing the result shown in Table 3, it can be seen that the harmonic contents and recovery time are reduced with LADRC control strategy when the reference of DC-side voltage sudden changes.

**TABLE 3. Performance comparison of three control strategies when the reference of DC-side voltage sudden changes.**

<table>
<thead>
<tr>
<th>Performance</th>
<th>PI</th>
<th>ADRC</th>
<th>LADRC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid current THD/%</td>
<td>4.43</td>
<td>2.78</td>
<td>2.35</td>
</tr>
<tr>
<td>Input power factor</td>
<td>0.998</td>
<td>0.998</td>
<td>0.998</td>
</tr>
<tr>
<td>Recovery time/s</td>
<td>0.15</td>
<td>0.12</td>
<td>0.07</td>
</tr>
<tr>
<td>Overshoot/%</td>
<td>1.264</td>
<td>0.64</td>
<td>0</td>
</tr>
</tbody>
</table>

Fig. 9 shows the simulation results when the load of rectifier sudden changes and other conditions remain unchanged. It can be seen from Fig.9(a), Fig.9(b) and Fig.9(c) (the voltage is reduced by 10 times in Figure) that the grid voltage and current is in the same phase. It is clearly observed that there are much smaller ripples in the DC-side voltage of the proposed LADRC method compared to PI control and ADRC from Fig.9(d). The Fig.9(e), Fig.9(f) and Fig.9(g) show that the grid current controlled by LADRC has smaller harmonic contents. These results clearly confirm that the proposed method is effective when the load of rectifier sudden changes.
The THD with ADRC

The THD with LADRC

FIGURE 9. Simulation waveforms when the load of rectifier sudden changes.

The performance comparison of three control strategies is shown in Table 4 when the load of rectifier sudden changes, the comparison results confirm that the LADRC control strategy can improve the dynamic and disturbance rejection performance of PWM rectifier when the load of rectifier sudden changes.

<table>
<thead>
<tr>
<th>Performance</th>
<th>PI</th>
<th>ADRC</th>
<th>LADRC</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC current THD/%</td>
<td>4.68</td>
<td>2.43</td>
<td>2.01</td>
</tr>
<tr>
<td>Input power factor</td>
<td>0.998</td>
<td>0.998</td>
<td>0.998</td>
</tr>
<tr>
<td>Recovery time/s</td>
<td>0.18</td>
<td>0.15</td>
<td>0.08</td>
</tr>
<tr>
<td>Overshoot/%</td>
<td>1.3</td>
<td>0.61</td>
<td>0</td>
</tr>
<tr>
<td>DC voltage drop/%</td>
<td>2</td>
<td>1.5</td>
<td>0.8</td>
</tr>
</tbody>
</table>

The aforementioned simulation results clearly confirm that the proposed method is effective in terms of both steady-state response and dynamic processes.

B EXPERIMENTAL RESULTS

To verify the feasibility and effectiveness of the proposed control strategy, a three-phase voltage-source PWM rectifier experimental platform is built up according to the structure given in Fig. 5 and is shown in Fig. 10. The parameters of the experimental prototype are listed in Table 5. The control algorithms are implemented on a 32-b DSP TMS320F28335.

The performances of rectifier controlled by three method at steady-state are almost the same in the experiment. Fig.11 shows the experimental waveforms when the rectifier controlled by the proposed method operates in steady-state. It can be seen from Fig.11 that the grid side current is a sine wave and the grid voltage and current is in the same phase. It is clearly observed that the proposed control strategy can obtain good current waveforms and the rectifier can achieve unit power factor operation.
dynamic tracking performance, disturbance rejection and voltage-loop and current-loop considering its better disturbance rejection control algorithm has been applied to voltage loop and inner-current loop. The linear active double closed-loop cascade structure composed of outer-three-phase voltage-source PWM rectifier, which is a IV. CONCLUSION

changes.

FIGURE 12. Experimental waveforms when the load of rectifier sudden changes.

Fig.12 shows the dynamic responses for traditional PI control and proposed LADRC method when load is suddenly changed to the system. It is clearly seen that the proposed LADRC method remains effective at reducing DC-side voltage ripples and that LADRC outperforms PI control when the load subjects to sudden change.

REFERENCES

This paper proposes a novel control strategy for the three-phase voltage-source PWM rectifier, which is a double closed-loop cascade structure composed of outer-voltage loop and inner-current loop. The linear active disturbance rejection control algorithm has been applied to voltage-loop and current-loop considering its better dynamic tracking performance, disturbance rejection and stronger robustness. The proposed strategy uses LSO and LSEF, which needs less nonlinear functions than ADRC. A comparative simulation and experiment with conventional PI control, ADRC and proposed LADRC control is conducted, and obtained results validate that satisfactory steady-state performance and fast dynamic responses could be achieved by proposed LADRC control.


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