PCB Layout Optimization of High-Frequency Inverter for Magnetic Coupled Resonance Wireless Power Transfer System

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This research was funded by National Natural Science Foundation of China, No. 61703081, the Natural Science Foundation of Liaoning Province, No. 20170520113, and the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, No. LAPS19005.

ABSTRACT Magnetic coupled resonance wireless power transfer system has the advantages of long transfer distance and high efficiency. However, it needs a high-frequency AC power, and the influence of the circuit parasitic elements at high frequency cannot be ignored, which brings challenges to the research and the design of the high-frequency power for the wireless power transfer system. In this paper, the effect of the parasitic elements in the full-bridge inverter and the reasons of high-frequency ringing generated are analyzed in detail. The influences of device packaging and the printed circuit board (PCB) layout on circuit parasitic elements are studied. An optimized inverter PCB layout design that aims to reduce the parasitic elements and to provide a stable and high-quality AC power for the wireless power transfer system is presented. Finally, the performance of the conventional PCB layout design and the proposed optimized PCB layout design are compared through experiments. The experiment results show that the proposed design not only reduces the parasitic inductance in the circuit, but also reduces the electromagnetic interference noises and improves the stability of the inverter at 900kHz switching frequency.

INDEX TERMS Magnetic coupled resonance, Wireless power transfer, High-frequency inverter, Parasitic elements, PCB layout.

I. INTRODUCTION

The Magnetic coupled resonance wireless power transfer (MCR-WPT) system has the advantages of high transfer efficiency and long transfer distance, which has become a special study in the field of wireless power transfer. Due to its good balance between the transfer distance and the transfer efficiency, MCR-WPT technology is used in many daily and industrial applications, such as smart phones, electric vehicles, and biomedical applications [1].

The basic principle of the MCR-WPT technology is the resonance between the transmitting coil and the receiving coil. The resonant frequency is equal to the switching frequency of the system [2]-[4]. For MCR-WPT system, the transfer frequency is generally several tens of kHz to tens of MHz. Within limits, increasing the frequency of the MCR-WPT system can effectively increase the transfer distance of the system, and decrease the size of the coupling coil, and improve the portability and practicability of the system [5]. This provides a good performance for low-power applications such as home appliances, material handling, and forklift charging, etc. However, at high frequency, the loss of the system will increase, which will affect efficiency. And the parasitic parameters in the inverter printed circuit board (PCB) will have a great influence on the circuit under high frequency working environment [6]. Therefore, a stable and high-quality AC power is essential for the MCR-WPT system. The research of the PCB layout in this paper is mainly to reduce the influence of parasitic parameters and to provide a stable and high-quality AC power for the MCR-WPT system. Thus, the design of the high-frequency inverter VOLUME 4, 2016
is crucial, and its performance directly affects the transfer performance of the system.

In [7], a class $\Phi_2$ inverter for MCR-WPT system was proposed, which realized zero voltage switching (ZVS), zero derivative of voltage at switching and reduced the loss. However, due to the single-switch structure, it is not suitable for high-power systems because of the high voltage pressure. In [8], a multi-phase parallel inverter topology was proposed, which could easily expand the output power. However, the circuit was complicated, and the influence of parasitic parameters was not considered. In [9-10], several high frequency inverter design methods using half bridge topology were presented. However, the consideration of high frequency ringing due to parasitic elements was lacked.

The parasitic elements in the high-frequency inverter circuit were mainly constituted by parasitic capacitance and parasitic inductance in the switching device, and stray inductances of the connection wires. The parasitic ringing in the circuit will not only affect the voltage and the current across the switching devices, but also cause switching loss and conduction loss. Furthermore, the ringing in the power loop also generates electromagnetic interference (EMI) noise which will affect the driver circuit, thereby affecting the stability of the system [11]. In [12], the effect of the parasitic inductance and the parasitic capacitance in the inverter was analyzed. The control method of the inverter which reduced the influence of the parasitic parameters was proposed. However, the research on PCB design was lacked. In [13], the effects of package parasitic inductance on the switching characteristics of the device were analyzed. The GaN HEMT simulation model was built to provide theoretical support for the package optimization of switching devices. However, this paper only provided a method to reduce the parasitic inductance by the switching device package optimization.

In order to improve the performance of the inverter at high frequency, many efforts have been made to improve device characteristics and packaging. Advanced packaging techniques improve device performance by reducing package parasitic inductance [14-15]. However, the gains in device performance have slowed as the technology reaches its theoretical limit, and the package improvements are limited by the inherent trench structure at higher voltages. Therefore, the PCB layout becomes another key factor limiting the performance of the inverter. A good layout can effectively reduce parasitic elements in the inverter and improve circuit performance. Literature [16] proposed a method to analyze the effect of parasitic elements on PCB layout, and simulated the influence of PCB layout on converter performance. However, the paper only predicted the influence of PCB parasitic elements on the actual circuit performance, and did not propose the related improvement method of PCB layout. Using a ferrite bead to reduce the influence of the parasitic inductance was mentioned in [17]. However, the power loss on the ferrite bead will be high at high frequency and high power condition. There have been research efforts to reduce the parasitic elements in circuits [18].

This paper analyzes in detail the influence of the parasitic elements on the inverter and the reason of the ringing generated. The influence of PCB layout on circuit parasitic elements are studied, and the advantages and disadvantages of the conventional PCB layout are analyzed. Furthermore, an optimized PCB layout of the inverter is proposed, which reduces the parasitic inductance in the circuit. The simulation and experiment results show that the optimized PCB layout significantly decreases the parasitic elements in the inverter and suppresses the ringing in the circuit.

The remains of this paper are organized as follows. Section II initially introduces the influence of the parasitic elements on the inverter and the reason for ringing in the inverter. Section III proposed an optimized PCB layout, and the conventional layout and optimized layout are compared. The performance of conventional layout and optimized layout are simulated and tested in section IV.

II. EFFECT ANALYSIS OF PARASITIC ELEMENTS

The topology of the high-frequency inverter circuit with parasitic elements is depicted in Fig. 1.

![FIGURE 1. The topology of high-frequency inverter with parasitic elements.](image)

The package parasitic elements in the MOSFET include the gate-source capacitances $C_{gs1,2,3,4}$, the gate-drain capacitances $C_{gd1,2,3,4}$, the drain-source capacitances $C_{ds1,2,3,4}$, the common source inductances $L_{s1,2,3,4}$, and the drain inductances $L_{d1,2,3,4}$. In addition, $R_{g1,2,3,4}$ are the gate drive resistors, $L_{g1,2,3,4}$ are the gate drive inductances, $L_{c1,2,3,4}$ are the stray inductances of the connection wires between MOSFETs. $L_{c5,6}$ are the stray inductances of the connection wires from MOSFETs to the input capacitor. $L_{c7,8}$ are the stray inductances of the connection wires from the input capacitor to the DC source. The input capacitor acts as an input filter that prevents high-frequency current comeback to the DC source, thus eliminating the effects of $L_{c7}$ and $L_{c8}$. $R_{ac}$ is the transmitting coil series equivalent resistance, $L_{t}$ is the transmitting coil inductance, and $C_{l}$ is the series resonant compensation capacitor.
The common source inductance $L_s$ is located in both the drain-source current path and the gate driver loop. Thus, it directly affects the driving speed of the switching device [19]. The gate drive current when the switch is turned on is given by (1).

$$I_g = \frac{V_{\text{driver}} - V_{gs} - V_{Ls}}{R_g} = \frac{V_{\text{driver}} - V_{gs} - L_s \frac{di}{dt}}{R_g}, \tag{1}$$

where $I_g$ is the gate drive current, $V_d$ is the gate drive voltage, $V_{gs}$ is the gate-source voltage, and $V_{Ls}$ is the common source inductance voltage which equals to $L_s \frac{di}{dt}$. $R_g$ is the gate drive resistor. It can be known from (1) that when the common source inductance increases, the gate drive current will decrease, which not only affects the driving speed of the switching, but also affects the optimal switching condition. Furthermore, the short-circuit problem may happen, and causes two switches in the same bridge arm to turn on simultaneously, making the inverter unstable.

$L_{\text{loop}}$ is the power loop inductance. It includes the drain inductances in the MOSFET and the stray inductances of the connection wires, which affects the switching speed and drain-source voltage [20]. The output capacitance of the MOSFET is equal to $C_{oss} = C_{ds} + C_{gs}$. The turn-on and turn-off process of the MOSFET is accompanied by the charge and discharge of the output capacitors at both ends, as depicted in Fig.2.

![FIGURE 2. Charging and discharging process of output capacitor.](image)

When the bottom MOSFET is switched from the off state to the on state, and the top MOSFET is switched from the on state to the off state, the output capacitor $C_{oss2}$ is short-circuited and starts to discharge. The output capacitor $C_{oss1}$ is charged. This will result in high $\frac{di}{dt}$, $\frac{dv}{dt}$, and high spike current.

The equivalent circuit of the inverter is depicted in Fig.3 when switch $Q_1$ and $Q_4$ turn on, $Q_2$ and $Q_3$ turn off. The power loop is represented by the continuous line and the ringing loop is represented by the dash line. During the switching transition, the voltage across the power loop inductance is shown as (2), and the drain-source voltage of the MOSFET is shown as (3).

$$V_{\text{loop}} = L_{\text{loop}} \frac{di}{dt}. \tag{2}$$

$$V_{ds} = V_{in} + V_{\text{loop}}. \tag{3}$$

where

$$L_{\text{loop}} = L_{c5} + L_{d1} + L_{s1} + L_{c2} + L_{d2} + L_{s2} + L_{c6}. \tag{4}$$

![FIGURE 3. Equivalent circuit of the inverter.](image)

Therefore, the high peak voltage is generated at the MOSFET. The charging and discharging process of the output capacitance derives the energy flowing between the parasitic inductance and the output capacitance, forming the ringing voltage and ringing current with a high peak.

The ringing current is obtained as (5). Furthermore, the drain-source voltage of MOSFET when it turns on is shown as (6), and the gate-source voltage of MOSFET which is affected by the ringing current is shown as (7).

$$i_{\text{ringing}} = C_{oss} \frac{dv_{ds}}{dt}. \tag{5}$$

$$V_{ds-\text{on}} = R_{ds-\text{on}} (I_L + i_{\text{ringing}}). \tag{6}$$

$$v_{gs} = L_s \frac{di_{\text{ringing}}}{dt}. \tag{7}$$

It can be known from (3), (6), and (7) that the ringing voltage increases the effective voltage across the MOSFET. Thus, the switching loss and the voltage pressure of the switching are increased. The ringing current will cross through the drain of the MOSFET and flow into the transmitting coil to cause the skin effect, which increases the conduction loss and affects the efficiency of the inverter. In addition, the high-frequency ringing current will affect the gate drive pulse, which makes the inverter unstable and cannot work in the optimal operation condition. It can even cause two switches in the same bridge arm to conduct at the same time, burning the switch. The ringing current will also generate the EMI noises, which will affect the driving circuit and other devices [20].

Based on the above analyses, the charge and discharge of the output capacitance in the switching transistor and the parasitic inductance in the circuit are the main causes of the high peak ringing current and the ringing voltage in the high-frequency ringing current will affect the gate drive pulse, which makes the inverter unstable and cannot work in the optimal operation condition. It can even cause two switches in the same bridge arm to conduct at the same time, burning the switch. The ringing current will also generate the EMI noises, which will affect the driving circuit and other devices [20].

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frequency inverter, which increases the conduction loss of the inverter and have a great impact on the stability and efficiency of the inverter. Therefore, reducing the parasitic inductance in the circuit is of great significance for improving the stability of the inverter.

The common source inductance $L_s$ is mainly controlled by the package inductance of the device. Thus, it is closely related to the packaging and the performance of the device. The power loop inductance $L_{loop}$ is mainly controlled by the package inductance of the device and the circuit layout. The switching device of this paper uses SiC MOSFET C3M0065100K. The MOSFET has high switching frequency, good package performance, and the package inductance is significantly lower than that of the Si material MOSFET. Therefore, the common source inductance, associated with the package inductance is no longer the main reason for the parasitic losses in the inverter. The power loop inductance, controlled by the PCB layout now becomes a major contributor to the loss. Therefore, it is shown that the PCB layout of the high-frequency inverter circuit has a critical effect on the high-frequency performance of the inverter. The excellent PCB layout can effectively reduce the parasitic inductance in the circuit and improve the operation performance of the circuit. In the following, an optimized inverter circuit PCB layout is presented, and compared with the conventional PCB layout in terms of performance.

III. PCB LAYOUT DESIGN OF THE INVERTER

SiC MOSFET has higher switching frequency and lower package parasitic inductance. Therefore, the PCB layout of the inverter is critical for reducing the parasitic inductance and improving the performance of the inverter. The high-frequency ringing loop formed by the parasitic inductance and the parasitic capacitance in the circuit is shown by the dash line in Fig. 1. The high-frequency ringing current and ringing voltage not only reduce the operating efficiency of the inverter, but also affect the stability. The parasitic inductance is related to the width and length of the connecting wire of PCB. The shorter the length of the connecting wire, the smaller the value of the parasitic inductance. The larger the width of the connecting wire, the smaller the value of the parasitic inductance [21-22]. In addition, this paper not only directly reduces the parasitic inductance in the PCB circuit, but also indirectly reduces the parasitic inductance by reducing the influence of ringing caused by parasitic parameters through reasonable layout. To make the area of the ringing loop reduced, to decrease the impact of the ringing, can be equivalent to reduce the parasitic inductance. Therefore, when designing the PCB layout, reducing the area of the ringing loop, decreasing the length of the connecting wire, and increasing the width of the connecting wire are the crucial objective.

A. CONVENTIONAL PCB LAYOUT

The conventional PCB layout places all MOSFETs in a single line on the same side. The input capacitor is placed in the same layer as MOSFETs in close proximity to minimize the area of the high frequency ringing loop, thus reducing the parasitic inductance. In this layout, the power loop only flows on the top layer of the PCB and is parallel to the plane of the board. Thus, the power loop parasitic inductance $L_{loop}$ is independent of the board thickness. The basic layout of the circuit and the high-frequency ringing loop are depicted in Fig. 4. The high-frequency ringing loop is highlighted in red.

This layout reduces the parasitic inductance in the circuit by reducing the area of the ringing loop. At the same time, this layout also uses the inner layer of the board as a shield. The magnetic field generated by the high-frequency ringing current induces a current in the shield layer, opposite to the direction of the ringing loop current. The current in the shield generates a magnetic field to counteract the original ringing loop magnetic field, which is equivalent to the reduction in the parasitic inductance, thereby effectively weakening the influence of the ringing current.

For the conventional PCB layout, the parasitic inductance of the power loop is independent of the thickness of the board. Since the inner layer is selected as the shielding layer, the $L_{loop}$ is related to the distance between the top layer and the inner layer. However, when the frequency and the power of the circuit are high, additional losses will occur in the shield, which will affect the efficiency.

B. OPTIMIZED PCB LAYOUT

The optimized PCB layout proposed in this paper is depicted in Fig. 5. As shown in Fig. 5(a), the MOSFET is placed in an H-shape, and the MOSFETs of the same bridge arm are placed on the same side. Thus, compared with the conventional layout, the H-shaped layout reduces the interference between different driving circuits due to the compact placement of switching devices, thereby reduces EMI noise between different bridge arms under high frequency operating condition, and improves the performance of the MOSFET. This also improves the stability of the inverter. The input capacitor is placed in the middle distance between the MOSFETs, with the positive input terminals located next...
to the drain connections of the MOSFET, which minimizes the trace length of the ringing loop. The influence of the parasitic parameters is further weakened. At the same time, the optimized layout is not a simple two-layer board, but a four-layer board structure. It uses the inner layer as the current loop. As shown in Fig.5 (b), the high-frequency loop is highlighted in red. The layout uses the inner layer to act as the return path for the current, directly underneath the top layer current loop. Because the distance between the top layer and the inner layer is close, the area of the ringing loop is smaller than the conventional layout. Therefore, this layout reduces the parasitic inductances by minimizing the physical size of the ringing loop, and the parasitic inductance is independent of board thickness. Furthermore, the field self-cancellation method is used to reduce the parasitic inductances. The ringing current is opposite to the current in the inner layer. Thus, the magnetic field is generated in opposite direction. In turn, the magnetic fields cancel each other out. As a result, the parasitic inductances will be reduced.

In addition, the layout of the driver modules of the two PCB designs presented in this paper are identical to ensure that the common source inductance \( L_s \) and the gate inductance \( L_g \) remain constant. And the driver module is close proximity to the MOSFET gate to minimize the common source inductance and the gate inductance. Therefore, through the layout optimization of the PCB, the effect of the parasitic inductance can be decreased, and the interference of other factors in the circuit is eliminated. The features of the conventional and the proposed optimized layout are compared in Table 1.

In summary, the optimized PCB layout proposed in this paper has the following advantages:

1) The area of ringing loop is minimized, thereby reducing the parasitic inductance.
2) The parasitic inductance is independent of the board thickness.
3) It weakens the EMI noise between different bridge arms of the inverter and improves the stability of the inverter.
4) The board trace length is as short as possible, and the trace width is as wide as possible, which reduces the conducting power loss.
5) Using the magnetic field self-cancellation method to reduce the influence of the ringing current, which can be equivalent to reduce the parasitic inductance.
6) Using the inner layer as the return path of the current, no shield layer is needed, thus avoiding the extra loss caused by the shield layer under the high-frequency operating condition.

IV. SIMULATION AND EXPERIMENT

A. SIMULATION ANALYSIS

In order to verify the feasibility of the presented PCB design, this paper uses Ansoft Q3D Extractor for simulation, and the PCB simulation models are depicted in Fig.6. The PCB models are imported into Ansoft Q3D Extractor. And setting the simulation working frequency to 900 kHz to extract the parasitic inductance in the PCB board. The simulation results are depicted in Table 2.

The simulation results show that the parasitic inductance in the conventional layout circuit is 336nH, and the parasitic inductance in the optimized layout circuit is 47nH. The voltage across the drain-source during switching is [21]

\[
V_{ds} = V_in + \frac{V_0}{\sin\varphi_1} e^{-t_4/\omega_r} \sin(\omega_r t - \varphi_1) = V_{in} + V_{ringing},
\]

where \( t_4 = \frac{2L_{loop}}{R_{diss}+R_{ds-on}} \), \( \omega_r = 2\pi f_r \), \( V_{in} \) is the input DC voltage, \( V_0 \) is the voltage across the output capacitor, \( V_{ringing} \) is the ringing voltage, and \( f_r \) is the ringing frequency. It can be seen from (8) that the parasitic inductance in the circuit has a great influence on the amplitude of the ringing voltage, and the drain-source voltage is affected as well.

The output capacitance of the switching device \( C_{oss} = 0.06pF \) can be got by consulting the data sheet of the MOSFET C3M0065100K. Using data and formulas obtained from

<table>
<thead>
<tr>
<th>Features</th>
<th>Conventional layout</th>
<th>Optimized layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>Induction independent of board thickness</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Field self cancellation</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Shield layer</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Weakening EMI noise</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### TABLE 1. Features of Conventional and Optimized Layout.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Conventional layout</th>
<th>Optimized layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency ( f/kHz )</td>
<td>900</td>
<td>900</td>
</tr>
<tr>
<td>( L_{loop}/nH )</td>
<td>336</td>
<td>47</td>
</tr>
</tbody>
</table>

### TABLE 2. Simulation Results.
The ringing frequency of the conventional layout and optimized layout can be obtained by (9). They are derived as follows: 

\[ f_{r_1} = 35 \text{MHz}, \quad f_{r_2} = 94 \text{MHz}. \]

The lower the ringing frequency of the parasitic elements in the circuit, the more easily the harmonic components in the circuit excite the ringing. Therefore, the current flowing through the MOSFET has a high peak, and the high peak voltage across the drain-source, the switching loss will be very high. While the output voltage waveform will excite harmonics. When the ringing frequency is high, since the ultra-harmonics content in the circuit is successively decreased, ringing does not happen easily, and thus the influence on the circuit is relatively small. The simulation results show that the optimized layout presented in this paper can effectively reduce the parasitic inductance in the circuit, and weaken the influence of the ringing on the circuit.

**B. EXPERIMENT RESULTS**

In order to verify the excellent performance and to design feasibility of the above optimized PCB layout, the experimental platform of the MCR-WPT system was built as depicted in Fig.7

The experimental MCR-WPT system was built with the C3M0065100K MOSFET of CREE Company [23] as the inverter switching devices. The max allowable drain-source voltage is 1000V. The max allowable drain current is 35A, and it has high-speed switching frequency. Thus, it can meet high power density and high frequency requirement of the MCR-WPT system. Other components of the system include a DC input power, an auxiliary power, a DSP28335 module, an inverter, a transmitting coil, a receiving coil, series resonance compensation capacitances, and load resistances.

Both coils are wound with an enameled wire of 2.5 mm in diameter and have a diameter of 20 cm. The frequency of the system is 900 kHz. The inductance and internal resistance of the two coils are measured by the network analyzer Keysight E5061B. The series resonance compensation capacitor is calculated by using the inductance value. The detailed parameters of the system are depicted in Table 3.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
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<tbody>
<tr>
<td>V_{DC} /V</td>
<td>24</td>
</tr>
<tr>
<td>L_1 /µH</td>
<td>2.76</td>
</tr>
<tr>
<td>C_i /nF</td>
<td>10</td>
</tr>
<tr>
<td>R_{a1} /Ω</td>
<td>0.97</td>
</tr>
<tr>
<td>R_{ds-on} /mΩ</td>
<td>65</td>
</tr>
<tr>
<td>L_2 /µH</td>
<td>2.76</td>
</tr>
<tr>
<td>C_2 /nF</td>
<td>10</td>
</tr>
<tr>
<td>R_{a2} /Ω</td>
<td>0.97</td>
</tr>
<tr>
<td>R_L /Ω</td>
<td>3.3</td>
</tr>
<tr>
<td>f_s /kHz</td>
<td>900</td>
</tr>
</tbody>
</table>

In order to compare the performance of the conventional PCB layout and the optimized PCB layout proposed in this paper, two inverter boards are created: the circuit board 1 is...
the conventional PCB layout, and the circuit board 2 is the proposed PCB layout in this paper. All of boards are made from the same type of copper board and all of devices using on each board are the same. The above two boards are respectively tested as inverter circuit of the MCR-WPT system to verify the feasibility of the proposed design. The gate-source drive voltage of MOSFET, the drain-source voltage of MOSFET, and the output voltage of the inverter are measured by the oscilloscope probe, and the Current Transformer KEYSIGHT 1147B is used to measure the output current of the inverter. The measured voltage and current are input to the Oscilloscope KEYSIGHT MSOX2024A, in which the data for the waveforms could be displayed and saved. The MATLAB is utilized to perform FFT analysis for the gate-source drive voltage data, the drain-source voltage data, and the output voltage data of the inverter.

The FFT analysis is performed on the gate-source drive voltage data of the conventional layout and the optimized layout, where the fundamental frequency is 900kHz, the max frequency is 10MHz. The results are depicted in Fig.8. Fig.8(a) shows the gate-source drive voltage of the conventional layout. Fig.8(b) shows the gate-source voltage of the optimized layout. FFT analysis results show that the total harmonic distortion (THD) of the conventional layout is 40.88%, and the THD of the optimized layout is 39.78%. The harmonic content of the optimized layout is less than that of the conventional layout. The harmonic content of the gate-source drive voltage in two PCB layouts is compared to indirectly indicate that the high frequency ringing generated by parasitic parameters will cause EMI interference to the driving circuit. The FFT analysis results can verify that due to the proposed optimized layout, the EMI noise between the bridge arms is weakened, the gate-source drive voltage contains less harmonic, and the switching stability is higher.

The drain-source overshoot voltage is measured by the oscilloscope probe, and the output current rise time of the inverter is measured by the current transformer. The measured results of two layouts are depicted in Fig.10 and Fig.11. Fig.10(a) shows the drain-source voltage and the output current rise time of the conventional layout, and Fig.10(b) shows the drain-source voltage and the output current rise time of the optimized layout. By comparison, the voltage peak across the MOSFET is reduced. Thus, the switching loss is reduced, which indicates that the optimized layout can effectively reduce the influence of the parasitic inductance in the circuit. The drain-source overshoot voltage of the conventional layout and the optimized layout are depicted in Fig.11(a) and Fig.11(b), respectively.
The parameters measured by the experiment and the parasitic inductance values of the power loop calculated are depicted in Table 4.

It is depicted in Table 4 that, compared with the conventional layout, the power loop inductance in the optimized layout is reduced by 87.8% and the drain-source overshoot voltage is reduced by 87.7%.

The FFT analysis is performed on the drain-source voltage data of the conventional layout and the optimized layout. In Fig. 12(a), the fundamental frequency is 35MHz, and the max frequency is 500MHz. In Fig. 12(b), the fundamental frequency is 102MHz, the max frequency is 1GHz. It is depicted in Fig. 12(a) that the ringing frequency in the conventional layout inverter is 35MHz, and its influence on the circuit is serious. A high voltage peak is generated at both ends of the MOSFET, which excites harmonics and affects the operating state of the switch. It is depicted in Fig. 12(b) that the ringing frequency in the optimized layout inverter is 102 MHz. However, since the frequency is high, it is difficult to form ringing, and the influence on the circuit is slight, and the operating state of the switch is perfect.

Compared with the simulation results, the power loop inductance measured by the experiment is lower, and the ringing frequency is slightly higher. This is because in the simulation, the effect of the shield layer and the magnetic self-cancellation on the parasitic inductance does not be simulated; the parasitic inductance of the probe also causes errors in the measurement results. However, the conventional PCB design and the optimized PCB design proposed in this paper are simulated and tested under the same condition. Therefore, the error does not affect the comparison between the proposed design or the conventional design.
Through the above simulation analysis and experimental results, it can be verified that the proposed PCB layout design method is effective in reducing the parasitic inductance in the circuit, weakening the EMI noise in the drive circuit, reducing the overshoot voltage, improving the performance and the stability of the inverter, and enabling the inverter to provide higher quality electrical energy.

V. CONCLUSION

Under high frequency operating conditions, the parasitic inductance and the parasitic capacitance have a serious impact on the performance of the inverter due to generating ringing voltage and ringing current in the circuit. In this paper, the effect of the PCB layout of the inverter on the parasitic elements is studied, and the limitations of the conventional PCB layout are overcome. An optimized PCB layout method based on SiC MOSFET is presented. Compared with the conventional PCB layout, the proposed layout has the following advantages:

1) The power loop inductance $L_{\text{loop}}$ is reduced by 87.8% compared to the conventional PCB layout.
2) The overshoot voltage is reduced by 87.7% compared to the conventional PCB layout.
3) The parasitic inductance is independent of the board thickness. Using field self-cancellation method to reduce the parasitic inductances. The inner layer is not required as a shield layer. Thus, no additional loss occurs.

4) The MOSFETs adopts the H-type layout, which reduces the EMI noise of the drive circuit and improves the performance and the stability of the inverter.

5) The effect of ringing voltage and ringing current is weakened.

With the PCB design studied in this paper, the advantages of SiC MOSFET switching technology are improved, providing higher voltage operation capability and a more stable power for the MCR-WPT system.

REFERENCES


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