A High Spectral Efficiency Receiver at 57-66 GHz Using 65nm-CMOS in LTCC Package with Polarization MIMO

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ABSTRACT This paper presents a dual-polarization antenna with high spectral efficiency for transmission application distance at 60 GHz. The dual-polarization antenna is integrated with the receivers through flip chip on the LTCC substrate at 60 GHz. The receiver front-end composes of a low noise amplifier and demodulator fabricated in 65-nm CMOS process. The conversion gain is higher than 14 dB and the noise figure is lower than 6 dB from 57 to 66 GHz. The total data rate of the proposed system’s spectral efficiency is up to 12 bit/s/Hz for wireless measurement and the EVM is below 5.5 %.

INDEX TERMS Dual polarization Antenna, Millimeter-Wave, Low Temperature Co-fired Ceramics, 5G, MIMO.

I. INTRODUCTION

Recently, 5G millimeter-wave (mm-wave) communication has been viewed as a potential solution to meet the demands of high throughput wireless communications within a limited available spectrum. The characteristic of fast decay in mm-wave also satisfies the requirement for frequency reuse at concentrated metropolitan regions. Interests in the development of 60-GHz transceivers (TRX) have increased in recent years because of their promising indoor/outdoor MIMO applications [1], [2].

There are several techniques that have been demonstrated to enhance the throughput of the receiver. For instance, a single polarization array system [3] is proposed to enhance the throughput. Its data rate reaches 7 Gbps with 64-QAM and its spectral efficiency is 6 bit/s/Hz. A 16-element TRX with polarization diversity is realized in [4], with a total data rate of 4.6 Gbps using 16-QAM. To further increase the throughput and special efficiency, dual-polarization techniques in [5] achieved 27.8 Gbps with a 16-QAM scheme, and its spectral efficiency is around 8 bit/s/Hz. Another way for better throughput is channel bonding technology. The maximum throughputs of 4-channel bonding reach 28.16 Gbps with spatial efficiency of 4 bit/s/Hz using 16-QAM [6], and a 42.24 Gbps with spatial efficiency of 6 bit/s/Hz using 64-QAM [7].

The schematic of the proposed dual-polarization receiver for 5G communication is depicted in Fig. 1. By using the vertical-polarization (V-polarization) and horizontal-polarization (H-polarization) simultaneously, it makes the available spectrum more efficient and also increases the throughput. Multiple antennas are widely used in MIMO systems. In modern communication application, the environments inevitably get more complicated, which make multi-path inference one of the more severe issues. If the isolation between H- and V-polarization is not enough, transmission quality will be degraded [8], [9]. The antenna isolation between H- and V-polarization is around 20 dB in [5] and 15 dB in [4] under 16-QAM. Therefore, employing a high isolation dual-polarization antenna while designing dual-polarization systems are design strategies for 5G mm-wave.

A mm-wave antenna-in-package solution for flip chip assembly based on low temperature co-fired ceramic (LTCC) technology has been reported in [10]. Fig. 1 presents a
The Ti–Au Sn–Au alloy is deposited onto the pads of the LTCC design for small size with good performance.

In this paper, the demonstration of a LTCC system-on-package (SoP) receiver integrating both a monolithic microwave integrated circuit (MMIC) and a dual-polarization antenna is presented. The designed and measured performance of this radio receiver and the LTCC SoP module will be discussed thoroughly in this paper.

The paper structure is as follows: The system integration of LTCC and CMOS as well as the system planning are introduced in Section II. The circuit component and design details are presented in Section III. The measurement results are exhibited in Section IV. Section V gives a brief conclusion to summarize the system performance.

II. RECEIVER DESIGN

The CMOS technology with antenna integration is evolving rapidly in recent years. When further integrating the antenna with CMOS technology, the chip area will inevitably increase due to the operation of the antenna. In addition, the radiation efficiency will also be affected as well because of the larger CMOS substrate loss. A fully integrated receiver with an antenna embedded in an organic substrate is reported in [11] and [12] and a receiver is reported in [13]. Therefore, the LTCC substrate with an embedded antenna is utilized with a flip-chip assembled CMOS in [14].

Since the LTCC process supports multilayer dielectrics, vertically embedded passive elements are possible and suitable for this process. For the fully integrated application, a small-sized antenna with dual-polarization is embedded in LTCC. Since the thickness of an LTCC substrate is around 1 mm, it is possible to embed an antenna at 60 GHz aside the LTCC substrate in the vertical direction. With the multilayer dielectrics in the LTCC, the dual-polarization antenna can be realized by stacked vias. End-fire radiation can also be realized with a small footprint that is suitable for implementation. The end-fire radiation at 60 GHz can be used for a wireless file transfer system as shown in [15].

The standard LTCC process usually does not allow the metal width and spacing to be smaller than 100 μm. Therefore, the post process for finer metal traces is developed on LTCC for a microstrip line in the couplers and flip-chip bumps. LTCC fabrication and post process flow has been depicted in many previous reports [16]. The relative dielectric constant of LTCC is 7.8 with a loss tangent of 0.009. The material of the bump is Cu, while Sn is used for the adhesion layer during the die-to-LTCC assembly procedure. The minimum linewidth of this process is about 20 μm.

The cross-section view of a 60-GHz receiver is shown in Fig. 2. The dual polarization antenna is vertically embedded in an LTCC design for small size with good performance. The Ti–Au Sn–Au alloy is deposited onto the pads of the CMOS chip to increase the top metal thickness for a more reliable assembly process. The size of the bump is 30 μm × 30 μm with a height of 27 μm. The circuit model for flip-chip interconnects can predict scattering parameters up to 100 GHz.

The 14 layers of LTCC are adopted to integrate the dual-polarization antenna system. Layers 1-to-8 are used for flip chip routing whereas layers 9-to-14 are served as redistribution layers (RDL). The dual-polarization antenna pattern is designed at the first layer while the eighth layer is used as a group plane. The bumps of the CMOS pads can be connected with the antenna through flip chip. In addition, by effectively using the vias between different metal layers, the RDL routing can planned without sacrificing area efficiency as shown in Fig. 2.

In the system design level, the proposed dual-polarization receiver is composed of a dual-polarization antenna, a passive mixer, and an LNA. Good isolation of a dual-polarization antenna reduces the multi-path interference and leads to high spectral efficiency. Furthermore, when increasing the quality of the transmission signal, having better linearity and less power consumption of the system are also important issues for the receiver. In order to increase linearity and reduce power consumption, the direct down receiver also includes a sub-harmonic passive mixer and LNA with linearizer. While the sub-harmonic passive mixer provides good linearity, the negative gain causes the system’s third-order intermodulation (IM3) to no longer be dominated by the mixer, but by the LNA, so an LNA linearizer is needed to improve the linearity of the system [17]. More details regarding the components of the proposed receiver will be discussed in the following sections.

A. ANTENNA

In wireless communication systems, antenna diversity methods are often used to make a system robust. In general, a diversity method utilizes several transmission paths that have different fading conditions. Proper combinations of the signals from these transmission paths can alleviate the fading effect and improve transmission reliability. Antenna diversity is a diversity method that uses two or more antennas to improve the quality of a wireless system. While some of
the antennas encounter severe fading, others may still have satisfactory signals.

Antenna diversity may be realized in many ways, depending on the environment and the likely interferences. Three major ways to employ antenna diversity are space diversity, pattern diversity, and polarization diversity. Among them, polarization diversity is an efficient way to mitigate multipath effects. It usually consists of a pair of antennas with orthogonal polarizations (e.g., horizontal/vertical, left-hand/right-hand circular polarization). For the random orientations of transmitting antennas in electronic devices, by using two orthogonal polarizations, the performance of a wireless system against polarization mismatches that cause energy loss and fading may be enhanced.

Among the many kinds of antennas, patch antennas are very suitable for 60-GHz/mm-wave applications because of their low-profile characteristics such as their compact size, light weight, and planar structure [18]-[21]. Furthermore, patch antennas are often applied to polarization diversity applications [22]. For 60-GHz systems, polarization diversity has gained more and more popularity because it compensates for polarization mismatch due to the random orientation caused by users and alleviates the multipath effects. However, in the 60-GHz band, conventional patch antennas are physically small; in order to prevent the feeding network from affecting the radiation pattern the patch antenna, the feeding network must be designed more carefully, which makes their fabrication and design process
more challenging [23].

In this paper, an oversized dual-polarized patch antenna is proposed. The term “oversized” means that the proposed antenna is augmented to exploit the higher-order modes, unlike a conventional patch antenna that is operated at the fundamental mode. In other words, while the resonant length of a conventional antenna is a half-guided-wavelength, the length of the resonant edge may be multiple half-guided-wavelengths for an oversized antenna.

The proposed antenna not only realizes antenna diversity through a pair of orthogonal polarization, but it also mitigates the feeding problems. For 60-GHz applications, the error tolerance of fabrication processes may also be increased because of the enlarged size.

The most cost-effective solutions to mm-wave applications is to integrate antennas into silicons with MMIC [24]. Several techniques for gain and efficiency improvement have been proposed, including techniques using high resistivity silicon substrates, micro-machining [25], artificial magnetic conductor concepts [26], and using dielectric resonators [27]. In addition, on-chip antennas eliminate the need for external off-chip connection and packaging process. In [24], the measured gain of the inverted-F antenna on a silicon substrate was -19 dB and that of the designed quasi-Yagi was -12.5 dB. In [28], the measured gain of an on-chip planar dipole antenna was -8 dB without a focusing dielectric lens. However, these on-chip antennas usually suffer from low gain and poor radiation efficiency because of the lossy silicon substrate. On the other hand, the LTCC technology makes the integration of passive components such as antennas with MMIC in a single package possible without sacrificing gain and radiation efficiency. Passive elements can be placed at different layers and modules can be miniaturized by three-dimensional integration. LTCC also shows excellent characteristics of low dielectric constant and conductor loss.

The tiny size of the antennas at 60 GHz leads to lower fabrication error tolerance and less feeding problems. An oversized patch antenna operating at TM30 mode is presented in this chapter to solve this problem. Even though there are many other higher-order modes in a microstrip antenna such as TM30 and TM32 modes, the TM30 mode is more suitable for 60-GHz point-to-point communication due to the characteristic of broadside radiation [29], [30]. In addition, the gain of the proposed patch antenna using the TM30 mode is higher than the gain of a patch antenna at fundamental mode. More detailed analysis is provided and compared to simulation results as follows.

The proposed dual-feed dual-polarization patch antenna at 60 GHz that is fabricated on LTCC is shown in Fig. 2. By exploiting its TM30 mode, a high gain characteristic can be achieved [31]. Dual-polarization has been realized by using two orthogonal feeding lines [32]. At 60 GHz, the microstrip line was similar with the “non-oversized” patch antenna, resulting in feeding difficulties at 60 GHz and making the patch antenna to not be the main radiator. The enlarged antennas do not require complicated matching networks and can mitigate the effect from the feeding lines. The microstrip-T coupled feed has better isolation between the two ports than the direct feed. Furthermore, without destroying the boundary condition, the slots not only enhance the isolation but also increase the polarization purity [33].

To further increase the port-to-port isolation, a TM30 version microstrip-T coupled patch antenna based on [34] is proposed. The proposed dual-feed T-shaped microstrip feeding line coupled patch antenna operating at its TM30 mode is shown in Fig. 3 (a). The impedance matching is conducted through tuning the width T_w and length T_L of the T-shaped microstrip feed line. To achieve the best coupling, the gap T_g must be tuned carefully.

The isolation between two input ports of the TM30 mode patch antenna can be improved by etching a pair of slots. The same technique is performed again in this coupled-fed version. Under the same boundary condition, we can etch one more pair of slots on the same patch. As shown in Fig. 3 (a), two pairs of slots are etched to optimize the isolation.

The geometry and design parameters of the proposed antenna at 60 GHz band are shown in Fig. 3 (a). The dielectric substrate is the LTCC with an expected relative permittivity ε_r=7.8, loss tangent tanδ=0.009, and thickness h=0.357mm. The simulated S-parameters of the proposed antenna are plotted in Fig. 4. The -10-dB impedance...
The bandwidth of the proposed antenna is 2.16 GHz (3.7%). The isolation between the two input ports is better than 23 dB and up to 35 dB from 57-GHz to 62-GHz (<-30 dB at 60-GHz). With such high isolation, the signal leaks from the main path to another polarization will be extremely small. The simulated current distribution of the proposed antenna at its TM$_{30}$ mode while being excited at different ports is shown in Fig. 3 (b) and (c). The square patch antenna is fed by a pair of T-shaped microstrip lines that are perpendicular to each other, producing more linear current to enhance the isolation between the two ports.

The simulated radiation pattern at the frequency dip point is shown in Fig. 5. There are no side lobes because the spacing between two radiating slots is about 0.5 $\lambda_0$ in this 60-GHz LTCC antenna. The perturbation from the feeding lines could be the main reason that causes the deep null in the E-plane pattern. The simulated antenna gain and radiation efficiency are plotted in Fig. 6. The antenna gain of port 1 and port 2 is up to 9-dBi and the radiation Efficiency of port 1 and port 2 is up to 77%. The proposed antenna owns the features of high gain and isolation and has been applied to 60-GHz applications. It is easier to match the input impedance of the proposed antenna when compared to the conventional one, which may need additional matching networks. Also, the error tolerance in the LTCC fabrication can also be increased due to the enlarged size. This design strategy is promising in mm-wave applications.

B. LOW NOISE AMPLIFIER

A 57-66 GHz low noise amplifier (LNA) with built-in linearizers using 65-nm CMOS process have been designed, fabricated, and measured in [35]. Based on the proposed linearizer in [35], the suppression of IM$^3$ power is 14 dB, the noise figure (NF) is 4.5 dB, and flat gain is 24 dB around 60 GHz [35]. Fig. 7 shows the schematic of the LNA with the proposed built-in linearizer. It consists of two stages: one common source stage and one cascode stage. The device sizes of the common source stage and cascode stage are determined based on the trade-off between gain, linearity, stability, and ease of matching network design. In order to get more space for signal swing, the supply voltage of the cascade cell is selected as 2 V. The source degeneration is applied to the input stage to realize good noise performance and input return loss simultaneously. Due to the design consideration of noise figure and overall linearity, the cascode stage with a built-in linearizer is selected as the
output stage. The matching network is accomplished by thin-film microstrip lines and spiral inductors.

The chip measurements are taken via on-wafer probing. The comparison between simulated and measured S-parameters is presented in Fig. 8. The small signal gain is around 24 dB from 52 to 66 GHz, which agrees with the simulation result reasonably. Additionally, the performance of the input and output return losses between two circuits is similar. The measured noise figure is plotted in Fig. 9, which averages 4.8 dB from 54 to 67 GHz and is in good agreement with simulation. Moreover, it can be seen that adding the linearizer does not degrade the noise performance.

Since the linearity of the passive mixer is much better than that of the RF amplifier, is much greater than $OIP^3_1 \times G_2$, then the system $OIP^3_1 \times G_2$ can be approximated as $OIP^3_1 \times G_2$. Thus, the system linearity depends mainly on the RF amplifier. The key to improve the system linearity is to improve the linearity of the RF amplifier [17]. The measured input power of the interested tones versus the input power is plotted in Fig. 10. It reveals that the $IM3$ distortion power of the LNA is improved by 14 dB after linearization in the range of input power -40 to -33 dBm which means that the proposed method is effective in wide input power range.

C. MIXER

By using a double-balanced mixer that is combined directly, the sub-harmonic mixer is designed and fabricated in 65-nm CMOS technology. It only needs a differential signals pair to drive the mixer, which not only saves the chip area but also reduces the loss. The mixer achieves a conversion gain of -11 dB from 52 to 66 GHz with an LO power of 5.5 dBm [36]. The sub-harmonic IQ demodulator is designed in TSMC 65-nm 1P9M CMOS technology. The block diagram of the modulator is depicted in Fig. 11 (a). It is composed of a broadside coupler, two LO Marchand-baluns, and two sub-harmonic mixers. The schematic of the mixer is shown in Fig. 11(b).

To operate the mixer at a low supply voltage with low power consumption, a Marchand-balun-based RF stage is utilized to establish current coupling between the RF inputs and LO stage. Since there is no RF transconductance stage, the required supply voltage is decreased. In addition, the RF input impedance is lower, so the matching network is not needed in this mixer. The device size of the switching core was selected carefully. A larger size exhibits more nonlinear behavior which can achieve a higher conversion gain, but it also causes more parasitic effects due to its size that results in a more in narrowband performance. To attain the required bandwidth, the size of M1-M4 is chosen as $32 \mu m / 0.06 \mu m$, which is a 16-finger device with 2-μm unit finger length.

In a balanced mixer topology, it is necessary to feed differential signals into the switching core. The Marchand-balun-based RF stage is utilized for single-to-differential conversion in mm-wave design due to its wideband frequency response and compact size. A quadrature coupler is used to produce I and Q paths in the demodulator. The I/Q paths dominate the image rejection ratio (IRR) performance. Therefore, a 90° broadside coupler is adopted.
In this design, the broadband coupler is composed of two top metal layers (metal 8 and metal 9). The ground plane beneath the coupled lines is taken away to decrease the capacitance to the ground and increase the effective dielectric constant. In order to attain appropriate coupling, there is an offset between metal 8 and metal 9. Fig. 15 (b) shows the chip photo of the modulator. The chip size is 510 μm × 660 μm including the dc and RF pads.

The demodulator is measured via on-wafer probing for RF and LO ports. IF ports are connected to the PCB with bonding wires as output ports. The LO and RF signals are generated by two analog signal generators (Agilent E8257D). An LO power of 6 dBm is found to achieve the optimal conversion gain (CG). The measured conversion gain versus RF frequency with down-converted IF signals of 0.5-GHz at 5.5-dBm LO power is shown in Fig. 12. It can be observed that the value of the CG is consistent with simulation. In addition, the measured RF 1-dB bandwidth is from 52 to 66 GHz, which is wider than the simulation. The measured CG of the IF frequency is about 1.5 GHz and the measured IP1dB compression point is -2 dBm.

The measured 1-dB IF bandwidth is from 0.1 to 1.5-GHz and the measured input 1-dB compression point compression point (IP1dB) is -2 dBm, which are coherent with the simulation as plotted in Fig. 13. Due to the cancellation mechanism of the adopted structure, the isolation of LO and 2LO frequency is excellent and is above 50 dB within the bandwidth, as shown in Fig. 14. Benefitting from the high 2LO-to-RF post isolation, the proposed mixer has a better demodulation capability due to less dc offset.

**D. RECEIVER**
The demodulator is designed and fabricated in TSMC 65-
nm CMOS technology, and consists of an LNA and a
demodulator as shown in Fig. 15. The black-solid line in
Fig.16 indicates the measured CG and NF. The CG is 
higher than 13 dB and the NF is lower than 6 dB from 57 to 66 GHz.

The measured CG versus LO power is the red-solid line. Fig. 16 shows that the CG is around 5 dB with LO power from 4
to 6 dBm. The measured CG versus RF frequency is shown in Fig. 17. Based on the results from Fig. 16 and Fig. 17, the LO power can be decided to achieve sufficient CG among the frequency of interest.

III. MEASUREMENT

A. ANTENNA MEASUREMENT

The E-band antenna measurement is still challenging due to the smaller antenna size. The radiation pattern is vulnerable to the measurement carrier. For instance, while using probes to feed the antenna, the probe itself is easily affected by other

FIGURE 19. Simulated and measured radiation pattern of the proposed antenna at different plane (a) V-polarization (b) H-polarization.

FIGURE 20. Measurement setup of IF power 330 to 30 degree for wireless testing.

FIGURE 21. The link budget of proposed receiver while corresponding angle equal to zero between transmitter and receiver.
surrounding metals that causes the measurement error for the antenna pattern [37]. To solve this problem, many published works for E-band antenna measurements are based on the near-field pattern to obtain a far-field pattern via Fast Fourier Transform (FFT). Although this approach can solve the near-field problem, the antenna still suffers from multi-reflection and quantization errors. Hence, we design a carrier for E-band antenna measurement to resolve this problem, as shown in Fig. 18. The pointer, device under test (DUT), and standard E-band horn antenna are placed at the locations a and b in Fig. 18, respectively. Since the operating frequency is 60 GHz, the distance should be larger than 10 wavelengths (60 GHz) to reduce the multi-reflection effect and ensure that the measurement scenario is far field. The carrier of the DUT can be rotated for pattern measurement at any angle. The KeySight signal generator is utilized to feed the proposed antenna (DUT) while the spectrum analyzer is used to capture the radiated power. With the aid of a carrier with rotational function, the power pattern of the proposed antenna can be obtained. Since the proposed antenna is dual polarization, the characteristics of each polarization are measured separately. Fig. 3 (a) shows the proposed dual-polarization antenna. Port 1 is set for V-polarization and port 2 is set for H-polarization.

The measurement results of the V-polarization at the XY and YZ planes has been normalized. The normalized power distribution from 330 to 30 degrees is shown in Fig. 19. The red line in Fig. 19 (a) is the result of V-polarization of port 1 whereas the blue line is for H-polarization of port 2. The power level of port 2 is 15 dB smaller than port 1 from 330 to 30 degrees at both XY-plane and YZ-plane, which indicates that a good isolation is achieved by the proposed dual-polarization antenna. Because the proposed antenna is designed to be as symmetrical as possible, the blue line (H-polarization) at port 2 in Fig. 19 (b) is the same as the red line (V-polarization) at port 1 in Fig. 19 (a). These results are also well matched to the simulated S-parameter ($S_{21}$).

**B. RECEIVER MEASUREMENT**

Fig. 1 illustrates the system block diagram of the proposed dual-polarization receiver. It can be divided into two parts,
one for V-polarization system (chip A) and the other for H-polarization system (chip B).

Fig. 20 shows the measurement setup for IF power measurement from 330 to 30 degrees. The AWG (Keysight M8190A) is used to generate the 64-QAM, 1-GHz OFDM modulation signals. The baseband signals are then up-converted to E-band. The E-band standard horn antenna is utilized to transmit the modulation signal. The received signals are down-converted to IF signals and are demodulated by PXA (KeySight series). As mentioned earlier, a carrier with a rotational function is utilized to measured the received power at different angles. Fig. 21 shows the system link budget while the relative angle between the transmitting antenna and the receiver system is 0 degrees.

The measurement setup of digital demodulation for wireless testing is shown in Fig. 22 (a). The digital I/Q source is generated by an arbitrary wave generator (AWG) and then up converted to V-band by the mixer module. The variable attenuator and power amplifier are used to provide adequate signal level for the wireless signal transmission. The LO source of the demodulator and mixer module are provided by the other signal generators. Finally, the demodulated baseband signal, I and Q, are fed into PXA signal analyzer (Keysight) to analyze the quality of high-speed digital demodulation. The link budget of the proposed receiver with a corresponding angle equal to zero between the transmitter and receiver is shown in Fig. 22 (b). It shows that the effect of the third-order modulation on the signal is much smaller than the noise floor. The signal to noise ratio (SNR) reaches

FIGURE 23. Simulated and measured radiation pattern of the proposed antenna (a) xz-plane (b) yz-plane

FIGURE 24. Measurement results of V-polarization with 64 QAM modulation constellation diagrams at 60 GHz.

(a) (b)

(a) (b)

FIGURE 25. Measurement results of H-polarization with 64 QAM modulation constellation diagrams at 60 GHz.

(a) (b)
25dB, which allows the proposed receiver to support 64-QAM modulation.

The measured IF power patterns of the dual-polarization receiver that has been normalized to be the maximum power from 330 to 30 degrees are presented in Fig. 23. Fig. 23 (a) shows the measured power pattern of a V-polarization system, which corresponds to the co-polarization of chip A. Since the isolation of the proposed dual-polarization system is not infinite, the signal leakage from a V-polarization to H-polarization system is inevitable, as shown from the cross-polarization of chip B. The red line in Fig. 23 (a) is the received signal at V-polarization whereas the blue line is the signal leakage. The power difference between the co-polarization and the cross-polarization is larger than 15 dB. When the H-polarization is matched with the co-polarization of chip B and the V-polarization is matched with the cross-polarization of chip A as shown in Fig. 23 (b), the red line becomes the received signal leakage at H-polarization while the blue line becomes the received signal. The power difference between the two polarizations in Fig. 23 (b) is larger than 15 dB. Due to the significant power difference between the co-polarization and cross-polarizations of the chips as shown in both Fig. 23 (a) and (b), it can be observed that both polarization systems have good isolation, which can reduce the interference between polarization systems.

Fig. 24 and Fig. 25 show that the measurement results of V- and H-polarization EVM with 64-QAM modulation constellation diagrams at 60-GHz are 5.1% and 5.4% respectively. These results imply that the proposed dual-polarization system is capable of 64-QAM, 1-GHz

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH MMW RECEIVER AROUND 60-GHz

<table>
<thead>
<tr>
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<td>28-nm CMOS</td>
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<td>LNA, Mixer Ant. (package)</td>
<td>LNA, Mixer Ant. (Package)</td>
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<td>LNA Mixer PLL Ant. (Horn)</td>
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<tr>
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<td>45 (array×16)</td>
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<td>*3.28</td>
<td>*1.09</td>
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*Without Integrated Antenna
bandwidth data transmission. The overall data rate for the proposed receiver is up to 12 Gbps.

The performance of this presented receiver is summarized in Table I with a comparison of some other state-of-the-art 60-GHz receivers. Benefitting from integrating the CMOS IC with the dual-polarization receiver antenna, the system can achieve a transmission distance of 0.5 meters with 44 mW power consumption, EVMs of less than 5.5 %, and a data rate of 12 Gbps using only one antenna.

IV. CONCLUSION
A dual-polarization receiver with low power and high spectral efficiency for half-meter application distance is proposed in this paper. The dual-polarization antenna is integrated with a receiver front-end through LTCC substrate. The dual-feed patch antenna with dual-polarization has been designed at a frequency of 60 GHz. The receiver is composed of a low-noise amplifier (LNA) and a demodulator in 65-nm CMOS process. By exploiting the TM$_{00}$ mode, a high-gain characteristic of 9 dBi can be achieved. The microstrip-T coupled feed is employed to obtain better isolation. To further increase the port-to-port isolation, a pair of slots is etched on the patch antenna.

The measured isolations of the dual-polarization antennas are both 20 dB. Both measured H-polarization and V-polarization measured antenna patterns indicate that the proposed dual-polarization antenna possesses high isolation as well. By integrating the proposed dual-polarization antenna with the RF front-end, the conversion gain of the proposed receiver system is higher than 14 dB and the NF is lower than 6 dB from 55 to 66 GHz. The measured EVM is below 5.5 % with a data rate of up to 12 Gbps. The proposed system shows a great potential for doubling the data rate by using two (V- and H-) polarizations within a single channel. By adopting the orthogonal characteristic of the proposed system, the channel as well as spectral efficiency can be increased.

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VI. REFERENCES

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