Minimizing the Jitter of Duty Cycle Distortion Correction Technology Based on Cross Point Eye Diagram Correction

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ABSTRACT Pattern jitter is a primary contributor to the increase of the bit error rate (BER) in high-speed communications, which occurs in large part due to duty cycle distortion (DCD). By considering DCD caused by transmission links and the distribution of jitter in DCD due to the pattern of the transmission link, this paper proposes a precise control method based on the cross point of the eye diagram to minimize the jitter associated with DCD and to effectively decrease the BER of high-speed digital communications. By capitalizing on the theoretical basis that the main form of DCD is the offset of the cross point of the eye diagram, the technology presented here reconstructs the pattern waveform by using a digital method and incorporates a time variable to precisely control the data edge position during the reconstruction process, thereby stabilizing the cross point at 50% to correct its drift. Accordingly, after fanning out the original pattern buffer and then passing two controllable delay lines with different delays through the buffer in a process that is driven by digital logic operation, the cross point of the waveform is reconstructed by changing the relative time delay of the two signals. As a result, the change in the position of the cross point of the eye diagram is transformed into the precise control of the relative time delay, minimizing the DCD jitter. The theoretical model is verified by experiments, indicating that this method can control the cross point of the non-return-to-zero (NRZ) pattern in the range of 30% to 70% under 3 Gbps with a resolution as great as 1%. Furthermore, this approach can solve the problem of cross point drift of the eye diagram and can significantly decrease the BER caused by DCD jitter.

INDEX TERMS Cross point of the eye diagram, pattern jitter, duty cycle distortion (DCD), bit error rate (BER).

I. INTRODUCTION
With the rapid development of communication systems and very large scale integration (VLSI) and considering that the data transmission rate has increased rapidly in recent decades, jitter has now become the bottleneck that limits the improvement of data transmission rates and lengths [1], [2]. Jitter is the deviation of a timing event of a signal from its ideal position [3]. Total jitter (TJ) mainly includes random jitter (RJ) and deterministic jitter (DJ). Deterministic jitter is composed of duty cycle distortion (DCD), intersymbol interference (ISI), period jitter (PJ) and bounded uncorrelated jitter (BUJ). Data-dependent jitter (DDJ) includes DCD and ISI. Jitter is the primary factor contributing to bit error [4], [5]. The most important contributor to the deviation of the cross point of the eye diagram of a signal from its ideal position is DCD, which refers to the deviation of the duty cycle of the signal relative to its normal value. There are several primary causes of DCD: the duty cycle of the signal sampling clock is different; the threshold of the signal decision level deviates from its ideal voltage value; and the rising and falling edges of the signal are not symmetrical [6]. For example, in high-speed communications, if the drive ability of the input/output buffer has more mismatches in the pull-up and pull-down, the cross point of the eye diagram may deviate, giving rise to jitter. As a result, this result leads to an increase in the BER [7]. Additionally, in the binary phase shift keying (BPSK) modulation system, because the signal amplitude of the input RF amplifier is low and fluctuating, the signal after the RF amplifier cannot satisfy the half-wave voltage
required by the phase modulator. As a result, the phase modulator, due to environmental changes and the effects of continuous high-frequency signals, among other reasons, causes the duty cycle of the modulated signal to change, which in turn leads to drift (upward or downward) of the cross point of the signal eye diagram. Accordingly, the eye sample point falls into the eye diagram template more easily, which eventually leads to an increase in the signal error rate, significantly affecting the quality of the communication [8]. Therefore, it is necessary to modify the cross point of the eye diagram to maintain the cross point at 50%, thereby minimizing the BER in the communication. Hence, our proposed solution to the problem of drift in the cross point of the eye diagram can improve the overall stability of the system.

Two methods are traditionally used to correct the deviation of the cross point of the signal eye diagram: one is to adjust the cross point of the output signal eye diagram by using an analog method. Usually, the capacitive load is added at the signal output end to change the slew rate of the signal, thereby changing the position of the cross point. To more clearly show the change in the slew rate of the rising and falling edges of the signal (rise time and fall time), a square wave signal was used to observe the change of the cross point of the eye diagram. Fig. 1(a), (b), and (c) show the cross point of the eye diagram of 30%, 50%, and 70% at 20 MHz using the analog method.

According to the experiment, this method can be used to better adjust the cross point of the eye diagram at a frequency of 50 MHz. When the frequency is higher than 50 MHz, the quality of the eye diagram is poor, which raises challenges in meeting the needs of signal processing efforts. The parasitic capacitance and the nonlinearity of the relationship between the capacitor charge, discharge time and current all contribute to these challenges. Furthermore, the applicable frequency range is low, and the quality of the output signal eye diagram is also undesirable. This combination of challenges creates significant difficulty in meeting the requirements of the current high-frequency applications.

The other method entails adjusting the cross point of the eye diagram by controlling the DC level of the zero crossing of the signal [9]. In this method, a bias tee is used to add the DC level. Even though a bias tee can correct the cross point of the eye diagram, nonetheless the experiment found that the cross point can only be corrected within a small range (when the cross point is in the range of 45% to 55%). Moreover, the noise of the DC component affects the quality of the output eye diagram. In addition, due to the limitation of the performance of the bias tee, this method is not suitable for low-frequency applications at the MHz scale. Fig. 2(a), (b), and (c) show the cross point at 46%, 50%, and 55% of the eye diagram using this method under 3 Gbps.
The method proposed in this paper can overcome the shortcomings of the two methods mentioned above. By precisely controlling the cross point, the jitter of the DCD and the BER of high-speed digital communication can be reduced. The method is applied to the rising and falling edges of the signal, which allows this method to add to the controllable fraction of the relative delay through the delay line. In this case, the waveform is reconstructed by using a digital method, thereby correcting the cross point of the eye diagram and reducing the bit error caused by the jitter of the DCD.

II. FUNDAMENTAL

A. THE RELATIONSHIP BETWEEN CROSS POINT AND BER

Eye diagram analysis is an important way to analyze the information in high-speed serial signal analysis. An eye diagram reveals important signal information, such as the time at which signal rise and fall occurs, as well as the signal overshoot, undershoot, ringing, duty cycle, jitter, noise, etc. An eye diagram can be used to measure the signal quality and signal integrity.

The ideal signal output cross point of the eye diagram is located at 50%. If the cross point of the eye diagram is higher than the ideal position, then the system will transmit too many 1-bits, and as a result, the signal will generate a bit error. If the cross point of the eye diagram is lower than the ideal position, then the system will transmit too many 0-bits, which also leads to an increase in the BER. This problem can also cause difficulty in extracting the frequency of the receiver signal frequency, which makes it impossible to synchronize the signals, further compounding synchronization loss. BER is the most basic measure of system performance, which is the ratio of the number of bit errors to the number of received bits. As the data rate exceeds 1 Gbps, a slight increase in the jitter or amplitude noise of the system has a far more significant effect on the BER [10].

As shown in Fig. 3, the signal integrity tolerances of the eye diagram, the jitter distribution at the cross point and the BER displayed by the bathtub curve are specified. In the eye diagram, multiple data levels and edge jumps are superimposed within the Unit Interval (UI) range, where a UI is the average time duration of a single bit or the reciprocal of the average data rate. The horizontal axis of the eye diagram represents time, and the vertical axis represents signal amplitude, which contains abundant information [11]; the BER is essentially the cumulative distribution function (CDF) of the total jitter probability density function (PDF) of the left and right cross points of the time interval, in which a bit error occurs. In Fig. 3, the time interval of interest is that to the right of sampling instant \( t_s \) for the left cross point, whereas that to the left of \( t_s \) is for the right eye crossing. Integrating the PDFs of both eye cross points, their respective time intervals produce the BER function [12]. The influence of the ISI and noise can be observed from the eye diagram, which reflects the overall characteristics of the digital signal, thereby estimating the system superiority and inferior. The jitter, overshoot and many parameters describing the eye diagram can be obtained according to the eye diagram, where the eye diagram can also analyze the influence of different jitter components on the signal, thereby analyzing the key factors that cause the jitter and then providing direction guidance for weakening the jitter, which further improves the performance of the system. The eye diagram is also the most basic prerequisite for understanding the BER in a link. The BER of the system depends on the sampling time and sample level of the data. Modern high-speed links generally have a certain BER and data transmission rate, which usually determines the amplitude of the noise and jitter that can be allowed in a link.

\[
\text{BER}(t_s) = \text{CDF}(t_s) = \frac{1}{2} \left[ \int_{-\infty}^{t_s} \text{PDF}_{\text{left}}(\Delta t) d(\Delta t) + \int_{-\infty}^{t_s} \text{PDF}_{\text{right}}(\Delta t) d(\Delta t) \right]
\]

B. THE RELATIONSHIP BETWEEN CROSS POINT AND DCD

The eye diagram can evaluate signal performance, in which the eye width and eye are introduced as key metrics. The cross point of a given eye diagram, that is, the percentage of the cross point of the eye diagram, is used to measure the relationship between the amplitude of the cross point and of the signal of the “1” level and the “0” level. In general, the logical “1” and logical “0” levels within 20% of the middle of the eye are selected, identifying the “1” level and “0” level positions. The levels of the different signals can be represented by different cross-proportional relationships. The cross point of a typical standard signal represents half the level of the signal. The cross point is calculated according to the vertical statistical center of the average. The proportional equation is as follows:
Cross point of the eye diagram percentage = [(Cross point level-“0” level) / (“1” level-“0” level)]×100%

This value can also be expressed as the percentage of the zero crossing as follows:

\[ C = \frac{P_{cr} - P_o}{H} \times 100\% \]  

(2)

where \( P_{cr} \) represents the level of the cross point, \( P_o \) represents a low level, and \( H \) represents the eye height. The percentage of the zero crossing can reflect the duty cycle of the signal, such that the percentage of the cross point is approximately 50% of the optimal value.

The cross point of the eye diagram percentage relationship can express the ability of different signals “1” and “0” to transmit signal quality, as well as the relationship between different signal width and cross point percentages. As shown in Fig. 4(a), when the cross point of the eye diagram percentage covers 30%, the duty ratio of signal “0” is greater than the duty cycle of signal “1”. As shown in Fig. 4(b), when the cross point of the eye diagram covers 50%, the duty ratio of signal “1” is equal to signal “0”. Finally, as shown in Fig. 4(c), when the cross point of the eye diagram covers 70%, the duty ratio of signal “1” is greater than the duty ratio of signal “0”.

As shown in Fig. 4(a), (b), and (c), the spectrum pattern simulation diagrams correspond to the trend of the pulse width duration as decreasing, constant and increasing, respectively. From the figure, it can be seen that the change of the pulse width significantly affects its spectrum.

\[ T = \text{the duration of an occurrence of a single logic-0 affected by DCD}, \]
\[ T_o = \text{the duration of a bit if it was not affected by DCD}, \]
\[ \Delta T_{\text{rise}}, \Delta T_{\text{fall}} = \text{the rise-time and fall-time of the signal}. \]

DCD can be expressed as the sum of two functions, as shown in the following equation:

\[ DCD = \frac{T_t}{T_i + T_o} - 0.5 + \frac{\Delta t_{\text{fall}} - \Delta t_{\text{rise}}}{2 \times T_{\text{bit}}} \]  

(5)

If the data rate is known, then \( T_t \) is known. The duration of an unknown number of logic-1 \( (T_{\text{e}}) \) can be measured between any rising edge and the immediately following falling edge [14], [15]. Thus, it can be shown that \( \text{dataDCD} \) is given by:

\[ \text{dataDCD} = 0.5 + \frac{T_{\text{e}} - T_{\text{bit}} \times \text{floor} \left( \frac{T_{\text{e}}}{T_{\text{bit}}} \right)}{2 \times T_{\text{bit}}} \]  

(6)

The distribution function of the jitter caused by DCD can be expressed as the sum of two functions, as shown in the following equation:

\[ J_{\text{DCD}}(x) = \frac{\delta(x - \frac{W}{2})}{2} + \frac{\delta(x + \frac{W}{2})}{2} \]  

(7)

where \( J_{\text{DCD}}(x) \) is the DCD probability density function (PDF), \( W \) is the peak-to-peak DCD magnitude, and \( x \) is the time displacement relative to the ideal time position. The two \( \delta \) functions represent the rising and falling edges of the signal. The magnitude of each \( \delta \) function is 1/2 because the equation assumes that there are equal numbers of rising and falling transitions in the transmitted signal [16], [17].

The PDF image of the DCD is shown in Fig. 5 [18].

**FIGURE 4.** Diagram of the effect of different duty cycles of signals on the spectrum and the cross point

**C. DCD CHARACTERISTIC ANALYSIS**

The DCD is the digital signal impairment that appears because all rising edges are delayed (or advanced) by the same value \( \Delta t_{\text{rise}} \) from the expected moment in time, and all falling edges appear delayed (or advanced) by the same value \( \Delta t_{\text{fall}} \) from the expected moment in time. Considering \( \Delta t > 0 \) for a delay and \( \Delta t < 0 \) for an advance in time, then:

\[ T_0 = T_{\text{bit}} - \left[ \Delta t_{\text{fall}} - \Delta t_{\text{rise}} \right] \]  

(4)

where \( T_0 \) = the duration of an occurrence of a single logic-1 affected by DCD,
precise delay adjustment part can generate precise relative delay, can reconstruct the pattern waveform by using a digital method and can precisely determine the relative delay control data position in the reconstruction process. The amount of relative delay is related to the size of the position where the cross point of the eye diagram has deviated by 50%. The output drive portion enhances the drive capability of the output signal. First, the signal input fanout buffer part can isolate the partial jitter of the upper stage and buffer the data reception, allowing the data of the fanout buffer part to pass through the digital precision delay adjustment part. If it is necessary to raise the position of the cross point, then the input data buffer must be fanned out, and as a result, the input into the digital precision delays the adjustment part. After passing two controllable delay lines with different delays, the original signal and the signal after the precision relative delay of the signal is given by “OR” digital logic operation after the output selection. As a result, the output is directed to the output drive section. The output drive section enhances the drive capability of the signal and generates the cross point at the desired position. Thus, the precise delay operation for the signal effectively reduces the cross point, as shown in Fig. 6(a). Similarly, the position of the cross point can also be reduced by precision relative delay and “AND” digital logic operation, as shown in Fig. 6(b).

The digital precision delay adjustment section is shown in Fig. 6(a) and (b) includes the relative delay adjustment, “AND” digital logic, “OR” digital logic and a 2:1 select data selector. The input of the relative delay adjustment is the output BUF_IN of the fanout buffer. After the relative delay through the two delay line outputs, which are used as “AND” digital logic and “OR” digital logic, the output of the “AND” digital logic and “OR” digital logic are used as the input to the data selector. The output of the data selector BUF_OUT is used as the input of the output drive section, and the data selector is the logic “1” selector. If the data is in the logic low to logic high transition, when the two delay lines produce a relative delay, the output of the other delay line remains at a low level due to the delay. Therefore, the inputs of the “AND” digital logic and “OR” digital logic are “logic low” and “logic high”. At this time, if the cross point is raised, the data selector is selected as logic high “1”, that is, if the “OR” logic is selected, then the output BUF_OUT is logic high, which is equivalent to pulse width widening, and the cross point of the eye diagram generated by the signal is shifted up. Similarly, the signal can be delayed, and the “AND” digital logic can be selected to realize the downward shift of the output signal eye diagram, thereby adjusting the signal cross point position.

To more intuitively analyze the principle of eye diagram cross point adjustment, Fig. 7(a) and (b) present a timing diagram for correcting 50% when the cross point is at 70% and 30%, respectively. As shown in Fig. 7(a), when the signal cross point changes from 70% to 50%, the input signal must pass the delay line variable relative delay $T_d$, and then the time variable precision control data edge position is added. As a result, the two signals are “AND” digital logic, and the pulse width of the signal is narrowed, so that the cross point is corrected to 50%. Similarly, as shown in Fig. 7(b), when the signal cross point of the eye diagram is corrected from 30% to 50%, it is also necessary to pass the input signal through the delay line variable relative delay $T_d$, and then the time variable precision control data edge position is added. The resulting two signals are “OR” digital logic, and the pulse width of the signal is widened. Therefore, the cross point is corrected to 50%. Then, when the cross point is offset above the ideal position, to stabilize the signal at 50%, the “AND” digital logic can be selected. Similarly, when the cross point offset is below the ideal position, the “OR” digital logic can be selected to stabilize the signal at 50%. Therefore, by adding time variables to the reconstruction process to precisely control the timing of the data edge position, the digital waveform method is used to reconstruct the pattern waveform, so that the cross point is stabilized at 50%, thereby correcting the drift of the cross point. In this method, two controllable delay lines with different delays can generate a controllable relative delay, which allows the influence of the device propagation delay to be eliminated and the cross point of the waveform to be reconstructed by changing the relative delay of the two signals. As a result of this process, the change in the position of the cross point is transformed into a precise control of the relative delay.
IV. THE CROSS POINT CORRECTION CONTROL AND JITTER TEST

In the transmission process of high-speed serial signals, jitter is one of the core aspects of signal integrity. Today, jitter is a key factor in restricting the development of high-speed digital systems, leading to increases in the BER of communication systems. Jitter is also a key indicator in the eye diagram. The larger the jitter is, the smaller the effective sampling window of the signal will be. In the frequency domain, the center of the jitter spectrum is the operating frequency of the signal, obeying the Gaussian distribution [19], [20]. The amplitude decreases gradually as the signal moves away from the center of the frequency. The signal of each frequency can be a combined signal of different frequency components. A signal that is not a centered frequency can be considered as the noise (phase noise) of the frequency domain. Jitter and phase noise are essentially the same. Both are the result of time domain analysis and frequency domain analysis. Therefore, the phase noise can be identified by testing the change of the position of the cross point and the size of different jitters. The following is a test to determine the effect of the change of the cross point on the DCD and the BER components of the signal jitter.

![FIGURE 8. The Distribution of TIE jitter and BER at different cross point positions](image)

From Fig. 8, it can be seen that there are two similar Gaussian distributions in the TIE histogram, namely, at 30% and 70% of the cross point, which obviously have more jitter in the DCD distribution characteristics. Because there is more jitter in the DCD components, the TIE histogram distribution features mainly include random jitter and DCD. At the 50% cross point, the DCD is very small. The distribution characteristics of the DCD have the characteristics of random jitter. When the cross point is at 50%, most sample values are jitter to 0 ps, while the cross points are at 30% and 70%, and most sample values are at approximately 17 ps.

From the test results, when the cross point has deviated from its ideal position, the data error rate increases sharply. Therefore, improving the stability of the cross point of the eye diagram can minimize the DCD jitter, thereby significantly reducing the BER. Fig. 9 is a circuit diagram showing the precise control of the cross point.

![FIGURE 9. The circuit schematic diagram for precise control of the cross point](image)

The input fanout buffer portion uses the NB7L14M, which is a differential 1:4 clock/data distribution chip. A CML output structure with internal source termination optimizes the skew and jitter of the waveform and has data-dependent jitter that is less than 10 ps. The device can generate four identical outputs that allow the data to operate up to 12 Gbps. Therefore, the NB7L14M is well suited as an input fanout buffer for this circuit. Its inputs include an internal 50 Ω termination resistor that accepts multiple levels such as LVPECL, LVCMOS, LVTTL, and LVDS. An external termination of 400 mV output swings the 50 Ω resistor to VCC. The input level is at the CML level.

The digital delay line in the precision delay adjustment portion uses the HMC911LC4B with a bandwidth of up to 24 GHz. The output differential voltage is up to 800 mVpp. The HMC911LC4B has a continuously adjustable delay range of 0 to 70 ps. Moreover, the device has internal...
temperature compensation characteristics that produce an offset with temperature changes, minimizing circuit delay. The output is internally terminated with 50 Ω to VCC and can be coupled with AC/DC. The delay device has a propagation delay with a typical value of 480 ps. Thus, to achieve the effect of precise control delay, by adding a delay line at the same time on both paths, the relative delay can increase the delay of the delay line to 80 ps. Better use of the linear control delay interval of the delay line can eliminate the impact of the delay line propagation delay. The relationship between the delay line control voltage and the time delay is shown in Fig. 10.

**FIGURE 10.** Time delay vs. delay control voltage

In the precision delay adjustment portion, the “AND” digital logic and “OR” digital logic select the HMC746LC3C. The device can be configured with external logic to achieve the required logic functions. This approach is widely used in RF test and high bandwidth test measurement applications at up to 14 Gbps with a programmable output voltage amplitude of 600 mV to 1.1 V. The “AND” and “OR” digital logic timing diagrams are shown in Fig. 11(a) and (b).

**FIGURE 11.** The sequence of “AND” logic and “OR” logic

The data selector in the precision delay adjustment section uses the HMC748LC3C, which is an alternative data selector with a maximum data rate of up to 14 Gbps, for path switching in high-bandwidth RF test areas. The selector outputs one of the two single-ended inputs at the appropriate selection. The HMC748LC3C also features an output level control pin that allows either for loss compensation or for signal level optimization. The data selector timing diagram is shown in Fig. 12.

**FIGURE 12.** The sequence of data selector

The output driver part uses NB4L16M, which is capable of receiving drive signals up to 5 Gbps and hence is very suitable for the output driver of this solution. The signal characteristics are shown by the LeCroy WaveMaster 813Zi-A digital oscilloscope with a 40 GS/s real-time sampling rate and 13 GHz bandwidth. The spectrogram is measured by the EXA Signal Analyzer N9010A, which has a frequency range from 10 Hz to 26.5 GHz. As shown in Fig. 13(a), the modulation system shows that when the cross point is at 36.14%, the size of the DDJ is 45.56 ps, of which the DCD is 31.11 ps and DCD accounts for 68.28% of the DDJ. After correcting the cross point, as shown in Fig. 13(b), the cross point is at 50.89%, the size of the DDJ is 12.228 ps, and the DCD is only 321 fs. It can be found that the jitter of the DCD becomes very small. Moreover, as shown in Fig. 13(c) and (d), the spectrum is significantly attenuated at a certain frequency. Through further testing and analysis, as shown in Fig. 14(a), it can be seen from the system that when the cross point of the eye diagram is at 35.34%, the DDJ size is 49.69 ps, and the DCD is 32.43 ps. Most of the DDJ is generated by the DCD. After the cross point is corrected, as shown in Fig. 14(b), the cross point is at 50.82%, the size of the DDJ is 19.13 ps, and the DCD is only 1.31 ps. In this case, the ISI correction basically remains unchanged. Because the ISI is mainly derived from signal dispersion following the attenuation and reflection of the transmission media [21]–[23], the cross point position brings about the DCD, mainly due to the pulse width being changed relative to the nominal duty ratio of 50%. Therefore, this method can effectively minimize the jitter of the DCD, thereby reducing the BER caused by the DCD [24], [25]. In addition, it can be seen that the signal’s spectrum is attenuated at a certain frequency, as shown in Fig. 14(c) and (d). Moreover, this method also succeeds in
minimizing the jitter of the DCD at the highest frequency.

FIGURE 13. The eye diagram and spectra before and after correction at a frequency of 1 Gbps

FIGURE 14. The eye diagram and spectra before and after correction at a frequency of 3 Gbps

This method can correct the cross point of the eye diagram when using a digital method. Moreover, the relative amount of delay change and the position of the cross point of the eye diagram are shown in Fig. 15.

FIGURE 15. Relative delay change vs. cross point position

After the analysis and experimental tests presented here, it can be seen that under the NRZ pattern and the delay change of 80 ps, the output cross point can be changed between 30% and 70%.

The following Fig. 16 diagrams the experimental test as an installed system.

FIGURE 16. Installed system of the experimental test

The experimental test setup includes the oscilloscope (LeCroy WaveMaster 813Zi-A) for testing the cross point and jitter, an arbitrary wave generator (Tektronix AFG3052C) for generating noise, and the correction module for the cross point of the eye diagrams, as well as a multifunctional control board with FPGA and MCU, which is used to precisely control the cross point of the eye diagram. To meet the accuracy requirements, a 16-bit high precision DAC is selected.

V. THE ROBUSTNESS OF THE CROSS POINT UNDER DISTURBANCE

The robustness of the signal under disturbance is an important problem. The stability of the output signal upon the addition will be tested experimentally. The noise, which is generated by the Tektronix AFG3052C, is injected into the output signal by the synthesizer. The noise obeys a Gaussian distribution with an amplitude of 100 mV. The synthesizer uses a Mini-Circuit Power Combiner, which has an internal 50 Ω impedance match, a very wide band (DC to 12 GHz), and excellent amplitude unbalance.

Fig. 17(a) and (b) show the corresponding PRBS waveform, the cross point of the eye diagram, the TIE track and the TIE histogram for 3 Gbps, which correspond to the case of no disturbance signal and a disturbance signal of 100 mV of noise, respectively. It can be seen that the outline of the eye diagram becomes coarser when the noise disturbance is added, as in Fig. 17(b), which can be compared with the cross point (33.5%) in Fig. 17(a), when no noise disturbance has been added. In this case, the cross point is in the ideal position (in light of the errors and the addition of noise), and the change is only 1%, which is not significant. Thus, this setup is more robust to disturbance. Fig. 17(c) and (d) display test pictures that correspond to 50% of the cross point without disturbance and with the addition of noise disturbance, respectively. Fig. 17(e) and (f) are test pictures that correspond to 70% of the cross point without disturbance and with the addition of noise disturbance, respectively. From the above experiments, it is

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found that the signal has good robustness to disturbances in the range of 30% to 70% of the cross point at the highest data rate of 3 Gbps.

Based on the experimental results, this method can generate a controllable relative delay through the delay line, can reconstruct the pattern waveform by using a digital method and can adjust the cross point of the signal eye diagram by using digital logic, thereby correcting the drift of the cross point. At the same time, the method offers strong robustness in the face of external interference. In this method, the physical layer design of several simple protocols can be directly completed using this digital method. Moreover, this method has the advantages of precise and convenient adjustment at higher data rates.

VI. CONCLUSION

In this paper, a digital adjustable cross point method is proposed to verify the jitter of the DCD component and the BER caused by cross point correction. This article corrects the cross point, presenting a digital method to further minimize the jitter of the DCD and BER and improve the quality of the eye diagram. The innovation presented in this paper is compared with the traditional ways of changing the cross point. Accordingly, this method reconstructs the pattern waveform by using a digital method, adds a time variable to precisely control the timing of the data position in the reconstruction process and realizes the precise cross point by using digital control. As a result, the cross point is stable at 50%, thus correcting the drift of the cross point and improving the data transmission quality. The robustness of this method is strong, as verified by experiments in which the method achieved a 30% to 70% controllable cross point of the NRZ pattern under 3 Gbps with a resolution up to 1%. In the experiments, the method solves the problem of drift in the cross point of the eye diagram and significantly reduces the BER caused by the DCD jitter. In addition, the proposed method can also predict the behavior of electrical systems based on analysis of cross points. In the simulations, the stress from jitter is limited by the availability of signal sources with controllable and flexible jitter properties in the design environment [26], [27].

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