Switching State Sequences Based Modulation Scheme for T-type 5L-ANPC Converter

KUN WANG1, YINGFEI XU1, GUANGDI LI1, YAN DENG1, XIANGNING HE1, (Fellow, IEEE), YI LU2, AND YONG YANG3

1 Zhejiang University, College of Electrical Engineering, Hangzhou, 310027 China
2 State Grid Zhejiang Electric Power Research Institute, Hangzhou 310014, China
3 State Grid Zhejiang Electric Power Co., Ltd., Hangzhou, 310000, China

Corresponding author: Yan Deng (e-mail: dengyan@zju.edu.cn).

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ABSTRACT A switching state sequences (SSSs) based modulation scheme along with a dead-time effect compensation method is proposed in this paper. In the proposed modulation scheme, the converter’s switching states changing sequence in one carrier period, i.e. the SSS, is treated as the basic unit to control the T-type 5L-ANPC converter. Because there are only two possible voltage levels in each SSS, the converter can be controlled as a traditional two-level converter within each SSS. Thus, a switching pulse modification based method is proposed to compensate the dead-time effect within each SSS. Moreover, an SSS transition rule and the transition diagram are furtherly presented to avoid the dead-time effect between different SSSs. Consequently, both the output voltage delay and the unwanted voltage glitches that caused by the dead-time effect are avoided in the whole modulation range. Besides, a balancing strategy is proposed to balance the flying capacitor voltage based on the charging abilities of SSSs. The performance and effectiveness of the proposed modulation scheme are validated by both simulation and experimental results.

INDEX TERMS Active neutral point clamped (ANPC) converter, dead time effect compensation, flying capacitor voltage balance, multilevel converter.

ABBREVIATION

ACH Active High
ACL Active Low
ACx Active High or Low
ANPC Active Neutral Point Clamped
CHB Cascaded H-Bridge
DTC Dead Time Compensation
FC Flying Capacitor
INTRM_SSS Intermediate Switching State Sequence
NPC Neutral Point Clamped
PD-PWM Phase Deposition Pulse Width Modulation
SSS Switching State Sequence
SV-PWM Space Vector Pulse Width Modulation
THD Total Harmonic Distortion

I. INTRODUCTION

Multilevel converters have received increased attention in medium- and high-power conversion systems due to the lower total harmonic distortion (THD) and higher efficiency [1]–[8]. The bulky output filters and series connection of semiconductor switches are also avoided. Generally, there are three types of multilevel converter topologies that widely used in industry, i.e. the neutral point clamped (NPC) converters [4], [5], flying capacitor (FC) clamped converters [6], [7] and cascaded H-bridge (CHB) converters [8].

The active neutral point clamped (ANPC) converter is one of the most popular multilevel converters, which combines the NPC converter and the FC converter. Because of the reduced circuit cost and control complexity, conventional five-level ANPC (5L-ANPC) converter in Fig. 1(a) has been widely used in industrial motor drives [9]–[12]. And recently, many variations of the conventional 5L-ANPC converter are presented in literature [13]–[17]. Among them, the T-type 5L-ANPC converter in Fig. 1(b) has a different connection mode of FC, which leads to a reduction of conduction loss [13]. And it has a higher overall efficiency than the conventional 5L-ANPC converter in medium voltage applications [14].
Modulation method, FC voltage balancing and the dead-time effect compensation (DTC) are the common concerns in the application of 5L-ANPC converters [18]–[22]. In [18], a space vector PWM (SV-PWM) method is proposed for the 5L-ANPC converter, where the dead-time effect is also compensated by selecting proper vector sequences and constraining the switching states transitions. However, large number of space vectors for high-level converters lead to heavy computational burden for the controllers. Selective harmonic elimination (SHE) PWM are researched for 5L-ANPC converters in [19]–[21]. The FC voltage can be regulated by swapping the switching patterns. However, SHE method requires complex calculations of the switching angles. Carrier-based PWM scheme requires no calculation for the switching angles or space vectors, which makes it more suitable for multilevel applications. In [22], phase-shifted PWM (PS-PWM) scheme is adopted to subtly control the traditional 5L-ANPC converter as a two-level converter cascaded with a three-level FC converter.

Dead-time has to be implemented in the PWM signals to prevent circuit shoot through during the switching intervals. However, the insertion of dead-time will cause output voltage error and current distortion. With the increase of switching frequency, this undesirable effect worsens and leads to the increased torque ripples, excessive heating of the motor or increased THD of the grid current. Therefore, the compensation of dead-time effect is crucial to the improvement of PWM converters performance. So far, the existing dead-time effect compensation methods mainly fall into two categories: the average-based DTC and the pulse-based DTC [23]–[33]. The average-based DTC method estimates the average voltage error and adds the opposite value of error to the converter voltage reference to compensate the distorted magnitude of output voltage [23]–[29]. But the output voltage delay caused by dead-time effect cannot be corrected with this method. By contrast, the pulse-based DTC modifies the driving signals pulse by pulse to correct both the magnitude error and the output voltage delay [30]–[33].

In this paper, a modulation scheme based on SSSs is proposed for the T-type 5L-ANPC converter. In this scheme, the switching state commutation sequences in one carrier period, rather than independent switching states, are treated as basic units for the converter control. Based on this scheme, the 5L-ANPC converter can be treated as a two-level converter within each SSS, which makes it convenient for the modification of driving pulses. A pulse-based DTC method is furtherly proposed to compensate the unwanted voltage glitches and output voltage delay in each SSS. Moreover, a SSS transition diagram is presented to deal with the dead-time effect between different SSSs. And FC voltage is also balanced based on the charging ability difference of SSSs.

This paper is organized as follows. Operation principles and the dead-time effect of the T-type 5L-ANPC converter are analyzed in Section II. Section III describes the SSSs based modulation scheme in detail. And the dead-time effect compensation method is proposed in Section IV. Section V analyzes the charging ability of each SSS and introduces the FC voltage balancing method. Simulation and experimental results are presented in Section VI.

II. OPERATION PRINCIPLES AND DEAD-TIME EFFECT OF T-TYPE 5L-ANPC CONVERTER

A. OPERATION PRINCIPLES

The configuration of a single-phase T-type 5L-ANPC converter is illustrated in Fig. 1 (b). Two dc-link capacitors \( C_{f}, C_{p} \) rated at \( V_{dc}/2 \) are series connected to the DC bus. And the flying capacitor \( C_{f} \) is rated at \( V_{dc}/4 \). Thus, five output voltage levels (+\( V_{dc}/2 \), +\( V_{dc}/4 \), 0, -\( V_{dc}/4 \) and -\( V_{dc}/2 \)) can be generated by the switching states shown in Table 1. The switching states are labeled from +2 to -2. The redundant switching state pairs for output level +\( V_{dc}/4 \) and -\( V_{dc}/4 \) are labeled as +1_2, +1_1, 0_1, 0_2, -1_1 and -1_2 respectively. It is observed that the redundant switching states have different effect on the FC voltage according to the direction of output current. Moreover, \( S_{1}, S_{2}, S_{3} \) are always OFF during the negative half period, and \( S_{4}, S_{5}, S_{6} \) are all OFF during the positive period, which is benefit for the T-type 5L-ANPC converter to reduce switching losses. The current paths of each switching state are presented in Fig. 2, where the output current is assumed to be positive.

![Figure 1. Configurations of 5L-ANPC converters. (a) Conventional 5L-ANPC converter. (b) T-type 5L-ANPC converter [13].](image-url)
which may lead to a) unwanted voltage glitches or b) delay of output voltage. These two types of dead-time effect are analyzed as follows.

Taking the switching state commutations between +1_1 and +2 as an example. As illustrated in Fig. 3, during the dead-time period, output current $i_o$ will conduct through the antiparallel diode of $S_1$ or $S_8$ according to the output current direction. In the first condition, the output current $i_o$ is positive, so the antiparallel diode of $S_1$ conducts, and the output voltage is clamped to an unwanted -1 level until the dead-time elapses. This condition results in unwanted voltage glitches of output voltage as shown in Fig. 4. However, when the output current $i_o$ is negative, the antiparallel diode of $S_8$ conducts during the dead time. And the output voltage is clamped to +2 level until the dead-time elapses. As shown in Fig. 5, this condition will not lead to voltage glitches, but result in a delay of output voltage when the switching state changes from +2 to +1_1.

Similarly, the dead-time effect of other commutation modes can be obtained. However, since not all the commutation modes are used in the proposed modulation scheme, the dead-time effects will be summarized in Section IV after the modulation scheme is introduced in the next section.

### TABLE 1. Switching states of the T-type 5L-ANPC converter.

<table>
<thead>
<tr>
<th>Switching State</th>
<th>Output voltage</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>$S_5$</th>
<th>$S_6$</th>
<th>$S_7$</th>
<th>$S_8$</th>
<th>$i_o&gt;0$</th>
<th>$i_o&lt;0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>+2</td>
<td>$+V_a/2$</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>+1_2</td>
<td>$+V_a/4$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>+1_1</td>
<td>$+V_a/4$</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>↓</td>
<td>↑</td>
</tr>
<tr>
<td>0_1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0_2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>-1_1</td>
<td>$-V_a/4$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>-1_2</td>
<td>$-V_a/4$</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>↓</td>
<td>↑</td>
</tr>
<tr>
<td>-2</td>
<td>$V_a/2$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

### B. DEAD-TIME EFFECT ANALYSIS

As shown in Table 1, there are three complementary switch-pairs in the T-type 5L-ANPC converter, i.e. 1) $S_2$ and $S_3$, 2) $S_1$ and $S_7$ ($S_8$) during the positive period, 3) $S_4$ and $S_5$ ($S_6$) during the negative period. Switches $S_2$, $S_3$ are common-cathode connected as one bidirectional switch controlled by the same switching signal. Similarly, switches $S_1$, $S_7$ ($S_8$) are common-cathode connected as one bidirectional switch and operated synchronously. During the dead-time period, the complementary switches are in OFF state simultaneously.
III. PROPOSED SSSs BASED MODULATION SCHEME

In order to reduce the computational complexity and compensate the dead-time effect effectively, an SSS based modulation scheme is proposed in this section. The SSSs construction and the mapping process is introduced at first. Then, the PWM polarity constrains for the SSS selection are discussed and the feasible SSSs group is obtained.

A. SSSs AND THE MAPPING PROCESS

As illustrated in Fig. 6 (a), phase-disposition PWM (PD-PWM) is adopted in the proposed modulation scheme. The modulation region is divided into four ranges by four carriers, \( P_2, P_1, N_1 \) and \( N_2 \). Fig. 6 (b) presents the situation where modulation reference lies in range \( P_2 \). By comparing reference with the carrier, the expected output voltage level can be obtained. It should be noticed that the selection of redundant switching states \(+1_1\) and \(+1_2\) is determined by the FC voltage balance strategy as introduced in Section V. All the possible SSSs in range \( P_2 \) are \((+1_1, +2, +1_1), (+1_2, +2, +1_2), (+1_1, +2, +1_2), (+1_2, +2, +1_1), (+2, +1_2, +2)\) and \((+2, +1_2, +2)\) and \((+2, +1_2, +2)\). And the SSSs in other ranges can be obtained in the same way.

It is observed that the switching state sequences consist of three switching states in one carrier period. To map the SSSs with the ON/OFF control of the eight switches, define “switching string” as the ON/OFF status change sequence of a switch in one carrier period. Therefore, for SSS \((+1_1, +2, +1_1)\) as shown in Fig. 7 (a), the switching string of \( S_1 \) is “010”, the switching strings of \( S_7, S_8 \) are both “101”, while that of \( S_2 \) is “111”, \( S_3, S_4, S_5, S_6 \) are “000”. Similarly, all the SSSs can be mapped with the ON/OFF control of eight switches.

One possible ON/OFF control scheme of the eight switches for SSS \((+1_1, +2, +1_1)\) is illustrated in Fig. 7(b). ACH and ACL are the PWM polarity of switches, which means “Active High” and “Active Low”, respectively. The PWM polarity which generates high output when reference is larger than the carrier is ACH, while that generates low output is ACL. Accordingly, the mapping between SSSs and the switching strings, along with the PWM polarities, are presented in Table 2, where ACx means ACH or ACL.

B. SSS SELECTION AND POLARITY COMBINATION

It is observed from Table 2 that the PWM polarity combination of eight switches for one SSS may conflict with that for another. For example, to generate SSS \((+1_1, +2, +1_1)\) and SSS \((+2, +1_1, +2)\), the required polarity of \( S_2, S_3, S_5, S_6 \) could be either ACH or ACL since they are constant during the whole carrier period. However, the required polarity of \( S_1 \) is ACH for SSS \((+1_1, +2, +1_1)\), but ACL for SSS \((+2, +1_1, +2)\). The required polarity of \( S_4, S_7 \) is ACL for SSS \((+1_1, +2, +1_1)\), but ACH for SSS \((+1_1, +1_2, +2)\).

Moreover, because there is no protection mechanism such as “shadow register” for most DSP controllers’ control register, the polarity specification of PWM modules cannot be configured arbitrarily during the program execution. The asynchronous modification of control register may lead to corruption or spurious operations. Therefore, the selection of SSSs is constrained by the PWM polarity combination of eight switches and should be defined at the beginning of the control program. Consequently, two PWM polarity combinations along with the corresponding SSS groups are extracted from Table 2. One of the polarity combination is “polarity combination 1”, is shown in Table 3 as an example. In the following analysis, all the selections of SSS are executed within this SSSs group.

Therefore, in each modulation range, the expected SSS can be generated by specific switching strings of eight switches. Taking dead-time effect compensation into consideration, the modulation reference generation of each switch and the SSS transition rules are further introduced in the following section.
### TABLE 2. Mapping from SSSs to switching strings and the PWM polarity mode of each switch

<table>
<thead>
<tr>
<th>Switching state sequence (SSS)</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>$S_5$, $S_6$</th>
<th>$S_7$, $S_8$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$+_1$, $+_2$, $+_1$</td>
<td>011</td>
<td>ACH</td>
<td>110</td>
<td>ACH</td>
<td>000</td>
<td>000</td>
</tr>
<tr>
<td>$+_2$, $+_1$, $+_1$</td>
<td>110</td>
<td>ACH</td>
<td>011</td>
<td>ACH</td>
<td>100 ACL</td>
<td>000</td>
</tr>
<tr>
<td>$+_1$, $+_2$, $+_1$, $+_2$</td>
<td>111</td>
<td>Acx</td>
<td>010</td>
<td>ACH</td>
<td>101 ACL</td>
<td>000</td>
</tr>
<tr>
<td>$+_2$, $+_1$, $+_1$, $+_2$</td>
<td>010</td>
<td>ACH</td>
<td>111</td>
<td>Acx</td>
<td>000 ACL</td>
<td>Acx</td>
</tr>
</tbody>
</table>

### TABLE 3. Polarity combination 1 and the corresponding SSSs group

<table>
<thead>
<tr>
<th>Switching state sequence (SSS)</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>$S_5$, $S_6$</th>
<th>$S_7$, $S_8$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$+_1$, $-_2$, $+_1$</td>
<td>011</td>
<td>ACH</td>
<td>110</td>
<td>ACH</td>
<td>000</td>
<td>000</td>
</tr>
<tr>
<td>$+_2$, $+_1$, $-_1$</td>
<td>110</td>
<td>ACH</td>
<td>011</td>
<td>ACH</td>
<td>100 ACL</td>
<td>000</td>
</tr>
<tr>
<td>$-_2$, $-_1$, $-_1$, $-_2$</td>
<td>111</td>
<td>Acx</td>
<td>010</td>
<td>ACH</td>
<td>101 ACL</td>
<td>000</td>
</tr>
<tr>
<td>$-_2$, $-_1$, $-_1$, $-_2$</td>
<td>010</td>
<td>ACH</td>
<td>111</td>
<td>Acx</td>
<td>000 Acx</td>
<td>Acx</td>
</tr>
</tbody>
</table>

- ANPC Converter
IV. DEAD-TIME EFFECT COMPENSATION

As presented in Table 2, there are 16 kinds of switching state commutation modes in the SSSs based modulation scheme. With the analysis method illustrated in Section II-B, all the dead-time effects are summarized in Table 4. It can be observed that unwanted voltage glitches and output voltage delays are induced. Thus, a dead-time effect compensation method is required.

<table>
<thead>
<tr>
<th>Modes</th>
<th>( i_o &gt; 0 )</th>
<th>( i_o &lt; 0 )</th>
<th>Modes</th>
<th>( i_o &gt; 0 )</th>
<th>( i_o &lt; 0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>(+1_1 &gt; +2)</td>
<td>-1 glitch</td>
<td>-1 glitch</td>
<td>Delay</td>
<td>(+1 &gt; +1_1 )</td>
<td>-1 glitch</td>
</tr>
<tr>
<td>(+1_2 &gt; +2)</td>
<td>Delay</td>
<td>+2 &gt; +1_1</td>
<td>Delay</td>
<td>(+1 &gt; +1_1 )</td>
<td>Delay</td>
</tr>
<tr>
<td>(+0_1 &gt; +1_1)</td>
<td>-2 glitch</td>
<td>+1_2 &gt; 0_1</td>
<td>Delay</td>
<td>-2 glitch</td>
<td>Delay</td>
</tr>
<tr>
<td>(+1 &gt; +1_1)</td>
<td>+2 glitch</td>
<td>0_2 &gt; -1_1</td>
<td>+2 glitch</td>
<td>Delay</td>
<td>-2 &gt; -1_1</td>
</tr>
<tr>
<td>(+1 &gt; -1_1)</td>
<td>-1 glitch</td>
<td>Delay</td>
<td>+1 glitch</td>
<td>Delay</td>
<td></td>
</tr>
<tr>
<td>(+2 &gt; -1_2)</td>
<td>Delay</td>
<td>-1_2 &gt; -2</td>
<td>Delay</td>
<td>-2 &gt; -1_2</td>
<td>Delay</td>
</tr>
</tbody>
</table>

Table 4. Dead-time effects of 16 commutation modes

A. DEAD-TIME EFFECT COMPENSATION WITHIN SSSs

Since the switching states transitions are mapped to the ON/OFF control of eight switches, the 5L-ANPC converter can be controlled as a two-level converter in each SSS. In the digital control scheme, modulation reference is calculated and loaded to the PWM module’s “counter-compare” register every carrier period. Thus, in the proposed compensation method, a modification offset (named as DT) is added to or subtracted from the original reference (Ref) to modify the driving pulses. The value of DT is determined by the predefined dead-time value \( T_d \), switching frequency \( f_{sw} \), and the amplitude of the carriers \( V_p \) as shown in (1).

\[
DT = 2 \times T_d \times f_{sw} \times V_p
\]

Table 5 demonstrates the reference modification process for the complementary switches \( S_1, S_7 \) and \( S_8 \) to compensate the dead-time effect within SSS \((+1_1, +2, +1_1)\). For the other switches that keep ON or OFF in the whole SSS, the references are set as zero or the amplitude of carrier.

<table>
<thead>
<tr>
<th>( i_o &gt; 0 )</th>
<th>( i_o &lt; 0 )</th>
<th>( i_o &gt; 0 )</th>
<th>( i_o &lt; 0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S_1 )</td>
<td>( S_7 )</td>
<td>( S_8 )</td>
<td>( S_7 )</td>
</tr>
<tr>
<td>Ref</td>
<td>Ref – DT</td>
<td>Ref + DT</td>
<td>Ref – DT</td>
</tr>
<tr>
<td>Ref – 2*DT</td>
<td>Ref</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

When the output current \( i_o \) is positive, the reference of \( S_1 \) is set as original value Ref. While offset DT is subtracted from Ref for \( S_7 \) and added to Ref for \( S_8 \). Therefore, \( S_7 \) and \( S_8 \) are no longer operated synchronously. As illustrated in Fig. 8, when the output voltage transits from \(+1_1 \) to \(+2\), before \( S_1 \) turns on, \( S_8 \) has turned off ahead to prevent the direct parallel connection of DC capacitor and FC. While \( S_7 \) keeps ON to clamp the output voltage to level \(+1\), as shown in Fig. 9.

When \( S_1 \) turns on, the output current commutates to \( S_1 \), and the output voltage converters to \(+2\) instantly. At last, \( S_7 \) turns off. Similarly, when output level transits from \(+2\) to \(+1_1\), \( S_1 \) turns off after \( S_7 \) has turned on, and \( S_1 \) turns on at last. As shown in Fig. 8, the unwanted voltage glitches are prevented compared to Fig. 4. And it is noticed that the time span of level \(+2\) is same to the ON-time of \( S_1 \), which is determined by the original modulation reference. Thus, the expected output voltage time-span is guaranteed.

When the output current \( i_o \) is negative, the reference of \( S_8 \) is set as Ref. While offset DT is subtracted from Ref for \( S_1 \), and two times of DT are subtracted from Ref for \( S_7 \). As illustrated in Fig. 10, the switching action sequence of switches is the same as when \( i_o > 0 \). However, because the reference of \( S_8 \) is set as the original value and the time span of level \(+2\) is now same to the ON-time of \( S_1 \), so the delay of output voltage in Fig. 5 is also prevented.

In conclusion, the modification offset DT should be added to or subtracted from the original reference of corresponding switches to make sure that:

a) \( S_1 \) changes its state only when \( S_1 \) is ON and \( S_8 \) is OFF;
b) \( S_8 \) changes its state only when \( S_8 \) is ON and \( S_5 \) is OFF;
c) Turn off \( S_3 \) before turn on \( S_7 \);
d) Turn off \( S_2 \) before turn on \( S_3 \).

FIGURE 8. Compensation method within SSS \((+1_1, +2, +1_1)\) when \( i_o > 0 \).

FIGURE 9. Commutation transient when the output is clamped to \(+1\) by \( S_7 \).
B. TRANSITION RULE FOR DIFFERENT SSSs AND DIFFERENT MODULATION RANGES

Because the adjacent switching states of two SSSs may differ from each other, so when the converter transits from one SSS to another, unwanted output voltage glitches or short connection of capacitors may be induced due to the dead-time. As illustrated in Fig. 11 (a), when the switching state changes from +1_1 to +1_2, all the related switches state are reversed. And during the dead-time, the floating capacitor is short connected by S2 and S3, and the positive bus capacitor is short connected by S1, S7 and S8. Since the compensation method above can only deal with dead-time effect inside the SSSs, an SSS transition rule is furtherly proposed for this situation.

The proposed rule is called “tail and head” rule, which goes like this: the head of the following SSS should be the same as the tail of the former one. Thus, the inversion of switches is avoided. One example of this rule is presented in Fig. 11 (b). Accordingly, the SSSs transition diagram between different SSSs in each modulation range is obtained in Fig. 12.

However, it can be observed that there is no proper SSSs for the converter to transit between different modulation ranges under the “tail and head” rule. Therefore, ten intermediate SSSs are constructed to link different modulation ranges as presented in Table 6. The intermediate SSSs are named as INTRM_SSS PxNy (x, y = 1, 2), where PxNy means that this intermediate SSS is used for the transitions from range Px to Ny. The proposed intermediate SSS group also coincides with the polarity combination 1.

Overall, the whole SSSs transition diagram is presented in Fig. 12. It should be noted that only one feasible transition path is illustrated in Fig. 12 to simplify the diagram. While the actual transition paths are influenced by the requirement of FC voltage balancing control as analyzed in the following section.

FIGURE 10. Compensation method within SSS (+1_1, +2, +1_1) when i0<0.

FIGURE 11. Transitions between different SSSs. (a) Abnormal transition. (b) Transition with “tail and head rule”.

FIGURE 12. SSSs transition diagram for the whole modulation range.
V. BALANCING STRATEGY OF THE FLYING CAPACITOR

Balance of the FC voltage is vital for the stable operation and performance of 5L-ANPC converters. In this section, the charging ability of SSSs is analyzed at first. It shows that different SSSs have different influence on the FC voltage. Accordingly, the selection methods of transition paths for both the steady state operation and the FC voltage regulation are presented.

A. CHARGING ABILITY OF SSSs

Each SSS consists of three switching states: head-, middle- and tail-state. Since the reference signal is constant in each carrier period, the head- and tail-state in each SSS last for the same time duration. Assume that the output current remains unchanged in one carrier period, according to the influence of switching states on the FC voltage presented in Table 1, the charging ability of SSSs can be obtained as follows.

For SSS P2_A (+1_1, +2, +1_2), its middle-state +2 has no influence on the FC voltage. However, when i_1>0, its head-state +1_1 charges the FC, and its tail-state +1_2 discharges the FC with the same output current and the same time. So P2_A (+1_1, +2, +1_2) is a “balancing SSS” and it is labeled with symbol “~” in Fig. 12. For P2_C (+1_2, +2, +1_2), both its head- and tail-state (+1_2) charge the FC when i_1>0, so P2_C is a “charging SSS” and labeled with “↑”. While for P2_D (+1_1, +2, +1_1), both the head- and tail-state (+1_1) discharge the FC when i_1>0, so P2_D is a “discharging SSS” and labeled with “↓”.

Similarly, the charging ability of other SSSs can be determined as labeled in Fig. 12. And for simplification, the charging ability of each SSS when i_1<0 is not illustrated. It should be noticed that the charging effect of the intermediate SSSs are ignored, because these SSSs are only adopted once when the modulation reference passes through different modulation ranges.

B. BALANCING CONTROL OF FC VOLTAGE

As shown in Fig. 13 (a), the modulation range is determined at first. Then FC voltage V_Fc is compared with its rated value V_{FC}. If FC voltage is within the threshold V_{TH}, i.e. |V_{FC} - V_{TH}|, balancing SSSs of this range are preferred, such as SSS P2_A and SSS P2_B of range P2. However, if there is no balancing SSSs in this range, the charging SSS and discharging SSS should transit in turns to maintain the FC voltage.

VI. SIMULATIONS AND EXPERIMENTAL VALIDATION

In order to validate the proposed modulation scheme and the dead-time effect compensation method, both simulation and experiments are carried out on the T-type 5L-ANPC converter. The parameters for simulation and experimental prototype are given in Table 7. And the voltage variation threshold of FC is set as 10% of its rated voltage.
A. SIMULATION RESULTS

Fig. 14 presents the output waveforms under the proposed modulation scheme without dead-time effect compensation. Since the DTC method and the intermediate SSSs are not adopted, many voltage glitches are observed in the output voltage. The driving signals of S1, S7, S8 along with the output voltage glitch (-1) are illustrated in Fig. 15, which is consistent with the analysis.

When the proposed modulation scheme with DTC method is adopted, unwanted voltage glitches are effectively avoided as shown in Fig. 16. The FC voltage is also well balanced around its rated value. Fig. 17 illustrates the details of the output voltage and driving signals of S1, S7, S8, which is consistent with the proposed DTC method.

B. EXPERIMENTAL RESULTS

The block diagram and pictures of the T-type 5L-ANPC converter prototype is presented in Fig. 18. In the prototype, the DC-link is provided by a front-end boost converter. And ADI ADSP-CM419F is adopted as the controller.

The converter performance without DTC is illustrated in Fig. 19 and Fig. 20 at first. As shown in Fig. 19, many glitches are induced in the output voltage, which coincides well with the analysis and the simulation. And the output current is distorted with a THD of 3.62%. The detail waveforms of the -1 voltage glitch and gate driving voltage of S1, S7, S8 are illustrated in Fig. 20.

When the proposed modulation scheme with DTC method is adopted, the output voltage glitches are effectively avoided as shown in Fig. 21. And the output current THD is reduced to 2.89%. Fig. 22 illustrates the gate driving voltage of S1, S7, S8 and the output voltage. When the output voltage transits from +1_1 to +2, S8 turns off at first, while S7 keeps on to clamp the output voltage to +1. After a dead time of 1.4μs, S1 turns on, and the output voltage changes to +2 instantly. At last, S7 turns off. Fig. 23 and Fig. 24 illustrate the FFT analysis and THD calculation of the output current.

### Table 7. Parameters for simulation and experimental prototype.

<table>
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<th>Parameters</th>
<th>Values</th>
<th>Parameters</th>
<th>Values</th>
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<td>DC voltage ($V_d$)</td>
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<td>Switching frequency</td>
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<td>FC voltage ($V_{dc}$)</td>
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<tr>
<td>Dead time</td>
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</table>

FIGURE 14. Simulation waveforms of the output voltage, current and FC voltage without dead-time effect compensation.

FIGURE 15. Simulation waveforms of output voltage and driving signals of S1, S7, S8 without dead-time effect compensation.

FIGURE 16. Simulation waveforms of the output voltage, current and FC voltage with the proposed dead-time effect compensation method.

FIGURE 17. Simulation waveforms of output voltage and driving signals of S1, S7, S8 with the proposed dead-time effect compensation method.

FIGURE 18. Block diagram and pictures of the prototype. (a) block diagram and (b) (c) pictures of the T-type 5L-ANPC converter setup.

FIGURE 19. Simulation waveforms of output voltage and driving signals of S1, S7, S8 without dead-time effect compensation.
Effectiveness of the proposed DTC method under different modulation index is provided in Fig. 25. It is observed that the proposed method achieves good compensation performance from low modulation index to over modulation.
VII. CONCLUSION

This paper presents a switching state sequences (SSSs) based modulation scheme and a dead-time effect compensation method for the T-type 5L-ANPC converter. In the proposed scheme, SSSs in each carrier period are treated as the basic control units, so the T-type 5L-ANPC converter can be controlled as a two-level converter within each SSS. The dead-time effect within each SSS is compensated by properly adjusting the driving pulses of switches. Besides, a “tail and head” rule is proposed to avoid the dead-time effect between different SSSs and different modulation ranges. Moreover, an FC voltage balancing method under the proposed scheme is also presented. Simulation and experimental results verify the effectiveness of the proposed modulation scheme and dead-time effect compensation method.

REFERENCES


Kun Wang received the B.E.E. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2013. He is currently working toward the Ph.D. degree from the College of Electrical Engineering, Zhejiang University, Hangzhou, China. His current research interests include modular multilevel converters, dc–dc converters and grid-connected photovoltaic systems.

Yingfei Xu received the B.E. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2017. He is currently pursuing the M.S. degree with the Zhejiang University, Hangzhou, China.

His current research interests include high-voltage dc–dc converters, modular multilevel converters and grid-connected photovoltaic systems.

Yang Yang was born in 1968 and received his Ph.D. degree in power system automation from Southwest Jiaotong University, Chengdu, China, in 1994. He is now a senior engineer and the General Manager of State Grid Zhejiang Electric Power Research Institute, Hangzhou, China. His research focus is on high power electronics technology, LLC-HVDC transmission system, VSC-HVDC transmission system, and DC grid.

Yi Lu received his B.S. degree in electrical engineering from North China Electric Power University, Baoding, China, in 2001. He received his M.S. and Ph.D. degrees in intelligence engineering and electrical engineering from the University of Liverpool, Liverpool, U.K., in 2002 and 2007, respectively. In 2008, he joined the State Grid Zhejiang Electric Power Research Institute, Hangzhou, China. He is a senior engineer, and his research interests include HVDC and FACTS.

Xiangning He (M’95–SM’96–F’10) received the B.Sc. and M.Sc. degrees from Nanjing University of Aeronautical and Astronautical, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 1989.

From 1989 to 1991, he was a Lecturer at Zhejiang University. In 1991, he received a Fellowship from the Royal Society of U.K. He was involved in research with Heriot-Watt University, Edinburgh, U.K., as a Post-Doctoral Research Fellow for two years. In 1994, he joined Zhejiang University. Since 1996, he has been a Full Professor with Zhejiang University. His research interests are power electronics and industrial applications.

Dr. He is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE) and has been appointed as IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2011. He is also a Fellow of the Institution of Engineering and Technology (formerly IEE), U.K.

Guangdi Li received the B.Sc. degree in Electrical Engineering from Northeastern University, Shenyang, China, in 2013. He is currently working toward the Ph.D. degree from the College of Electrical Engineering, Zhejiang University, Hangzhou, China.

His research interests include AC microgrid, energy storage system, three-phase inverters, chargers for electrical vehicles, and multilevel converters.

Yan Deng received the B.E.E. degree from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1994, and the Ph.D. degree in power electronics and electric drives from the College of Electrical Engineering, Zhejiang University, in 2000.

Since 2000, he has been a faculty member at Zhejiang University, teaching and conducting research on power electronics. He is currently a Professor with Zhejiang University. His research interests are topologies and control for switch-mode power conversion.

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