Research on Coordination and Optimal Configuration of Current Limiting Devices in HVDC Grids

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ABSTRACT This paper proposes a collaborative optimal configuration method of current limiting reactors (CLRs) and fault current limiters (FCLs) in modular multilevel converter (MMC) based high voltage direct current (HVDC) grids. The calculation methods of dc line fault currents and bridge arm fault currents considering the collaboration of CLRs and FCLs have high accuracy. The multi-objective optimization configuration model is established, in which the fault current limiting effect, the total inductances of CLRs and the number of FCLs are used as objective functions while the DCCBs current breaking capacity, the converter valves overcurrent protection, the boundary of the dc line protection area, the dynamic performance of the dc system and the converter station outlet dc voltage are used as constraints. In this paper, the multi-objective optimization algorithm is used to solve multi-objective optimal configuration problem for CLRs and FCLs. Finally, the proposed method is tested with a symmetrical monopole four-terminal MMC-HVDC grid in PSCAD/EMTDC. Simulation results verify that the proposed optimal configuration method can ensure the continuous and reliable operation of the dc grid under dc faults.

INDEX TERMS DC grid, modular multilevel converter, dc fault current, current limiting reactor, fault current limiter, multi-objective.

I. INTRODUCTION

With the urgent need of modern power grid for high reliability and high quality power supply, efficient utilization of renewable energy and multi-type power conversion. Modular multilevel converter (MMC) based high voltage direct current (HVDC) grids are attracting growing attention because of its numerous advantages [1]-[4], such as facilitating access of distributed energy and energy storage equipment, flexible operation mode and high power quality, etc.

For a dc grid, the main problem is that the low impedance of dc lines leads to the rapid and extensive development of dc-side short-circuit fault currents, which seriously threatens the safe and reliable operation of the system [5], [6]. Therefore, it is currently a key and difficult technical challenges how to realize the continuous operation of HVDC grids under dc faults.

The scheme of installing dc circuit breakers (DCCBs) at both ends of dc lines can isolate fault lines quickly and restore stable operation of other areas without fault, which can ensure the reliability of the system to the greatest extent. It is the protection and restoration scheme for dc grids recommended by CIGRE [7]. However, this scheme is faced with two challenges: a) with the development of dc systems in the direction of high-voltage and large-capacity, the development of the high-voltage and large-capacity DCCB is limited by technical backgrounds and capital costs [8], [9]; b) the insulated gate bipolar transistor (IGBT) has a poor overcurrent capability, MMC will be blocked to protect IGBT as soon as the fault current in the arms of MMC exceeds a current threshold of the converter valve, resulting in unnecessary power interruptions in the healthy dc system, which undoubtedly is contrary to the original intention of using DCCB to isolate faults quickly in the dc grid [10]-[12].
Hence, the study on the rational configuration method of fault current limiting devices for suppressing the fault current without MMC blocking is of great significance to ensure the safe and reliable operation of HVDC grids.

Recently, many researchers have focused on the application of current limiting reactors (CLRs) and fault current limiters (FCLs) in the HVDC grid. The dc fault current can be passively suppressed by installing CLR at both ends of dc lines, and the boundary of dc line protection area can be formed by using CLR [13]. Reference [14] used CLR at the dc side of MMC to ensure that DCCBs cut off the dc fault current without MMC blocking, but the method is only applicable to the hybrid HVDC grid. Reference [15] proposed a CLR sizing criterion for continuous operation of the meshed HVDC grid under dc faults. However, the system only relies on the CLR to passively suppress the fault current, and the fault current limiting method is single. At the same time, this method does not consider the dynamic performance constraints of the system. Due to the limited current limiting effect of the CLR, the excessive inductance value of the CLR will bring about many problems such as high capital cost, large footprint, poor dynamic performance of system and long fault isolation time [16]. Therefore, the inductance value of the CLR should have a reasonable value interval. The minimum value of the interval is related to the basic condition that the CLR forms the boundary of the dc line protection area. The maximum value of the interval is related to the dynamic performance of the dc system.

Different to the CLR, the FCL has almost no negative influences on the system normal operation, and it is actively put into the short-circuit path to suppress the fault current after the short circuit. Reference [17] designed an inductive superconducting FCL applied in multi-terminal HVDC systems. Reference [18] proposed essential technical indicators of the dc superconducting FCL and compared current limiting performance of different types of the superconducting FCL. However, the application of superconducting FCLs in the dc grid needs further research, including selectivity of relay protection, rapid recovery after fault isolation and so on. Reference [19] proposed a resistive dc FCL in MMC-HVDC systems to limit the rising rate of dc fault current, which consisted of a control module and a damping module.

It can be seen that most of the existing research has focused on single fault current limiting devices. Research on the collaboration of various fault current limiting devices was rarely involved. Owing to the absence of the reasonable and effective collaborative optimization configuration method of CLRs and FCLs, the main contribution of this paper is to propose a collaborative optimal configuration scheme of CLRs and FCLs for HVDC grids, ensuring the continuous operation of HVDC grids under dc faults.

The rest of this paper is organized as follows: Section II proposes the fault current calculation method. In Section III, the problem formulation is introduced. The detail of proposed method is given in the section IV. The proposed method is applied and validated in a four-terminal MMC-HVDC grid in Section V. Finally, the conclusions is provided in section VI.

II. FAULT CURRENT CALCULATION METHOD

A. DC FAULT PROTECTION SEQUENCE

At present, there is still a lack of reasonable and effective collaborative optimization configuration method of CLRs and FCLs in HVDC grids. Although simulation can find an optimal configuration scheme that meets the conditions, it cannot achieve the global optimal allocation. This paper mainly provides a theoretical basis for the parameter selection of CLR and the location determination of FCL from the point of view of system.

In order to improving fault ride-through capability of HVDC grids, and from the perspective of reducing the energy absorption of the metal oxide arrester (MOA) and reducing the fault clearing time [20], this paper suppresses the dc fault current by installing a resistive FCL at both ends of dc lines. Fig. 1 shows the simplified circuit of input the current limiting resistor with parallel MOA.

During normal operation, the current limiting resistor is bypassed and does not generate additional power loss. When a dc short-circuit fault occurs at time \( t_0 = 0 \), it can be detected rapidly by the fault detection system. At time \( t_1 \), the FCL receives the operation signal from the fault detection system, the current limiting resistor is put into the short-circuit path to suppress the fault current. The operation time of main protection for dc line fault is from \( t_0 \) to \( t_1 \). In view of the high requirement of relay protection in HVDC grids, it is usually within 3 ms [10], [21], [36]. In this paper, it is assumed that relay protection can complete fault detection and identification within 3ms and transmit operation signals to FCLs and DCCBs.

In recent years, DCCBs have been developed rapidly [37], [38]. Hybrid DCCBs have a great application prospect in HVDC grids due to their advantages such as short breaking time and low on-state losses [22]. As shown in Fig. 2, a hybrid DCCB consists of the main branch and the breaking branch.

During normal operation, the current is going through the main branch consisting of an ultrafast disconnector and an auxiliary dc breaker. When a dc short-circuit fault occurs at time \( t_0 = 0 \), the DCCB receives the operation signal and opens the auxiliary dc breaker at time \( t_1 \). After a delay of about 0.25 ms, at time \( t_2 \), the fault current is commutated from the main branch into main dc breaker in the breaking branch. When auxiliary dc breaker completes its operation, the ultrafast disconnector is triggered. After a delay of about 2 ms, the main dc breaker is then opened at time \( t_3 \) and the MOA is put into the short-circuit path to absorb the fault energy. Then the fault current decreases rapidly. When the fault current is less than a certain threshold, fault isolation is completed by residual dc breaker at time \( t_4 \). The dc fault protection sequence diagram of HVDC grids is shown in Fig. 3.
FIGURE 1. Simplified circuit of input the current limiting resistor with parallel MOA.

The main branch

Residual dc breaker

The breaking branch

FIGURE 2. The hybrid DCCB structure.

FIGURE 3. The dc fault protection sequence diagram of HVDC grids.

B. SIMPLIFIED MODEL OF MMC UNDER DC FAULT

The pole-to-pole short-circuit fault in the dc side of a dc grid is the biggest threat to the system. Within a few milliseconds after the dc fault, MMC capacitors will discharge rapidly and cause very high short-circuit currents both in the dc lines and the arms of MMC. During this time, the fault current component from the ac grid can be ignored [23]. As shown in Fig. 4, the MMC can be equivalent to the RLC circuit before blocking [24].

In Fig. 4, $U_{dc}$ is the dc voltage at the instant of dc fault occurrence, $I_{dc}$ is the dc current at the instant of dc fault occurrence. $C$, $L$ and $R$ are the equivalent MMC capacitance, inductance and resistance respectively. The equivalent circuit parameters can be expressed as

$$
\begin{align*}
C &= \frac{6C_0}{N} \\
L &= \frac{2L_0}{3} \\
R &= \frac{2R_0}{3}
\end{align*}
$$

where $C_0$ is the value of the submodule capacitance, $N$ is the number of inserted submodules in each bridge arm, $L_0$ is the value of the bridge arm reactor, and $R_0$ is the sum of on-state resistance of $N$ switching devices in normal operation of single-phase bridge arm (including IGBTs and diodes).

FIGURE 4. Simplified model of MMC before MMC is blocked. (a) The MMC structure. (b) Equivalent circuit model.

C. FAULT CURRENT CALCULATION METHOD FOR DC LINES

Accurate calculation of fault currents is the basis of the optimal configuration for fault current limiting devices. Meanwhile, the optimal configuration for the fault current limiting device should consider the most serious fault scenario that may occur in the HVDC grid. As shown in Fig. 5, a symmetrical monopole four-terminal MMC-HVDC grid is constructed to verify the proposed fault current calculation method. And calculates the fault current of the dc line for the case of pole-to-pole dc short-circuit fault at the beginning and end of the line. Table 1 shows the basic parameters of the four-terminal flexible dc power grid.

In Fig. 5, $f_i$ ($i = 1, 2, 3, 4, 5, 6, 7, 8$) is the pole-to-pole dc short-circuit fault at the outlet of the dc line. DB adopt the hybrid DCCB topology presented in Fig. 2. The CLR and the resistive FCL are installed at both ends of dc lines to limit the dc fault current and realize dc fault ride-through in the HVDC grid. The parameters of the four-terminal MMC-HVDC grid are listed in Table I.
The equivalent circuit of the four-terminal MMC-HVDC grid before FCL action.

As shown in Fig. 6, \( R_j \) and \( L_j \) (\( i, j = 1, 2, 3, 4 \)) are the resistance and inductance of the dc line respectively. \( L_{kx} (k = 1, 2, 3, 4, 5, 6, 7, 8) \) is the CLR at both ends of the dc line. \( C_i, L_i, \) and \( R_i \) are the equivalent MMC capacitance, inductance and resistance respectively. And the equation of state can be established as

\[
\begin{align*}
\dot{\mathbf{u}} &= \mathbf{R}\mathbf{i} + \mathbf{L}\dot{\mathbf{i}} \\
\mathbf{u} &= \mathbf{P}\mathbf{i}
\end{align*}
\]  

(2)

where \( \mathbf{u} = [u_1, u_2, u_3, u_4]^T \) is the node voltages matrix before FCL action, \( \mathbf{i} = [i_{12}, i_{23}, i_{30}, i_{04}, i_{41}]^T \) is the branch currents matrix before FCL action.
As shown in Fig. 7, current limiting resistors \((R_{55} \text{ and } R_{66})\) are put into the short-circuit path to suppress the fault current after FCL action. And the equation of state can be established as

\[
\begin{align*}
\mathbf{A} \mathbf{u}_t &= \mathbf{R} \mathbf{i}_t + \mathbf{L} \mathbf{i}_t \\
\mathbf{u}_t' &= \mathbf{P} \mathbf{i}_t
\end{align*}
\]

(3)

where \(\mathbf{u}_t = [u_{t1}, u_{t2}, u_{t3}, u_{t4}]^T\) is the node voltage matrix after FCL action. \(\mathbf{i}_t = [i_{t12}, i_{t23}, i_{t30}, i_{t04}, i_{t41}]^T\) is the branch current matrix after FCL action.

The concrete forms of correlation matrix \(\mathbf{A}\), initial resistance matrix \(\mathbf{R}\), inductance matrix \(\mathbf{L}\), matrix \(\mathbf{P}\) and modified resistance matrix \(\mathbf{R}_r\) are shown in Appendix.

The initial value matrix of node voltage and branch current is obtained by calculating the steady-state power flow of dc grid. The fault current of dc lines can be obtained by solving the simultaneous differential equations (2) and (3) using MATLAB.

At present, it is basically confirmed in the planned HVDC grid project that a 100-mH-level the CLR should be installed at both ends of the dc line to improve the survivability of dc grids under dc faults [9]. In order to validate the fault current calculation method, a pole-to-pole dc short-circuit fault is applied at \(f_5 = 2\) s. and all the CLR and FCL are 0.1 H and 10 \(\Omega\) respectively. Fig. 8 shows the comparison waveform between the simulation result and the numerical calculation result of dc line fault currents during the pole-to-pole dc short-circuit fault. It can be seen from the Fig. 8 that within 6 ms after the fault occurs, the numerical solution of dc line fault currents can fit accurately with the fault current waveforms obtained from simulation.

As can be seen in Fig. 9, since the CLR is configured at both ends of the dc line, the dc voltages at the outlet of MMC1 and MMC2 at the far end of the fault point change little within a few milliseconds after the occurrence of the pole-to-pole short circuit fault, the dc voltages at the outlet of MMC3 and MMC4 at the near end of the fault point decrease slowly within a few milliseconds after the occurrence of the pole-to-pole short circuit fault. Fig. 10 shows the ac-side current of each MMC after the pole-to-pole dc short-circuit fault occurs. When the dc voltage at the outlet of MMC does not drop very much, the ac-side current of MMC cannot be changed immediately, and there will be no obvious overcurrent phenomenon in ac system. With the continuous drop of the dc voltage at the outlet of MMC, the system gradually loses control of the ac output, and the ac-side current of MMC increases gradually. The dc voltage at the outlet of the MMC during a few milliseconds after the fault is calculated as

\[
\begin{align*}
\mathbf{u}_{dc} &= \mathbf{u}_t + \mathbf{L}_M (-\mathbf{A}^T) \mathbf{i}\mathbf{j} + \mathbf{R}_M (-\mathbf{A}^T) \mathbf{i}\mathbf{j} \\
\mathbf{u}_{dc} &= \mathbf{u}_t + \mathbf{L}_M (-\mathbf{A}^T) \mathbf{i}\mathbf{j} + \mathbf{R}_M (-\mathbf{A}^T) \mathbf{i}\mathbf{j}
\end{align*}
\]

(4)

where \(\mathbf{u}_{dc} = [u_{dc1}, u_{dc2}, u_{dc3}, u_{dc4}]^T\) and \(\mathbf{u}_a = [u_{dcr1}, u_{dcr2}, u_{dcr3}, u_{dcr4}]^T\) are respectively the dc voltage matrix before and after FCL action. \(\mathbf{L}_M\) is the equivalent inductance matrix of MMC, \(\mathbf{R}_M\) is the equivalent resistance matrix of MMC, and the mathematical form is as follows:

\[
\mathbf{L}_M =
\begin{bmatrix}
L_1 & 0 & 0 & 0 \\
0 & L_2 & 0 & 0 \\
0 & 0 & L_3 & 0 \\
0 & 0 & 0 & L_4
\end{bmatrix}
\]

(5)

\[
\mathbf{R}_M =
\begin{bmatrix}
R_1 & 0 & 0 & 0 \\
0 & R_2 & 0 & 0 \\
0 & 0 & R_3 & 0 \\
0 & 0 & 0 & R_4
\end{bmatrix}
\]

(6)

Therefore, the ac-side current of MMC can be calculated approximately in a very short time using the calculation formula of steady state for ac currents.

The fault current in the arms of MMC can be further calculated as

\[
\begin{align*}
\mathbf{i}_{f,T} &= -\frac{1}{3} i_{f,A} - \frac{1}{2} i_{f,B} \\
\mathbf{i}_{f,B} &= -\frac{1}{3} i_{f,A} + \frac{1}{2} i_{f,B}
\end{align*}
\]

(7)

where \(i_{f,T}\) and \(i_{f,B}\) \((i = 1, 2, 3, 4; j = a, b, c)\) are the fault current flowing through the upper and lower bridge arms of \(f\) phase of MMC\(i\) respectively. \(i_{f,A}\) is the ac current flowing through the phase \(f\) at the ac side of MMC\(i\). And \(i_{f}\) is the dc current at the outlet of MMC\(i\).

Fig. 11 shows the comparison waveform between the simulation result and the numerical calculation result of fault currents in the arms of MMC3 during the pole-to-pole dc short-circuit fault. Similarly, within 6 ms after the fault occurs, the numerical solution of the fault current in the
arms of MMC can fit accurately with the fault current waveform obtained from simulation.

As mentioned above, the main objective of this paper is to find the optimal locations of fault current limiting devices to ensure the continuous operation of HVDC grids under dc faults. CLRs can be installed in series with the dc lines to suppress the fault current, however, the excessive inductance value of the CLR will decrease dynamic performances of the dc system, even lead to instability of the dc system. It is necessary to cooperate with the active current limiting device such as FCL to suppress fault current synergistically.

Taking performances of the dc system and capital costs of the fault current limiting device into account, a multi-objective optimal model was established which the objective functions are both the optimal the fault current limiting effects, the minimum total inductances of CLRs and the minimum number of FCLs installations in this paper.

1) Optimization of the fault current limiting effect

In order to ensure that DCCBs can reliably cut off the dc fault current after a pole-to-pole dc short-circuit fault occurs in the dc grid. The fault current flowing through both sides of the dc line where the fault is located should always be less than the maximum breaking current of the DCCB with a certain surplus. In this paper, the arithmetic average value of the ratio of the fault current flowing through both sides of the dc line to the maximum breaking current of the DCCB under all fault conditions is taken as an indicator reflecting the global current limiting effect of dc system. The objective function $f_1$ is defined as

$$f_1 = \min \frac{1}{2n} \sum_{i=1}^{n} \left| I_{f_i}(t_1) \right| + \left| I_{f_i}(t_3) \right|$$

where $n$ is the number of fault scenarios considered. $t_1$ is the action time of main dc breaker after the fault occurs. $I_0(t_1)$ and $I_0(t_3)$ are respectively the fault current flowing through both sides of the dc line where the fault $i$ is located. $I_{D_{\text{max}}}$ is the maximum breaking current of the DCCB. The smaller the value of the objective function $f_1$, the better the fault current limiting effect.

2) Minimization of the total inductances of CLRs

Under the condition that HVDC grids can realize dc fault ride-through operation under dc faults, reducing the total inductances of CLRs as much as possible can not only improve system performances but also reduce capital costs. The objective function $f_2$ is defined as

$$f_2 = \min \sum_{C} L_C$$

where $N_C$ is the total number of CLRs installed on the dc lines, $L_C$ is the inductance value of the CLR.

3) Minimization the number of FCLs installations

In view of the fact that it is difficult to meet the fault ride-through requirements of converter valves in actual HVDC projects to suppress fault current only by using CLRs [26], FCL can limit the fault current further to ensure that DCCBs cut off the dc fault current without MMC blocking. However, the capital cost of FCLs is expensive, and the number and location of FCLs installations need to be coordinated with the

III. PROBLEM FORMULATION

A. OBJECTIVE FUNCTIONS

FIGURE 9. The dc voltage at the outlet of each MMC during a pole-to-pole short circuit fault.

FIGURE 10. The ac-side current of MMC.

FIGURE 11. Bridge arm fault current results from simulation and numerical calculation.
parameter selection of CLRs. The objective function \( f_i \) is defined as
\[
f_i = \min N_F
\]
where \( N_F \) is the total number of FCLs installed on the dc lines.

B. PROBLEM CONSTRAINTS

Constraints include DCCBs current breaking capacity constraints, converter valves overcurrent protection constraints, CLRs sizing constraints and converter station outlet dc voltage constraints.

1) DCCBs current breaking capacity constraints

The fault current flowing through the DCCBs after the fault occurs should always be less than the maximum breaking current of the DCCB with a certain surplus. Therefore, the fault current has to be satisfied
\[
\begin{align*}
I_{D,(t_i)} &\leq k_1, \\
I_{D_{\max},(t_i)} &\leq k_1,
\end{align*}
\]
where \( N_D \) is the total number of DCCBs installed on the dc lines. \( t_i \) is the action time of FCLs after the fault occurs. \( I_{D,(t_i)} \) and \( I_{D_{\max},(t_i)} \) are dc fault currents flowing through the DB. \( k_1 \) is the reliability coefficient. In this paper, we adopt \( k_1 = 0.9 \).

2) Converter valves overcurrent protection constraints

Due to the poor overcurrent capability of the IGBT, MMC will be blocked to protect IGBTs as soon as the fault current in the arms of MMC exceeds two times the rated current of the IGBTs. Therefore, the fault current flowing through the IGBTs must be within two times the rated current of the IGBTs to avoid converter blocking. The converter valves overcurrent protection constraints can be expressed as
\[
\begin{align*}
\frac{1}{3} I_{a,(t_i)} + \frac{\sqrt{2}}{2} I_{a} &\leq 2 I_G - I_A, \\
\frac{1}{3} I_{a,(t_3)} + \frac{\sqrt{2}}{2} I_{a} &\leq 2 I_G - I_A,
\end{align*}
\]
where \( N_M \) is the total number of converter stations. \( I_{a,(t_i)} \) and \( I_{a,(t_3)} \) are the dc fault currents at the outlet of MMCi. \( I_a \) is the RMS value of phase current on the ac-side of the MMCi. \( I_G \) is the rated current of the IGBTs. \( I_A \) is the safety margin.

3) CLRs sizing constraints

A certain size of CLR should be configured at both ends of the dc line so that the dc fault is selectively detected and successfully isolated without MMC blocking. However, the inductance value of the CLR cannot increase indefinitely, which should have a reasonable value interval. The inductance value of each CLR must be kept within the allowed range as
\[
L_{\text{min}} \leq L_{C,i} \leq L_{\text{max}}, \quad i = 1,2,\cdots, N_C
\]
where \( L_{\text{min}} \) is the minimum inductance value to satisfy CLR to form the boundary of the dc line protection area. \( L_{\text{max}} \) is the maximum inductance value that satisfies the dynamic response requirements of the dc system.

4) Converter station outlet dc voltage constraints

In order to prevent excessive dc voltage drop during dc grid ride-through operation, and to ensure continuous operation of the dc grid under dc faults. The dc voltage should be maintained at a safe level before the dc fault is isolated.
\[
\begin{align*}
U_{\text{dc},(t_i)} &\geq k_2 U_{\text{dc}}, \\
U_{\text{dc},(t_3)} &\geq k_2 U_{\text{dc}},
\end{align*}
\]
where \( U_{\text{dc},(t_i)} \) and \( U_{\text{dc},(t_3)} \) are the dc voltages at the outlet of MMCi. \( U_{\text{dc}} \) is the rated dc voltage of the dc system. \( k_2 \) is the reliability coefficient. In this paper, we adopt \( k_2 = 0.6 \).

C. MULTIPLE OBJECTIVE OPTIMIZATION

By aggregating the objectives and constraints, the multi-objective optimal problem can be written as
\[
\begin{align*}
\min f(x) &= [f_1(x), f_2(x), f_3(x)] \\
\text{s.t. } g_i(x) &\leq 0, \quad i = 1, 2, \cdots, m
\end{align*}
\]
where \( x \) is the decision variable vector. \( f(x) \) is the vector of the objective function and \( g_i(x) \) is the inequality constraints. \( m \) is the number of inequality constraints.

In the vector function \( f(x) \), the objectives are in conflict with each other, and are expressed in different units. Within a reasonable range, the larger the inductance value of CLRs and the more the number of FCLs, the better the fault current limiting effect, but the higher the corresponding costs. It is not realistic to optimize multiple objectives simultaneously. Therefore, the optimal solution of multi-objective optimization problem is a set of solutions that are no worse than other solutions, namely Pareto optimal solutions [27].

Some concepts regarding the Pareto optimal solution are introduced as follows.

Pareto dominance: For two feasible solutions \( x_1 \in S \) and \( x_2 \in S \), S is the feasible region defined by constraints. \( x_1 \) is said to dominate \( x_2 \) if and only if
\[
\forall i \in \{1,2,3\}, f_i(x_1) \leq f_i(x_2)
\]
\[
\exists i \in \{1,2,3\}, f_i(x_1) < f_i(x_2)
\]

Pareto Optimal solution set: A feasible solution \( x_1 \in S \) is said to be a Pareto optimal solution (non-dominated solution) if and only if there is no another feasible solution \( x_2 \in S \) that dominates \( x_1 \). The solution set consisting of all Pareto optimal solutions is the Pareto optimal solution set.

IV. PARETO OPTIMAL SOLUTION OF MULTI-OBJECTIVE OPTIMAL CONFIGURATION SCHEME FOR CURRENT LIMITING DEVICES

A. MULTI-OBJECTIVE SHUFFLED FROG-LEAPING ALGORITHM (MOSFLA)

The shuffled frog leaping algorithm (SFLA) is a new meta-heuristic optimization method proposed by Eusuff and Lansey in 2003 [28], which has the advantages of rapid convergence, simple and practical, etc. And it has been applied in the unit commitment problem [29], photovoltaic model identification [30], optimal reactive power dispatch [31] and so on. In recent years, some multi-objective
optimization algorithms based on SFLA have been proposed and applied to the field of multi-objective optimization [32], [33]. In this paper, the multi-objective shuffled frog-leaping algorithm (MOSFLA) is used to solve multi-objective optimal configuration problem for CLRs and FCLs. The details of proposed MOSFLA are described as follows.

**Step 1:** Initial parameter settings.

Initial parameters include the number of ethnic groups $m$, the frog individual number $n$ in the ethnic groups, the number of ethnic internal iterations $N_e$, the total number of population evolution $N_p$, and the maximum allowed step size $S_{max}$.

**Step 2:** Initial population generation.

The initial frog population can be described as

$$X = [x_1, \ldots, x_F]^T$$

where $F=m\times n$ is the population size. Each frog represents a configuration scheme of fault current limiting devices, and the $i$th frog can be shown as

$$x_i = [CLR_1, \ldots, CLR_n, FCL_1, \ldots, FCL_n], \quad i = 1, \ldots, F$$

where $CLR_j (j=1, \ldots, 8)$ is the inducance value of the CLR, and the value range of $CLR$ is $[L_{min}, L_{max}]$. $FCL_k (k=1, \ldots, 8)$ is the discrete variable representing the installation status of the FCL in the dc grid. $FCL = 0$ indicates that the FCL is not configured, $FCL = 1$ indicates that the FCL is configured.

**Step 3:** Fitness values calculation.

Evaluate objective functions and constraints of each individual frog and add penalty function if there is any constraint violation. The fitness function consists of the objective function and the penalty function. And the smaller the value of the fitness function is, the easier it is for individual frog to be retained. The fitness function is defined as

$$fitness_1(x_i) = f_1(x_i) + 10^4 V(x_i)$$
$$fitness_2(x_i) = f_2(x_i) + 10^4 V(x_i)$$
$$fitness_3(x_i) = f_3(x_i) + 10^4 V(x_i)$$

$$V(x_i) = \alpha \sum_{j=1}^{N_e} |p_{DB}(x_i)| + \beta \sum_{j=1}^{N_b} |p_{ana}(x_i)| + \epsilon \sum_{j=1}^{N_a} |p_{DC}(x_i)|$$

where $fitness_1(x_i)$, $fitness_2(x_i)$ and $fitness_3(x_i)$ are the fitness functions of the objective function $f_1(x_i)$, $f_2(x_i)$ and $f_3(x_i)$ respectively. $V(x_i)$ is the degree violating the constraints. $\lambda_1$, $\lambda_2$ and $\lambda_3$ are the penalty coefficients corresponding to the objective function $f_1(x_i)$, $f_2(x_i)$ and $f_3(x_i)$ respectively. Their values are positive integers, which are determined by the order of magnitude of the objective function and the penalty function. $N_b$, $N_a$ and $N_a$ are the number of constraint violations of DCCBs current breaking capacity constraints, converter valves overcurrent protection constraints and converter station outlet dc voltage constraints respectively. $p_{DB}(x_i)$, $p_{ana}(x_i)$ and $p_{DC}(x_i)$ are the $j$th over-limit degree of the DC breaker breaking capacity constraint, the $k$th over-limit degree of the converter overcurrent protection constraint and the $l$th over-limit degree of the converter station outlet dc voltage constraint respectively. $a$, $b$ and $c$ are weight coefficients reflecting the importance of DCCBs current breaking capacity constraints, converter valves overcurrent protection constraints and converter station outlet dc voltage constraints respectively.

**Step 4:** The ethnic groups division.

The initial frog population is sorted by means of the fast non-dominated sorting method [34]. Assume that the set of all frogs dominated by individual frog $x_i$ is $W_i$, denoted as

$$W_i = \{ x_j | x_j \text{ is dominated by } x_i, x_j \in X \}$$

Assume that $n_i$ is the number of frogs in $W_i$ and the initial frog population is sorted in descending order by $n_i$. If two frogs have the same $n_i$, they are arranged randomly.

The frog with the largest $n_i$ in the frog population will be saved into the external population $X_p$, which is the non-inferior solution set. And a frog is randomly selected from $X_p$ as the global optimal individual $x_e$.

The frog population is divided into $m$ ethnic groups with $n$ frogs in each ethnic group. The first frog of the sorted frog population is put in the first ethnic group, the second frog is put in the second ethnic group, the $m$th frog is put in the $m$th ethnic group, the $(m+1)$th frog is put in the first ethnic group and so on.

**Step 5:** Evolution within the ethnic groups.

For each ethnic group, the frog with the largest $n_i$ is randomly selected as the optimal individual $x_e$ in each ethnic group, and the frog with the smallest $n_i$ is randomly selected as the worst individual $x_w$ in each ethnic group. $x_w$ is updated as follows

$$\begin{cases} S = r(x_e - x_w) \\ x_{new} = x_w + S, \quad -S_{max} \leq S \leq S_{max} \end{cases}$$

where $S$ is the change of the frog position. $r$ is a random number between 0 and 1. Considering that the configuration position of FCL is a discrete variable, the real numbers are rounded up to the nearest integer to obtain the discrete variable.

The fitness value of generated $x_{new}$ is calculated. If $x_{new}$ dominates $x_w$, then $x_{new}$ will replace the $x_e$ in the ethnic group. Otherwise, the calculation of equation (21) is repeated, but in this case $x_e$ is replaced by $x_w$. If $x_{new}$ still cannot dominate $x_e$, then a new individual $x_{new}$ is randomly generated in the feasible region to replace the worst individual $x_w$ in the ethnic group. The above update process is repeated until the number of ethnic internal iterations $N_e$ is reached.

**Step 6:** Iterative global optimization.

The updated ethnic groups are mixed with others to generate a new population, and steps 4 and 5 are repeated. The above process is repeated until the total number of population evolution $N_p$ is reached.

The application oriented flowchart of MOSFLA is illustrated in the appendix.

**B. THE BEST COMPROMISE SOLUTION**

In order to provide a reference for decision makers to choose the best compromise solution from Pareto optimal solution set. In this paper, the best compromise solution is extracted.
from the Pareto optimal solution set based on the fuzzy theory [35]. The fuzzy membership function is defined as

$$
\mu_i = \begin{cases} 
1, & f_i \leq f_{i,\min} \\
\frac{f_{i,\max} - f_i}{f_{i,\max} - f_{i,\min}}, & f_{i,\min} \leq f_i \leq f_{i,\max} \\
0, & f_{i,\max} \leq f_i
\end{cases} \quad (22)
$$

where $f_i$ is the value of the $i$th objective function. $f_{i,\max}$ and $f_{i,\min}$ are upper and lower limits of the objective function respectively. $\mu_i = 0$ means that decision makers are completely dissatisfied with the value of an objective function, and $\mu_i = 1$ means that decision makers are completely satisfied with the value of an objective function.

In this paper, $\mu$ is used to represent the satisfaction of decision makers with the configuration scheme of fault current limiting devices. The best compromise solution is the solution with the highest $\mu$

$$
\mu = \frac{1}{n} \sum_{i=1}^{n} \mu_i \quad (23)
$$

where $\mu$ is the normalized value of the satisfaction. $n$ is the number of the objective functions.

V. SIMULATION VALIDATIONS AND RESULT ANALYSIS

In order to verify the rationality of the proposed collaborative optimal configuration scheme of CLRs and FCLs, a symmetrical monopole four-terminal MMC-HVDC grid shown in Fig. 5 is simulated in PSCAD/EMTDC.

In the normal operation, MMC1 uses constant dc voltage control mode with the voltage of 500 kV, and meanwhile absorbs active power from the dc system. MMC2, MMC3 and MMC4 use constant active power control mode and inject 800 MW, 600 MW and -600 MW power into the dc system, respectively. In this paper, the fault current limiting device is symmetrically configured at the positive and negative pole lines of the dc grid. The maximum breaking current of the hybrid DCCB is 9 kA, and the time from the occurrence of the fault to the main dc breaker action is 6 ms. The rated current of IGBT is 2 kA. Considering the limitation of resilience volume and heat dissipation capacity, the current limiting resistor is 10 $\Omega$.

A. SIMULATION RESULTS AND DISCUSSION

The proposed MOSFLA program is performed on the MATLAB software platform to obtain the Pareto optimal solution set. Parameters used in MOSFLA are set as $m = 20$, $n = 10$, $N_e = 25$, $N_s = 200$, $S_{\max} = 0.02$, $L_{\min} = 0.1$ H, $L_{\max} = 0.2$ H, and the weight coefficients $a = b = c = 1/3$.

Fig. 12 shows the Pareto optimal front obtained by MOSFLA program. As shown in Fig. 12(b), the blue, green and red points represent the Pareto optimal solution when configuring 6, 7 and 8 FCLs respectively.

By comparing the Pareto optimal front when the number of FCLs is 6, 7 and 8, it can be seen that the total inductance of CLRs is basically inversely proportional to the fault current limiting effect. The greater the total inductance value of the CLRs, the better the fault current limiting effect. At the same time, with the increase of the number of FCLs in the dc grid, the fault current limiting effect of the dc system will also be improved.

As shown in Fig. 12(b), B(8) is the most conservative configuration scheme for fault current limiting devices. In contrast, the configuration scheme corresponding to A(6) requires the least number of FCLs. And the total inductance of CLRs is small, the dynamic performance of the dc system is relatively better, the fault current limiting effect is relatively poor.

The normalized value of the satisfaction of the decision variable vector in the Pareto optimal solution set is calculated according to the fuzzy membership function proposed in section IV, and the solution C(6) with the largest normalized value of the satisfaction is selected as the best compromise solution, as shown in Fig. 12(b). The corresponding optimization result of C(6) is as follows: $L_{C1} = 0.184$ H, $L_{C2} = 0.164$, $L_{C3} = 0.172$, $L_{C4} = 0.179$, $L_{C5} = 0.169$, $L_{C6} = 0.136$, $L_{C7} = 0.159$, $L_{C8} = 0.153$, and only FCL2, FCL3, FCL5, FCL6, FCL7, FCL8 are configured in the dc grid.

FIGURE 12. The Pareto optimal front.

B. SIMULATION AND VERIFICATION

The best compromise solution C(6) is applied to the four-terminal MMC-HVDC grid, and a pole-to-pole dc short circuit fault is assumed to occur at $f_5$ location at $t = 2$ s. The simulation results are shown in Figs. 13-16.

As shown in Fig. 13, the normal dc voltage of the system is around 500 kV. When a pole-to-pole dc short circuit fault

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happened at $t = 2$ s, the dc voltage begins to drop, and after the dc fault is isolated, the dc voltage restores to 500 kV.

As shown in Fig. 14, the peak amplitude of the fault current happens at 6 ms after the fault occurs, which is less than the DCCBs current breaking capacity (9 kA), indicating the dc fault current can be cut off by the DCCBs safely.

Fig. 15 shows the simulation results of the active power of each MMC. After the fault occurs, the active power of the converter station with the constant dc voltage control fluctuates greatly, and the active power of the converter station with the constant active power control is basically unaffected. Active power gradually restores stability after the dc fault is isolated.

Fig. 16 shows the simulation results of the bridge arm currents of MMC3. After the fault occurs, the arm currents of MMC3 increases sharply but not reach the threshold of currents of MMC3. After the fault occurs, the arm currents of MMC3 fluctuates greatly, and the active power of the converter station  with the constant dc voltage control

![Image](https://example.com/image.png)

**FIGURE 13.** DC voltages at the outlet of MMC1-MMC4.

![Image](https://example.com/image.png)

**FIGURE 14.** DC currents at the outlet of MMC1-MMC4.

![Image](https://example.com/image.png)

**FIGURE 15.** Active powers of MMC1-MMC4.

![Image](https://example.com/image.png)

**FIGURE 16.** Bridge arm currents of MMC3.

In order to further validate the effectiveness of the Pareto optimal front, the obtained Pareto optimum solution is applied to the four-terminal MMC-HVDC grid, and the pole-to-pole dc short-circuit fault $f_1 \sim f_6$ (at $t = 2.0$ s) is set respectively to verify whether the configuration schemes meet the requirements of the dc grid.

The partially configuration schemes for fault current limiting devices are shown in Table II. The simulation results under some configuration schemes are shown in Table III.

<table>
<thead>
<tr>
<th>TABLE II</th>
<th>PARTIALLY OPTIMIZED CONFIGURATION SCHEME</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scheme</td>
<td>no fault current limiting devices</td>
</tr>
<tr>
<td>only CLR</td>
<td>[0.2,0.2,0.2,0.2,0.2,0.2,0.2,0.2,0.2,0.0,0.0,0.0,0.0,0.0]</td>
</tr>
<tr>
<td>A(6)</td>
<td>[0.164,0.163,0.167,0.145,0.168,0.162,0.158,0.147,0.1,0.1,0.1,0.1,0.1]</td>
</tr>
<tr>
<td>B(6)</td>
<td>[0.175,0.189,0.176,0.178,0.194,0.191,0.157,0.184,1.1,1.1,1.1,1.0]</td>
</tr>
<tr>
<td>A(8)</td>
<td>[0.126,0.162,0.163,0.154,0.172,0.135,0.156,0.146,1.1,1.1,1.1,1.1]</td>
</tr>
<tr>
<td>B(8)</td>
<td>[0.182,0.179,0.175,0.158,0.198,0.183,0.154,0.192,1.1,1.1,1.1,1.1]</td>
</tr>
<tr>
<td>C(6)</td>
<td>[0.184,0.164,0.172,0.179,0.169,0.136,0.159,0.153,0.1,0.1,1.1,1.1]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TABLE III</th>
<th>SIMULATION RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scheme</td>
<td>The total inductances of CLRs /H</td>
</tr>
<tr>
<td>no fault current limiting devices</td>
<td>0</td>
</tr>
<tr>
<td>only CLR</td>
<td>1.6</td>
</tr>
<tr>
<td>A(6)</td>
<td>1.274</td>
</tr>
<tr>
<td>B(6)</td>
<td>1.444</td>
</tr>
<tr>
<td>A(8)</td>
<td>1.214</td>
</tr>
<tr>
<td>B(8)</td>
<td>1.421</td>
</tr>
<tr>
<td>C(6)</td>
<td>1.316</td>
</tr>
</tbody>
</table>

From Table III, it can be seen that although the configuration scheme of with only 0.2 H CLR installed at both ends of the dc line has better fault current limiting effect, the dc system cannot realize fault ride-through due to the fact that it does not meet the converter valves overcurrent protection constraints under extreme conditions. The collaborative optimal configuration scheme of CLRs and FCLs can ensure the safe and reliable operation of HVDC grids under dc faults. Decision makers can choose an appropriate configuration scheme in the Pareto optimal solution set based on the actual situation.

VI. CONCLUSION

This paper proposes a collaborative optimal configuration method of CLRs and FCLs for HVDC grids, which improves the fault ride-through capability of HVDC grids. The main contributions include the following:
1) In this paper, a method for calculating the fault current of dc lines and the fault current of bridge arm considering the collaboration of CLR and FCL is proposed.

2) Consideration of the constraints of the DCCBs current breaking capacity, the converter valves overcurrent protection, the boundary of the dc line protection area, the dynamic performance of the dc system and the constraints of the converter station outlet dc voltage to ensure continuous and reliable operation of the dc system under dc faults.

3) All the steps in the presented methodology are independent of the dc grid connection topology. Therefore, the presented methodology for optimal configuration of fault current limiting devices can be applied to all types of meshed, ring or radial dc grids.

**APPENDIX**

\[
A= \begin{bmatrix}
1 & -1 & 0 & 0 \\
0 & 1 & -1 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & -1 \\
-1 & 0 & 0 & 1 \\
\end{bmatrix}
\]

\[
R_1 = \begin{bmatrix}
R_1 + R_2 + 2R_{12} & -R_2 & 0 & 0 & -R_4 \\
-R_2 & R_2 + R_3 + 2R_{23} & -R_3 & 0 & 0 \\
0 & -R_3 & R_3 & 0 & 0 \\
0 & 0 & 0 & R_4 + 2R_{34} & -R_4 \\
-R_4 & 0 & 0 & -R_4 & R_4 + R_4 + 2R_{41} \\
\end{bmatrix}
\]

\[
L = \begin{bmatrix}
L_1 + L_2 + 2L_{C1} + 2L_{C2} + 2L_{t2} & -L_2 & 0 & 0 & -L_4 \\
-L_2 & L_2 + L_3 + 2L_{C3} + 2L_{C4} + 2L_{23} & -L_3 & 0 & 0 \\
0 & -L_3 & L_3 + 2L_{C5} & 0 & 0 \\
0 & 0 & 0 & L_4 + 2L_{C6} + 2L_{34} & -L_4 \\
-L_4 & 0 & 0 & -L_4 & L_4 + L_4 + 2L_{C7} + 2L_{C8} + 2L_{41} \\
\end{bmatrix}
\]

\[
R = \begin{bmatrix}
R_1 + R_2 + 2R_{12} & -R_2 & 0 & 0 & -R_4 \\
-R_2 & R_2 + R_3 + 2R_{23} & -R_3 & 0 & 0 \\
0 & -R_3 & R_3 + 2R_{F5} & 0 & 0 \\
0 & 0 & 0 & R_4 + 2R_{F6} + 2R_{34} & -R_4 \\
-R_4 & 0 & 0 & -R_4 & R_4 + R_4 + 2R_{41} \\
\end{bmatrix}
\]

\[
P = \begin{bmatrix}
1/C_1 & 0 & 0 & 0 \\
0 & 1/C_2 & 0 & 0 \\
0 & 0 & 1/C_3 & 0 \\
0 & 0 & 0 & 1/C_4 \\
\end{bmatrix}
\]
Start

- Input system parameters and initialize MOSFLA parameters
- Generate the population of $F$ frogs randomly
- Fitness function evaluation for each frog
- Sort the population by fast non-dominated sorting method and find the global optimal individual $x_g$
- Divide $F$ into $m$ ethnic groups
- Local search within each ethnic group
- Whether the number of ethnic internal iterations $N_e$ is reached
  - Yes
  - Determine the optimal individual $x_b$ and the worst individual $x_w$
  - Replace $x_b$ by $x_g$ and update position of worst frog $x_w$ by equation (21)
  - Complete a local search within an ethnic group
  - Replace the worst frog $x_w$ with new frog $x_{new}$
  - End

End

FIGURE 17. Flowchart of MOSFLA

REFERENCES


