Parametric Analysis and Optimization of a DC Current Flow Controller in Meshed MTDC Grids

Puyu Wang¹,², Member, IEEE, Na Deng³, Xiao-Ping Zhang⁴, Senior Member, IEEE, Ningqiang Jiang¹, Senior Member, IEEE

¹Department of Electrical Engineering, School of Automation, Nanjing University of Science and Technology, Nanjing, Jiangsu, 210094 China
²Jiangsu Provincial Key Laboratory of Smart Grid Technology and Equipment, Nanjing, Jiangsu, 210096 China
³ABB Sifang Power System Co., Ltd, Jia 3, Anxiang Avenue, Tianzhu Airport Industrial Zone, Shunyi District, Beijing, 101300 China
⁴Department of Electronic Electrical and Systems Engineering, School of Engineering, University of Birmingham, Birmingham, B15 2TT UK

Corresponding author: Puyu Wang (e-mail: puyu.wang@njust.edu.cn).

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ABSTRACT A DC current flow controller (CFC) in a multi-terminal HVDC (MTDC) grid has the functionality of adjusting and optimizing the power flow on the DC lines. In this paper, the impact of DC CFC parameters on the system stability and dynamic performance is analyzed with three contributions: (1) A mathematical model and a small-signal model of the DC CFC in a meshed MTDC grid are derived; (2) Considering the impact of controller parameters on gain margins, phase margins and cut-off frequencies, the stability analysis is performed in the frequency domain. A parametric optimization scheme is proposed with deployment of the control variate method and scanning method; (3) A method is proposed to determine the size range and the voltage reference of the common capacitance based on their influence on dynamic behaviors. Two DC CFC equipped multi-terminal meshed HVDC grids are established in PSCAD/EMTDC. Simulation results justify the effectiveness of the theoretical analysis. The proposed parametric selection scheme is demonstrated by dynamic responses shown in the comparative studies.

INDEX TERMS Multi-terminal HVDC (MTDC), DC current flow controller (CFC), small-signal analysis, parametric analysis and optimization.

I. INTRODUCTION

In the past several decades, there has been an increasing number of high-voltage direct current (HVDC) transmission lines in power systems. Most of the HVDC systems have two terminals, including types of line-commutated converter (LCC) and voltage-sourced converter (VSC) [1]-[3]. Several multi-terminal HVDC (MTDC) systems have emerged to enhance the transmission capacity and reliability, such as the European supergrid project [4] and China Zhou’shan five-terminal HVDC project [5]. Following the history of AC networks, the DC lines are developing gradually from point-to-point connections to multi-end radial connections, and will finally form meshed DC networks. A generalized MTDC grid, including different types of converters, is shown in Fig. 1.

In comparison with the conventional AC grid, there are still many existing problems for DC power systems after forming meshed topologies, particularly the issue of current/
are operating close to its maximum limits or even overloaded, while other DC lines are underutilized. Therefore, it is essential to introduce DC current flow control devices so as to enhance the control degrees of freedom and to optimize the power flow distribution in MTDC grids.

As aforementioned above, the DC power flows in an MTDC network are mainly determined by the line resistances and line terminal voltages. Hence, the DC current flow control approach can be generally classified into two categories, i.e. by means of (a) adjustable resistors; (b) controllable voltage sources.

The concept of method (a) is by changing the equivalent DC line resistance, i.e. inserting variable resistor(s) into a DC line. This method was firstly proposed in [7] and could accurately control the power flow with easy implementation. However, its drawbacks were (i) large power losses due to frequent switching-in resistance and (ii) the lack of capacity to achieve bi-directional control of DC power flow because of the unidirectional increase of line resistance.

For method (b), there are two approaches, i.e. by means of (1) using a DC-DC transformer; (2) inserting an equivalent voltage source. The first approach is to put a DC transformer in series into a DC line so as to adjust the DC power flow by varying the voltage ratio between the transformer [8-10]. The DC transformer can also be used to interconnect DC networks with different voltage ratings and to isolate DC faults. However, the application of this approach is mainly limited by the high losses and cost, since all power transferred has to pass the DC-DC transformer during the control process.

In comparison with the former approach, method (2), i.e. inserting an equivalent voltage source, is proved to have advantages of lower operational losses and reduced topological complexity [11-21]. This is due to the fact that the control of DC power flow is achieved by changing the line terminal voltages via inserting an adjustable voltage source, not necessitating the control device to undertake all voltage ratings and power transferred. The adjustable in-line voltage source can either be provided by external power sources outside the MTDC grid [12-15], or be achieved by the energy exchanges between adjacent DC lines [16-21]. The latter approach is more favored and deployed in practical applications, since it does not require external equipment, which saves both the cost and space. In [16], a new interline DC power flow controller (IDCPFC) was proposed and bi-directional power flow control was achieved. Since modular design was not applied in the IDCPFC, the scalability of the proposed topology was not facilitated. In [17], an m-port DC power flow controller (MDCPFC), which comprised MMC AC/DC converters and an interconnected three-phase three-winding AC transformer, was proposed for DC power flow control without requiring power exchange with an external AC network. However, the requirement of MMC AC/DC converters and AC transformers increased the total cost and space in the MDCPFC. In [18], a cascaded power flow controller (CPFC) with a two-layer control strategy was proposed. The CPFC was proposed with an average model of a DC-DC converter, i.e. controlled current and voltage sources, in which a detailed topology of the CPFC was not provided. In [19], a two-line DC current flow controller (CFC), which comprised two full-bridge DC-DC converter sharing a common capacitor, was proposed. The controllable voltage sources were implemented by altering the current flowing into the common capacitor. The control strategies of the DC CFC under steady-state operating conditions were proposed in [20]. A small-signal model and control system designed were developed in [21].

This paper further investigates the parametric selection and optimization of the DC CFC in a meshed MTDC grid with the main contributions as follows.

1) Regarding a two-line DC CFC equipped three-terminal HVDC grid, a mathematical model and a small-signal model are derived;
2) The system stability in the frequency domain is analyzed. The impact of parametric selections of the proportional gains and integral gains in the control systems of the DC CFC on the gain margins and phase margins is analyzed. A parameter optimization scheme is proposed;
3) The impact of the parametric selections of the common capacitor of the DC CFC and the capacitor voltage reference setting on the system dynamic performance is analyzed. A principle regarding the selection of the parameters is proposed.

The rest of this paper is organized as follows. Section II introduces the system configuration. A comprehensive mathematical model is derived with the calculations of steady-state operating points. A small-signal model is derived in Section III and the system stability is analyzed in the frequency domain. The impact of the control parameters of the DC CFC on the system gain margins and phase margins is analyzed in Section IV and a parameter optimization scheme is proposed. In Section V, the impact of the parameters of the DC CFC on system dynamic behaviors is analyzed. In addition, a principle of the selection ranges of the common capacitor and capacitor voltage reference is proposed.

II. SYSTEM CONFIGURATION, MATHEMATICAL MODEL, AND STABILITY ANALYSIS

A. SYSTEM CONFIGURATION

Fig. 2(a) shows a three-terminal meshed HVDC grid equipped a two-line DC CFC. $T_n$ ($n = 1, 2, 3$) denotes each terminal of the MTDC system; MMC-$n$ denotes the MMC at each terminal; SM-$k$ ($k = 1, 2$) denotes the DC-DC converter in the DC CFC. Fig. 2(b) presents the configuration of the two-line DC CFC. It has two full-
bridge DC-DC converters and one energy storage capacitor, where each converter has four IGBTs. Both DC-DC converters are interconnected through the capacitor as an energy exchange hub in parallel, which forms the two-line DC CFC.

B. MATHEMATICAL MODEL

Regarding SM-1 and SM-2 in the two-line DC CFC, \( S_{a1} \) and \( S_{a2} \) have the same switching pattern, thus they are given the same name of \( S_a \). Similarly, both \( S_{b1} \) and \( S_{b2} \) are named as \( S_b \).

For each full bridge, the two switches in the three pairs, \( S_a \) and \( S_b \), \( S_{11} \) and \( S_{12} \), \( S_{22} \) and \( S_{23} \), are switched complementarily. Fig. 3 depicts the switching characteristics of the switches.

The output voltage \( v_{SM} \) of a SM has three instant values:

1) \( v_{SM} = 0 \) when both the upper IGBTs (\( S_a \), \( S_{a4} \)) are switched on and both lower IGBTs (\( S_b \), \( S_{b4} \)) are switched off or vice versa. The common capacitor is bypassed under this switching mode.

2) \( v_{SM} = v_e \) when both \( S_a \) and \( S_{a4} \) are switched on and both \( S_b \) and \( S_{b4} \) are switched off. The capacitor is charged.

3) \( v_{SM} = -v_e \) when both \( S_a \), \( S_{a4} \) are switched on and both \( S_b \), \( S_{b4} \) are switched off. The capacitor is discharged.

The two-line DC CFC can be regarded as two controllable voltage sources, \( e_{12} \) and \( e_{13} \), installed in serial with two DC branches. The control of the voltage sources depends on the operation modes of SMs, which are summarized in Table I.

<table>
<thead>
<tr>
<th>Switching Modes ((m))</th>
<th>Operating Modes</th>
<th>( S_a )</th>
<th>( S_b )</th>
<th>( S_{11} )</th>
<th>( S_{12} )</th>
<th>SM Voltage ((V_{SM}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bypass ((m_1))</td>
<td>OFF</td>
<td>OFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charge ((m_2))</td>
<td>ON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Discharge ((m_3))</td>
<td>OFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bypass ((m_4))</td>
<td>OFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

According to Fig. 3 and Table I, the relationship between the switching modes, \( m_i (i = 1, \ldots, 4) \) and the duty cycles, \( d_j (j = a, \ldots, d) \) can be derived as follows:

\[
\begin{align*}
    m_1 &= \min \{d_a, d_d\} \\
    m_2 &= \max \{0, d_a - d_d\} \\
    m_3 &= \max \{0, d_e - d_a\} \\
    m_4 &= 1 - \max \{d_e, d_d\}
\end{align*}
\]  

Hence, the average output voltages of SM-1 and SM-2 in a control period are:

\[
\begin{align*}
    e_{12} &= \sum_{i=1}^{d_a} m_i \cdot v_{SM-1} = (m_a - m_1) \cdot v_e = (d_a - d_1) \cdot v_e
\end{align*}
\]  

\[
\begin{align*}
    e_{13} &= \sum_{i=1}^{d_e} m_i \cdot v_{SM-2} = (m_e - m_3) \cdot v_e = (d_e - d_3) \cdot v_e
\end{align*}
\]  

The inserted voltage source \( e_{12} \) and \( e_{13} \) can be controlled by duty cycles of \( G_{ac} \) and \( G_{dc} \), i.e. \( d_1 \) and \( d_2 \).

In terms of the common capacitor in the DC CFC, it is charged/discharged under mode 2/3, which yields:

\[
\begin{align*}
    C_{dc} \frac{dv_e}{dt} &= i_{dc} = \sum_{i=1}^{d_a} m_i \cdot i_{SM-1} + \sum_{i=1}^{d_e} m_i \cdot i_{SM-2}
\end{align*}
\]  

i.e.

\[
\begin{align*}
    \frac{dv_e}{dt} &= \frac{(d_a - d_1)}{C_{dc}} \cdot i_{12} + \frac{(d_e - d_3)}{C_{dc}} \cdot i_{13}
\end{align*}
\]  

The fact that the DC CFC achieves DC network current flow control by means of currents exchanges via the energy hub (common capacitor) can be observed in (4). An equivalent circuit diagram of the DC CFC represented in the form of controlled current sources is illustrated in Fig. 4.
C. STEADY-STATE OPERATING POINTS

Since the main focus of this paper is parametric analysis and optimization of the two-line DC CFC, the dynamics of AC systems and converters at terminals are not considered. Their functions are regarded as equivalent DC voltage/current sources (\(T_1\) and \(T_2\) apply constant current control, while \(T_3\) applies constant DC voltage control).

The steady-state relationship between \(u\) and \(y\) is:

\[
\begin{align*}
\dot{x} &= A \cdot x + B \cdot u \\
y &= C \cdot x + D \cdot u
\end{align*}
\]

where \(x = [i_1, i_2, i_3, v_1, v_2, u_T]^T\) ;

\(u = [i_1, i_2, v_1, v_2, y_1, u_T]^T\).

The matrices \(A, B, C,\) and \(D\) are listed in Appendix A.

III. SMALL-SIGNAL MODEL AND STABILITY ANALYSIS

A. SMALL-SIGNAL MODEL

A small-signal model (9) is obtained by adding a small perturbation around the steady-state operating point.

\[
\begin{align*}
\dot{\Delta x} &= A \cdot \Delta x + B \cdot \Delta u \\
\Delta y &= C \cdot \Delta x + D \cdot \Delta u
\end{align*}
\]

where \(\Delta d_1\) and \(\Delta d_2\) are regarded as input variables with perturbations, i.e. \(\Delta u\) is separated into two parts, \(\Delta u_c\) and \(\Delta u_d\). The input variables, output variables and state variables in the small-signal model are as follows:

\[
\begin{align*}
\Delta u &= [\Delta d_1, \Delta d_2]^T \\
\Delta x &= [\Delta i_1, \Delta i_2, \Delta i_3, \Delta v_1, \Delta v_2, \Delta y_1]^T
\end{align*}
\]

The model can be written in the state-space form:

\[
\begin{align*}
\Delta x &= A \cdot \Delta x + B \cdot \Delta u_c + B_d \cdot \Delta u_d \\
\Delta y &= C \cdot \Delta x + D \cdot \Delta u_c + D_d \cdot \Delta u_d
\end{align*}
\]

There is one system eigenvalue located in the right-half s-plane, which indicates the system is unstable. Additional control is required to achieve the correction of the system stability.

C. STABILITY ANALYSIS

According to model (10), a block diagram of the open-loop control system is depicted in the blue area in Fig. 5.
The open-loop transfer function of the control system concerning the input variable of $\Delta u_c$ can be obtained.

$$\mathbf{g}_{c, op} = \begin{bmatrix} 
\mathbf{g}_{c, op_{11}} & \mathbf{g}_{c, op_{12}} \\
\mathbf{g}_{c, op_{21}} & \mathbf{g}_{c, op_{22}} 
\end{bmatrix} = \mathbf{A} \cdot \Delta \mathbf{u}_c$$ \hspace{1cm} (11)

The stability of a minimum phase system (MPS) can be evaluated by the analysis of its Bode diagram. According to the definition of an MPS [22-23], i.e., a minimum-phase system does not have poles or zeros in the right-half s-plane or on the jω-axis, excluding the origin, the poles and zeros of the open-loop transfer function of the two-line DC CFC are calculated to check whether the system is an MPS. The diagonal matrices, $\mathbf{g}_{c, op_{11}}$ and $\mathbf{g}_{c, op_{22}}$, are taken as the transfer function for the stability analysis of $i_{12}$ and $V_c$, respectively. The poles and zeros of the open-loop transfer function are calculated and presented in Table IV.

<p>| TABLE IV POLES AND ZEROS OF THE OPEN-LOOP TRANSFER FUNCTION OF $i_{12}$ AND $V_c$ WITHOUT/WITH ADDING MATRIX $\mathbf{E}$ |
|-----------------|-----------------|-----------------|
| Open-loop transfer function of $i_{12}$ without adding matrix $\mathbf{E}$ | Open-loop transfer function of $i_{12}$ with adding matrix $\mathbf{E}$ |</p>
<table>
<thead>
<tr>
<th>Poles</th>
<th>Zeros</th>
<th>Poles</th>
<th>Zeros</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-9 \pm j119$</td>
<td>$-10.42 \pm j137.55$</td>
<td>$-9 \pm j119$</td>
<td>$-10.42 \pm j137.55$</td>
</tr>
<tr>
<td>$-17 \pm j63$</td>
<td>$-20.00 \pm j54.16$</td>
<td>$-9 \pm j119$</td>
<td>$-20.00 \pm j54.16$</td>
</tr>
<tr>
<td>$-18 \pm j34$</td>
<td>$-81.61$</td>
<td>$-17 \pm j63$</td>
<td>$-50$</td>
</tr>
<tr>
<td>$-22 \pm j55$</td>
<td>$-18 \pm j34$</td>
<td>$-18 \pm j34$</td>
<td>$-81.61$</td>
</tr>
</tbody>
</table>

All the poles and zeros are located in the left-half s-plane or the origin. It indicates that the meshed HVDC grid under study is an MPS. Hence, the stability of the open-loop system can be evaluated according to the Bode diagram. The Bode diagrams of both diagonal matrices are presented in Fig. 6, where the black solid line shows the Bode diagram of $i_{12}$, the blue dashed line shows the Bode diagram of $V_c$:

![FIGURE 6. Bode diagram of $\mathbf{g}_{c, op_{11}}$ and $\mathbf{g}_{c, op_{22}}$ without Matrix $\mathbf{E}$](image)

In Fig. 6, the phase margin of $\mathbf{g}_{c, op_{11}}$ is close to 90 degrees, which indicates that the response of $i_{12}$ is stable. However, the phase margin of $\mathbf{g}_{c, op_{22}}$ is -90 degrees, which indicates that the response of $V_c$ is unstable, necessitating additional control strategies to correct the performance of $V_c$.

The stability can be improved by providing a phase shift on the associated element of the input $\Delta u_c$. In addition, to eliminate the steady-state error of both $i_{12}$ and $V_c$, a matrix $\mathbf{E}$ with PI controller is designed preliminary to the input $\Delta u_c$ as shown in the green area in Fig. 5. The expression of $\mathbf{E}$ is:

$$\mathbf{E} = \begin{bmatrix} 
E_{11} & E_{12} \\
E_{21} & E_{22} 
\end{bmatrix} = \begin{bmatrix} 
\frac{1}{P_{i,2of}} & 0 \\
0 & \frac{1}{P_{i,1of}} 
\end{bmatrix} \begin{bmatrix} 
K_{p1} \pm jK_{i1} \\
K_{p2} \pm jK_{i2} 
\end{bmatrix}$$ \hspace{1cm} (11)

where the diagonal matrix $E_{22}$ has a phase shift of -180° which is achieved by timing -1. In the open-loop system with matrix $\mathbf{E}$, the input variable is changed from $\Delta u_c$ to $\Delta \mathbf{e}_c$, where $\Delta \mathbf{e}_c$ is the error signal of the input references and measurements:

$$\Delta \mathbf{e}_c = \Delta \mathbf{y}_{ref} - \Delta \mathbf{y} = \begin{bmatrix} 
\Delta y_{ref,1} - \Delta y_{12} \\
\Delta y_{ref,2} - \Delta y_{22} 
\end{bmatrix}$$ \hspace{1cm} (12)

A unity feedback matrix $\mathbf{F}$ is used to form a close-loop control system as shown in Fig. 5. In the close-loop system, the input variable becomes $\Delta \mathbf{e}_c$. The addition of the control matrix $\mathbf{E}$ can significantly enhance the system stability. Fig. 7 illustrates the Bode diagram of $\mathbf{g}_{c, op_{11}}$ and $\mathbf{g}_{c, op_{22}}$ after adding control matrix $\mathbf{E}$.

![FIGURE 7. Bode diagram of $\mathbf{g}_{c, op_{11}}$ and $\mathbf{g}_{c, op_{22}}$ with Matrix $\mathbf{E}$](image)

In Fig. 7, the black solid line shows the gain margin and phase margin of $i_{12}$, while the blue dashed line shows the gain margin and phase margin of $V_c$. With matrix $\mathbf{E}$ in which the parameters of the PI controllers are $K_{p1} = K_{i1} = 1$, $K_{p2} = K_{i2} = 50$, the phase margin of $V_c$ is changed from -90° to 76.7° and both the gain margins and phase margins of $i_{12}$ and $V_c$ are now positive, which indicates the stability of the system. In addition, the gain margins of both $i_{12}$ and $V_c$ become infinite after adding matrix $\mathbf{E}$, which indicates that the gain margins of the system are sufficiently large and the changes of the phase margins may have more impact on the system stability and dynamic behaviors. Hence, in the following analysis, the impact of the system parameters on the phase margins is...
mainly investigated. From Table III, all the eigenvalues of the system under steady-state operating point locate on the left-half s-plane with adding matrix E. Since matrix E defines the dependency of $\Delta u_c$ on $\Delta E_c$, the parametric selection of matrix E is important and has great impact on the system stability and dynamic performance.

**IV. CONTROL SYSTEM PARAMETER OPTIMIZATION**

**A. OPTIMIZATION OF PROPORTIONAL GAINS**

A study on the impact of parametric selection of matrix E on the phase margin is conducted. In order to exploit the influence of each parameter, the control variate method and scanning method are deployed. Initially, the parameters of the integral gains $K_{i1}$ and $K_{i2}$ are fixed at 50, while the proportional gains $K_{p1}$ and $K_{p2}$ are gradually increased from 1 to 20 with an interval of 0.5. The tendency of changes of the phase margins and cut-off frequency can be scanned and observed. The changes of phase margins with the increase of the proportional gains are presented in Fig. 8. Table V presents several typical points of Fig. 8.

When $K_p$ is fixed at 50 while increasing $K_i$, the phase margins of both $t_{i2}$ and $v_c$ decrease. In addition, the phase margins decrease significantly at the initial stage and gradually slow down when $K_p$ is greater than 5. The cut-off frequencies almost increase linearly with the increase of $K_p$. Based on the typical selection principle of phase margins in practical engineering [22] and synthesizing the dynamic behavior of the phase margins and cut-off frequencies of both $t_{i2}$ and $v_c$, the principle of the selection of $K_p$ is made to keep the phase margins larger than $70^\circ$ while the cut-off frequency smaller than 500 rad/s. The eligible ranges of $K_{p1}$ and $K_{p2}$ are $[2, 5]$ and $[1, 2]$, respectively. $K_p$ is temporarily selected as 2 for subsequent analysis.

**B. OPTIMIZATION OF INTEGRAL GAINS**

Similarly, in order to identify the impact of the integral gains on the phase margins, the parameters of $K_{p1}$ and $K_{p2}$ are fixed at 2, while $K_{i1}$ and $K_{i2}$ are increased between ranges of 0 to 2000 with an interval of 50. The changes of phase margins with the increase of the integral gains are presented in Fig. 9. Table VI presents several typical points of Fig. 9.

When $K_i$ is fixed at 2 while increasing $K_p$, the phase margins of both $t_{i2}$ and $v_c$ decrease. In addition, the phase margins decrease significantly at the initial stage and gradually slow down when $K_i$ is greater than 500. The cut-off frequencies almost increase linearly with the increase of $K_i$, while the growing slope is mild. Similarly, the principle of the selection of $K_i$ is made to keep the phase margins larger than 70 while the cut-off frequencies smaller than 500 rad/s. The eligible ranges of $K_{i1}$ and $K_{i2}$ are $[0, 50]$ and $[0, 200]$, respectively. $K_i$ is selected as 50 for the following analysis.

**V. COMMON CAPACITOR AND VOLTAGE REFERENCE**

**A. PARAMETRIC ANALYSIS OF DC CFC**

For a two-line DC CFC, the control of DC power flow is achieved through energy exchange of adjacent DC lines. The energy exchange hub is the common capacitor which connects both full-bridges and can also be regarded as an
energy router. The stored energy $W_c$ of the common capacitor $C_{cfc}$ due to charging/discharging comply with the following mathematical relationships:

$$p_c = v_c \cdot i_c = C_{cfc} \cdot v_c \cdot \frac{dv_c}{dt}$$  \hspace{1cm} (13)

$$W_c = \int_0^t p_c \cdot dt = \int_0^t v_c \cdot i_c \cdot dt = \int_0^t v_c \cdot C_{cfc} \cdot dv_c$$  \hspace{1cm} (14)

where $p_c$ is the instantaneous charging/discharging power of the capacitor, $v_c$, $i_c$ is the voltage and current of the capacitor, $t$ is the time period. Regarding other energy storage components, particularly electrochemical energy storage devices, e.g., lead-acid batteries and lithium batteries cannot absorb/release instantaneous high currents, due to the limitations of electrochemical mechanisms [24, 25].

For capacitors, they can conduct fast charging/discharging operation. Moreover, they can conduct in-depth charging/discharging operation, i.e., significant change of voltages [26].

The change of stored energy of a capacitor, $\Delta W_c$, is determined by the difference of the squared capacitor voltage, that is:

$$\Delta W_c = W_{c2} - W_{c1} = \frac{C_{cfc}}{2} (v_{c2}^2 - v_{c1}^2)$$  \hspace{1cm} (15)

where $W_{c1}$ and $v_{c1}$ are the stored energy and voltage at a former stage, $W_{c2}$ and $v_{c2}$ are the stored energy and voltage at a later stage. In comparison with other energy storage devices, large power exchange could be achieved with a small capacitor, which meets the requirement of bulk-power transmission via DC lines. In addition, capacitors allow significant changes of voltages within a short period, i.e., high-speed charging/discharging performance or high frequency charging/discharging operation. Thus, it can implement fast distribution of energy among the DC lines.

The parametric selections of the capacitance and the capacitor voltage reference are of great importance to the performance of the two-line DC CFC.

- The capacitance indicates the energy storage capability of the common capacitor, as shown in (13). The energy storage capability may not be sufficient to achieve efficient energy exchange with too small capacitance. However, too large capacitance may result in unexpected large overshoots and increase in duration of DC voltages and currents to reach new steady states. In addition, the volume, size and cost of the capacitor will increase.

- Regarding the control reference setting of the common capacitor, it is also an important index for evaluating the energy storage capability of the capacitor, since the energy storage of the capacitor is directly proportional to its voltage square as shown in (13). When the two-line DC CFC is operated to control the DC line currents by means of energy exchange, one full-bridge DC-DC converter (SM-1) applies constant current control to regulate the line current, while the other full-bridge (SM-2) applies DC voltage control to stabilize the voltage of the common capacitor, i.e., SM-2 operates as a slack bus to stabilize the capacitor voltage while sending/receiving power as required. Hence, the stabilization control of the capacitor voltage and mitigation of the voltage fluctuations are essential for stable operation.

**B. SELECTION OF THE CAPACITANCE**

In order to analyze the impact of the capacitance on the phase margins, the control variate method and scanning method, are deployed. The parameters of $K_p$ and $K_i$ are fixed at 2 and 50, respectively, while $C_{cfc}$, the capacitance of the common capacitor, is increased between ranges of 10 $\mu$F to 10 mF with an interval of 20 $\mu$F. The changes of phase margins with the increase of $C_{cfc}$ are presented in Fig. 10. Table VII presents several typical points of Fig. 10.

When $K_p$ and $K_i$ are fixed while increasing $C_{cfc}$, the phase margin of $i_{12}$ increases while that of $v_c$ decreases. For the phase margin of $i_{12}$, it increases significantly at the initial stage and gradually slows down when $C_{cfc}$ is greater than 2 mF. For the phase margin of $v_c$, it decreases with a slope of 3.5 when $C_{cfc}$ increases from 10 $\mu$F to 3.4 mF and decreases significantly with a slope of 10.8 when $C_{cfc}$ increases from 3.4 mF to 4.4 mF, and gradually slows down when $C_{cfc}$ is greater than 4.4 mF. The cut-off frequencies both decrease with the increase of $C_{cfc}$. Since PM-1 is increasing while PM-2 is decreasing with the increase of $C_{cfc}$, the intersection point of both PMs can be evaluated if it is appropriate as the optimal $C_{cfc}$ with the same principle. The capacitance at the intersection point is 2.2 mF and the PMs are both 81º with the cut-off frequencies both at 229 rad/s, which satisfy the pre-defined principle. Thus, 2.2 mF capacitance is selected for the subsequent analysis.

**TABLE VII**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>$C_{cfc}$ (mF)</th>
<th>PM-1</th>
<th>PM-2</th>
<th>$\omega_1$ (rad/s)</th>
<th>$\omega_2$ (rad/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scheme 1</td>
<td>10</td>
<td>9.6º</td>
<td>1272</td>
<td>89.9º</td>
<td>48008</td>
</tr>
<tr>
<td>Scheme 2</td>
<td>50</td>
<td>21.5º</td>
<td>587</td>
<td>89.8º</td>
<td>9608</td>
</tr>
<tr>
<td>Scheme 3</td>
<td>100</td>
<td>30.3º</td>
<td>432</td>
<td>89.5º</td>
<td>48008</td>
</tr>
<tr>
<td>Scheme 4</td>
<td>200</td>
<td>42.1º</td>
<td>331</td>
<td>89.1º</td>
<td>2408</td>
</tr>
<tr>
<td>Scheme 5</td>
<td>1000</td>
<td>72.8º</td>
<td>239</td>
<td>85.6º</td>
<td>489</td>
</tr>
<tr>
<td>Scheme 6</td>
<td>2000</td>
<td>80.2º</td>
<td>230</td>
<td>81.7º</td>
<td>251</td>
</tr>
<tr>
<td>Scheme 7</td>
<td>5000</td>
<td>85.1º</td>
<td>226</td>
<td>61.4º</td>
<td>102</td>
</tr>
<tr>
<td>Scheme 8</td>
<td>10000</td>
<td>86.7º</td>
<td>225</td>
<td>59.3º</td>
<td>67</td>
</tr>
</tbody>
</table>

**FIGURE 10.** Performance of phase margins with the increase of $C_{cfc}$.
C. CAPACITOR VOLTAGE REFERENCE

The impact of the voltage reference settings of the common capacitor on the phase margins is analyzed. Similarly, the parameters of $K_p$ and $K_i$ are fixed at 2 and 50, respectively, and the common capacitance is fixed at 2.2 mF, while the voltage reference $V_{ref}$ of the common capacitor is increased between ranges of 0.5 kV to 20 kV with an interval of 0.5 kV. The changes of phase margins with the increase of $V_{ref}$ are presented in Fig. 11. Table VIII presents several typical points of Fig. 11.

![FIGURE 11. Performance of phase margins with the increase of $V_{ref}$](Image)

**TABLE VIII**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>$V_{ref}$ (kV)</th>
<th>$K_p$</th>
<th>$K_i$</th>
<th>$\omega_0$ (rad s$^{-1}$)</th>
<th>$\omega_0$ (rad s$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scheme 1</td>
<td>0.5</td>
<td>12.4</td>
<td>474</td>
<td>89.0º</td>
<td>2255</td>
</tr>
<tr>
<td>Scheme 2</td>
<td>1.0</td>
<td>20.6º</td>
<td>276</td>
<td>88.3º</td>
<td>1128</td>
</tr>
<tr>
<td>Scheme 3</td>
<td>5.0</td>
<td>81.0º</td>
<td>229</td>
<td>81.0º</td>
<td>229</td>
</tr>
<tr>
<td>Scheme 4</td>
<td>10.0</td>
<td>87.4º</td>
<td>384</td>
<td>59.9º</td>
<td>106</td>
</tr>
<tr>
<td>Scheme 5</td>
<td>15.0</td>
<td>88.6º</td>
<td>554</td>
<td>58.9º</td>
<td>86</td>
</tr>
<tr>
<td>Scheme 6</td>
<td>20.0</td>
<td>89.0º</td>
<td>728</td>
<td>57.4º</td>
<td>72</td>
</tr>
</tbody>
</table>

Fig. 11 shows that the phase margin of $i_{12}$ increases while the phase margin of $v_i$ decreases, the varying pattern of which is similar to that in Fig. 10. For the phase margin of $i_{12}$, it increases significantly at the initial stage and gradually slows down when $V_{ref}$ is greater than 5 kV. For the phase margin of $v_i$, it decreases with a slope of 1.71 when $V_{ref}$ increases from 0.5 kV to 8.5 kV and decreases significantly with a slope of 24.5 when $V_{ref}$ increases from 8 kV to 8.5 kV, and gradually slows down when $V_{ref}$ is greater than 9 kV. The cut-off frequency of PM-1 decreases initially to a minimum of 186 rad/s ($V_{ref} = 2.5$ kV) and increases afterwards, while the cut-off frequency of PM-2 decreases with the increase of $V_{ref}$. Since PM-1 increases while PM-2 decrease with the increase of $V_{ref}$, the intersection point of both PMs can be taken as the optimal $V_{ref}$. The $V_{ref}$ at the intersection point is 5.0 kV and the PMs are both 81.0º with the cut-off frequencies at 229 rad/s. Thus, the selected $V_{ref}$ also keeps the preset principle.

VI. SIMULATION SYSTEM AND RESULTS

In order to evaluate the effectiveness of the proposed optimal parametric selection scheme, a three-terminal HVDC system with the integration of a two-line DC CFC on DC Line 12 and Line 13 is established on the time-domain simulation environment PSCAD/EMTDC. The detailed system parameters were provided in Table II. The control strategies of the HVDC converter stations and the DC CFC were described in Section II-C.

Nine case will be studied with three types of incidents, i.e. step changes of $i_{12ref}$, disturbances at $T_1$, and disturbances on Line 13. In each incident, three different parametric selections will be evaluated, i.e. $PI$ parameters, capacitance of the common capacitor, and voltage reference of the common capacitor. The arrangement of the 9 cases are listed in Table IX.

**TABLE IX**

<table>
<thead>
<tr>
<th>Incidents</th>
<th>Different $K_p$ Parameters</th>
<th>Different Capacitances</th>
<th>Different Voltage Refs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step changes of $i_{12ref}$</td>
<td>Case A1</td>
<td>Case B1</td>
<td>Case C1</td>
</tr>
<tr>
<td>Disturbances at $T_1$</td>
<td>Case A2</td>
<td>Case B2</td>
<td>Case C2</td>
</tr>
<tr>
<td>Disturbances on Line 13</td>
<td>Case A3</td>
<td>Case B3</td>
<td>Case C3</td>
</tr>
</tbody>
</table>

A. PARAMETRIC SELECTIONS OF PI CONTROLLERS

In this section, three cases are conducted to investigate the system response of the three types of incidents with different parametric selections of $PI$ controllers.

1) STEP CHANGES OF $i_{12REF}$

In this case, the system response under a step change of $i_{12}$ is simulated with different parametric selections of the proportional gains $K_p$ and integral gains $K_i$. Initially, the DC CFC is in bypass mode. According to the control reference settings of the converters at each terminal and the DC line parameters in Table II, the initial value of $i_{12}$ can be calculated at 1.25 kA. The DC CFC is activated at 0.5 s with $i_{12ref}$ at 0.8 kA and $V_{ref}$ at 5 kV. At 1.5 s, $i_{12ref}$ is stepped up to 1 kA and resumes 0.8 kA at 2.5 s. Simulation results with different $K_p$ and $K_i$ are presented in Fig. 12 and Fig. 13.

When the DC CFC is bypassed, no current flows into the common capacitor, thereby resulting zero $v_i$ before 0.5 s as shown in Fig. 13. The DC currents are naturally distributed according to the line resistance. Fig. 12 shows that $i_{12}$ is 1.25 kA before 0.5 s, which is consistent with theoretical analysis. At 0.5 s, the DC CFC is activated. When $K_p$ is 0.2 and $K_i$ is 50, both $i_{12}$ and $v_i$ cannot reach the new steady state within 0.5 s. The oscillations are significant with overshoots of 35% in $i_{12}$ and 108% in $v_i$. When $K_p$ is 2 and $K_i$ is 500, $i_{12}$ can be stabilized within 0.3 s with an overshoot of 25% and $v_i$ can reach the new steady state within 0.2 s with an overshoot of 80%. Both $i_{12}$ and $v_i$ can be controlled with stepping up/down control. When $K_p$ is 2 and $K_i$ is 5, the overshoots during transients become smaller. However, it takes over 1 s for $i_{12}$ to reach a new steady state, while $v_i$ can reach a new steady state within 0.6 s. When $K_p$ is 2 and $K_i$ is 50, both $i_{12}$ and $v_i$ can be stabilized within 0.2 s with overshoots of 5% in $i_{12}$ and 32% in $v_i$. When $K_p$ is 20 and $K_i$ is 50, both $i_{12}$ and $v_i$...
can be stabilized within 0.1 s with overshoots of 1% in $i_{12}$ and 20% in $v_c$.

Hence, the simulation results shown in Fig. 12 and Fig. 13 indicate the effectiveness of the proposed optimized parameters ($K_p = 2$, $K_i = 50$) and demonstrate that the dynamic behaviors can be further improved with the increase of $K_p$. This is because with the increase of $K_p$, the cut-off frequency will increase and exceed the preset value of 500 rad/s. It will indeed enhance the dynamic response, while it does increase the cost and difficulty of the control system design. Therefore, it is appropriate to choose the optimized parameters of $K_p$ at 2 and $K_i$ at 50. Under the conditions of cost permitting and no technical barrier, the gain $K_p$ can be further increased to make the system response even faster.

This is because small $K_i$ will lead to small cut-off frequency, the value of which determines the response speed of the control system. The rest two parametric sets have better performance in both steady state and anti-interference performance where the set of $K_p$ at 20 and $K_i$ at 50 has the optimal performance with minimum overshoot, least period of reaching the new steady state and strongest capability of anti-interference. Thus, the simulation results justify the correctness of the theoretical analysis.

2) DISTURBANCES AT $T_1$

In this case, the system response under disturbances at $T_1$ is simulated with different parametric selections of $K_p$ and $K_i$. At 0.5 s, DC CFC is activated from bypassing mode with $i_{12ref}$ at 1 kA and $v_{cref}$ at 5 kV. At 1.5 s, a disturbance signal composed of a sinusoidal magnitude of 0.7 kA and frequency of 2 Hz is added on the DC current source $i_1$ for 1 s. The simulation results are shown in Fig. 14 and Fig. 15.

The set of $K_p$ at 2 and $K_i$ at 500 presents least anti-interference capability. This is because the phase margins of $i_{12}$ and $v_c$ will continually decrease with the increase of integral gain $K_i$. The second least anti-interference capability lays on the set of $K_p$ at 0.2 and $K_i$ at 50, since the phase margins of $i_{12}$ and $v_c$ are reduced with smaller $K_p$, which is consistent with previous analysis. The set of $K_p$ at 2 and $K_i$ at 5 presents strong anti-interference capability with small oscillations during the disturbance, while the slow response from one state to a new steady state is its main drawback.

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B. PARAMETRIC SELECTIONS OF Ccfc

1) STEP CHANGES OF I12REF

In this case, the system response under step changes of $I_{12ref}$ is simulated with different parameters of $C_{cfc}$. The initial condition and the incident are the same as those in Case A1. The simulation results are shown in Fig. 18 and Fig. 19.

When $C_{cfc}$ is 100 mF, $I_{12}$ and $v_c$ cannot be stabilized. It is because with the increased $C_{cfc}$, the cut-off frequency of $v_c$ reduces significantly, leading to tardy response of $v_c$ and $I_{12}$. When $C_{cfc}$ is 0.01 mF, $I_{12}$ can be rapidly stabilized, while $v_c$ persists significant oscillations. When the other three $C_{cfc}$ values are applied, $I_{12}$ and $v_c$ can be well stabilized. The $C_{cfc}$ at 2.2 mF presents optimal control performance with smallest overshoot and least period of reaching new steady states.

2) DISTURBANCES AT $T_1$

In this case, the system response under disturbances at $T_1$ is simulated with different $C_{cfc}$. The initial condition and the incident are the same as those in Case B1. The simulation results are shown in Fig. 20 and Fig. 21.

Two values, 100/0.01 mF, are not considered, since the system cannot be stabilized. The performance is similar using the other three sets. When the disturbance occurs from 1.5 s to 2.5 s, both $I_{12}$ and $v_c$ can be well stabilized.

3) DISTURBANCES ON LINE 13

In this case, the system response under disturbances on Line 13 is simulated with different $C_{cfc}$. The initial condition and the incident are the same as those in Case C1. The simulation results are shown in Fig. 22 and Fig. 23.
When the $C_{fc}$ values 1 mF, 2.2 mF and 3.6 mF are used, both $i_{12}$ and $v_c$ can be well stabilized when the disturbance occurs from 1.5 s to 2 s. The anti-interference capability using three parameters is similar.

C. DIFFERENT $V_{cref}$ OF THE COMMON CAPACITOR

1) STEP CHANGES OF $i_{12}$ref

In this case, the system response under step changes of $i_{12}$ref is simulated with different $V_{cref}$. The initial condition and the incident are the same as those in Case A1. The simulation results are shown in Fig. 24 and Fig. 25.

Considering the settings of $V_{cref}$ at 2 kV and 3.5 kV, $i_{12}$ cannot be controlled to 0.8 kA after activating the DC CFC at 0.5 s. This is because the energy stored in the common capacitor is relative to its voltage square according to (13). When $V_{cref}$ is selected excessively small, it will directly lead to the reduction of the energy storage in the capacitor, thereby reducing the instantaneous absorbed/ released power. The rest three parametric sets can all achieve smooth control of $i_{12}$. The set of $V_{cref}$ at 5 kV presents the optimal control performance with smallest overshoot during the transition from one steady state to a new one. For the set of $V_{cref}$ at 50 kV, since the initial value of $v_c$ is zero when the DC CFC is bypassed, it needs a certain period to rise to 50 kV. This time-consuming transition results in delayed response of $i_{12}$ and significant overshoot at the first stepping up control. In addition, obvious current oscillations can be seen when $i_{12}$ reaches new steady states. Hence, the simulation results justify the effectiveness of the optimal $V_{cref}$ proposed.

2) DISTURBANCES AT $T_1$

In this case, the system response under disturbances at $T_1$ is simulated with different $V_{cref}$. The initial condition and the incident are the same as those in Case B1. The simulation results are shown in Fig. 26 and Fig. 27.

When $V_{cref}$ is 2 kV, significant oscillations can be observed when the disturbances occur. It can be seen that with the increase of $V_{cref}$, the impact out of the disturbance on both $i_{12}$ and $v_c$ becomes less significant. Synthesizing the simulation results in Case C1 and Case C2, it can be concluded that with the increase of the capacitor voltage reference, the anti-interference capability is enhanced while the steady state performance is degraded. The simulation results verify the proposed optimal parametric selection of $V_{cref}$ at 5 kV.

3) DISTURBANCES ON LINE 13

In this case, the system response under disturbances on Line 13 is simulated with different $V_{cref}$. The initial condition and the incident are the same as those in Case C1. The simulation results are shown in Fig. 28 and Fig. 29.
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FIGURE 29. $v_c$ with different $V_{	ext{ref}}$ under disturbances on Line 13

For the sets of $V_{	ext{ref}}$ at 2 kV and 3.5 kV, $i_{12}$ cannot remain the reference settings after the disturbance. With the increase of $V_{	ext{ref}}$, both $i_{12}$ and $v_c$ can be well stabilized. Therefore, synthesizing the dynamic performance of Case C1, C2 and C3, the proposal of $V_{	ext{ref}}$ at 5 kV is valid.

VII. ANALYSIS AND DISCUSSIONS

Due to the fact that the gain margins of both $i_{12}$ and $v_c$ are infinite after adding matrix $E$, the parametric impact on the system stability and dynamic behaviors is mainly analyzed on the phase margins. However, it is essential to justify the condition of the gain margin with the proposed optimal parameters, since the stability of a system is fully determined by both the phase margin and gain margin. The bode diagram of the system with optimal parameters is depicted in Fig. 30.

FIGURE 30. Bode diagram of $gc_{op1}$ and $gc_{op2}$ with optimal parameters

With the proposed optimal parameters, the infinite gain margins are maintained and the phase margins are both around 81°, which is consistent with the theoretical analysis in Section V. Hence, it is justified based on the theoretical analysis and simulation results that the principle of parametric selections and optimizations enlarges both phase margins and cut-off frequencies of $i_{12}$ and $v_c$. The increase of phase margins will enhance the stability margins of the system, while the increase of cut-off frequencies will expedite the system response. Regarding the parametric selections of three types of variables, i.e. proportional and integral gains, capacitance, and capacitance voltage reference, the increase of the proportional gains will enhance both phase margins and cut-off frequencies of $i_{12}$ and $v_c$. Hence, under the permission of technical level and cost, $K_p$ can be set up as large as possible. The increase of integral gains will reduce the phase margins of $i_{12}$ and $v_c$ while increase their cut-off frequencies, resulting in enhancing the system response speed while sacrificing the system stability margin and anti-interference capability. Hence, the selection of $K_i$ should be moderate, i.e. neither too large nor too small. The increase of the common capacitance will lead to increase of the phase margin of $i_{12}$. However, it will decrease the phase margin of $v_c$ and the cut-off frequency of both $i_{12}$ and $v_c$. That means the changes of the capacitance will have direct impact on the response speed. Hence, the selection of $C_{	ext{cfc}}$ should also be moderate. The increase of $V_{	ext{ref}}$ will optimize the performance of $i_{12}$, i.e. enhance both the phase margin and cut-off frequency of $i_{12}$, which increases its stability margin and response speed. However, it will deteriorate the behavior of $v_c$, i.e. decrease its phase margin and cut-off frequency, which narrows the stability margin and reduce the response speed. Hence, the selection of $V_{	ext{ref}}$ should be moderate. In addition, the selection of $V_{	ext{ref}}$ has direct impact on the voltage level in operating the DC CFC and the requirement on the insulation level. The simulation results indicate that the parametric selection of $V_{	ext{ref}}$ at 5 kV can achieve optimal dynamic behaviors in both steady state and transients. This voltage level is only less than 2% of that of the typical HVDC transmission grid. The design of the DC CFC has the merit of modular structure and the flexible technique of energy exchange applied for the control of DC line currents in the meshed grid, which realize the features of lower cost and easier implementation for practical engineering.

VIII. CONCLUSIONS

In this paper, regarding a two-line DC CFC integrated three-terminal HVDC grid, a small-signal model has been established for stability analysis in the frequency domain. The impact of the proportional gains and integral gains on the phase margins has been quantitatively analyzed with the deployment of control variate and scanning approaches. An optimal parametric selection of $K_p$ and $K_i$ has been proposed. In addition, the impact of the capacitance and voltage reference of the common capacitor on the phase margins and dynamic behaviors has been analyzed. A principle of the parametric selection ranges regarding the capacitance and voltage reference has been proposed with a set of optimal parameters. Finally, the theoretical analysis and optimized parameters have been evaluated on the PSCAD/EMTDC. The simulation results have justified the effectiveness of the proposed method. The principle of the parametric selection ranges and optimal parametric selection method proposed can be applied for multi-line DC CFCs (see Appendix B).

APPENDIX A

The expressions of $A$, $B$, $C$, $D$, and $A_2$, $B_5$, $B_6$, $C_2$, $D_5$, $D_6$ are as follows.
DC lines, the rectifier adopts constant current control, while the constant voltage control or the minimal extinction angle control is employed by the inverter. The same is true for the VSC-based DC lines, where the DC current is controlled by the rectifier and the DC voltage is usually maintained by the inverter. Hence, it is reasonable to adopt constant current source or constant voltage source as the DC equivalence of converter, the type of which does not matter, when the converters at terminals respond rapidly. On the other hand, for an AC/DC power system, the task of power flow control can be divided into two levels. At the system level, the AC power flow is optimized and the real power desired to be transmitted by DC lines/networks is determined. Then at the second level, power flow distribution among the DC lines is considered. This paper investigates the method to implement the second level power flow control, i.e. DC current/power flow control. At the present stage, it is necessary to simplify the AC system and the terminals to reduce the complexity in DC current flow control study.

The approach proposed in this paper can be applied for MTDC grids with different types of converters at the terminals, e.g. $T_1$ can be a rectifier of an LCC terminal, while $T_2$, $T_3$ and $T_4$ are VSC terminals. As a demonstration, the impact of the PI parameters on the margins of the system undergoing a current step change will be investigated.

The mathematical model and the small-signal model are obtained by the same approach described in Section II and III. In order to achieve full controllability of branch currents in the four-terminal DC grid, the three-line DC CFC has to regulate two out of three DC branch currents, i.e. two of $i_{13}$, $i_{12}$, $i_{14}$. In the following analysis, the three-line DC CFC is used to regulate $i_{12}$ and $i_{13}$, and to control the voltage of the common capacitor. The four-terminal system with the DC CFC is verified as an MPS. The system parameters are shown in Table X. The values of $d_{13}$, $d_{12}$ and $d_{14}$ can be obtained ($d_{13} = 0.34$, $d_{12} = 0.66$, $d_{14} = 0.50$) using the similar approach as (7) and (8).

**APPENDIX B**

In order to verify the proposed parametric optimization scheme in more complex DC grids, a three-line DC CFC equipped four-terminal meshed HVDC grid, as illustrated in Fig. 31, is analyzed.

In the four-terminal system, $T_4$ applies DC voltage control to maintain the DC voltage of the MTDC grid, while the other three terminals apply constant DC current control to import/export active power to/from the DC grid. The dynamics of the converters and the AC sides are not considered. It implies that prompt response is assumed for both LCCs and VSCs, and they can maintain ideal states at the DC sides. For the normal operation mode of LCC-based

![Image](https://example.com/image.png)

**FIGURE 31. A four-terminal meshed HVDC with a three-line DC CFC**

In the four-terminal system, $T_4$ applies DC voltage control to maintain the DC voltage of the MTDC grid, while the other three terminals apply constant DC current control to import/export active power to/from the DC grid. The dynamics of the converters and the AC sides are not considered. It implies that prompt response is assumed for both LCCs and VSCs, and they can maintain ideal states at the DC sides. For the normal operation mode of LCC-based

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>MTDC grid voltage</td>
<td>320 kV</td>
</tr>
<tr>
<td>$R_{13, 12}$ of Branch 12</td>
<td>1 Ω, 30 mH</td>
</tr>
<tr>
<td>$R_{13, 13}$ of Branch 13</td>
<td>3 Ω, 90 mH</td>
</tr>
<tr>
<td>$R_{14, 14}$ of Branch 14</td>
<td>2 Ω, 60 mH</td>
</tr>
<tr>
<td>$R_{14, 14}$ of Branch 24</td>
<td>2 Ω, 60 mH</td>
</tr>
<tr>
<td>$R_{13, 14}$ of Branch 34</td>
<td>1 Ω, 30 mH</td>
</tr>
<tr>
<td>Terminal capacitors $C_{1s}$, $C_{2s}$, $C_{3s}$</td>
<td>100 μF</td>
</tr>
<tr>
<td>Common capacitor $C_{dc}$</td>
<td>1000 μF</td>
</tr>
<tr>
<td>DC current reference at $T_1$ ($i_{1dc}$)</td>
<td>5 kA</td>
</tr>
<tr>
<td>DC current reference at $T_2$ ($i_{2dc}$)</td>
<td>1 kA</td>
</tr>
<tr>
<td>DC voltage reference at $T_1$ ($v_{1ref}$)</td>
<td>2 kA</td>
</tr>
<tr>
<td>DC voltage reference at $T_2$ ($v_{2ref}$)</td>
<td>320 kV</td>
</tr>
<tr>
<td>Current reference of Branch 12 ($i_{12dc}$)</td>
<td>1.6 kA</td>
</tr>
<tr>
<td>Current reference of Branch 13 ($i_{13dc}$)</td>
<td>1.6 kA</td>
</tr>
<tr>
<td>Voltage reference of $C_{dc}$ ($v_{ref}$)</td>
<td>5 kV</td>
</tr>
</tbody>
</table>
The Bode diagrams of $i_{t2}, i_{t3}$ and $v_i$ without/with matrix $E$, in which the parameters of the PI controllers are $K_{p1} = K_{p2} = K_{p3} = 1$, $K_{i1} = K_{i2} = K_{i3} = 50$, are illustrated in Fig. 32 and Fig. 33, respectively.

Gain Margin of $i_{t2}$ (without $E$) = Inf deg;  
Gain Margin of $i_{t2}$ (with $E$) = 120.6931 deg;  
Gain Margin of $v_i$ (without $E$) = -101.8655 deg;  
Gain Margin of $v_i$ (with $E$) = 82.5543 deg.

Phase Margin of $i_{t2}$ (without $E$) = 79.9939 deg;  
Phase Margin of $i_{t2}$ (with $E$) = 180 deg;  
Phase Margin of $v_i$ (without $E$) = -90 deg;  
Phase Margin of $v_i$ (with $E$) = 0 deg.

**FIGURE 32. Bode diagrams of $i_{t2}, i_{t3}, v_i$ without Matrix $E$**

<table>
<thead>
<tr>
<th>Frequency (rad/s)</th>
<th>Magnitude (dB)</th>
<th>Phase (deg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.02</td>
<td>0.02</td>
<td>0.02</td>
</tr>
<tr>
<td>0.04</td>
<td>0.04</td>
<td>0.04</td>
</tr>
<tr>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
</tr>
<tr>
<td>0.08</td>
<td>0.08</td>
<td>0.08</td>
</tr>
<tr>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
</tr>
<tr>
<td>0.12</td>
<td>0.12</td>
<td>0.12</td>
</tr>
<tr>
<td>0.14</td>
<td>0.14</td>
<td>0.14</td>
</tr>
<tr>
<td>0.16</td>
<td>0.16</td>
<td>0.16</td>
</tr>
<tr>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>0.20</td>
<td>0.20</td>
<td>0.20</td>
</tr>
</tbody>
</table>

**FIGURE 33. Bode diagrams of $i_{t2}, i_{t3}, v_i$ with Matrix $E$**

In Fig. 32, the gain margins of $i_{t3}$ and $v_i$ are both negative and the phase margin of $v_i$ is negative, indicating that the response of $i_{t3}$ and $v_i$ is unstable. With the addition of matrix $E$ with PI controllers, the gain margins and phase margins of $i_{t2}, i_{t3}$ and $v_i$ present positive margins as shown in Fig. 33, which indicates the stability of the system. In addition, the gain margins of $i_{t2}, i_{t3}$ and $v_i$ are also infinite after adding matrix $E$, which indicates that the phase margins may have more impact on the system stability and dynamic behaviors.

Hence, the impact of the PI parameters on the phase margins is mainly investigated. Similarly, via the control variate method and scanning method, initially the parameters of the integral gains $K_{i1}, K_{i2}$ and $K_{i3}$ are fixed at 50, while the proportional gains $K_{p1}, K_{p2}$ and $K_{p3}$ are gradually increased between ranges of 1 to 20 with an interval of 0.5. The changes of phase margins with the increase of the proportional gains are presented in Fig. 34.

**FIGURE 34. Phase margins with the increase of proportional gains**

When $K_{p1}$ is fixed at 50 while increasing $K_{p2}$, the phase margins of both $i_{t2}$ and $v_i$ increase, while the phase margin of $i_{t3}$ increases at the initial stage and decreases when $K_{p2}$ is greater than 2. Regarding the proposed parametric selection principle, the eligible ranges of $K_{p1}, K_{p2}$ and $K_{p3}$ are [4.5, 20], [1, 20] and [0, 20], respectively. Synthesizing the dynamic behaviors of the phase margins of $i_{t2}, i_{t3}$ and $v_i$, it is appropriate to select $K_{p1}$ as 15, since the phase margins are over 80º and their dynamics tend to be stable.

In order to identify the impact of the integral gains on the phase margins, the parameters of $K_{p1}, K_{p2}$ and $K_{p3}$ are fixed at 15, while $K_{i1}, K_{i2}$ and $K_{i3}$ are increased between ranges of 0 to 2000 with an interval of 50. The changes of phase margins with the increase of the integral gains are presented in Fig. 35.

**FIGURE 35. Phase margins with the increase of integral gains**

When $K_{p2}$ is fixed at 15 while increasing $K_{p3}$, the phase margins of $i_{t2}, i_{t3}$ and $v_i$ decrease. Regarding the principle of parametric selection proposed, the eligible ranges of $K_{i1}, K_{i2}$ and $K_{i3}$ are [0, 1050], [0, 2000] and [0, 2000], respectively. Considering the fact that the integral gains are inversely...
proportional to the integral time constant and have influence on mitigating the steady-state error, the system response may be very slow and steady-state errors may emerge if the integral gains are selected too small. Synthesizing the dynamic behaviors of the phase margins of $i_{12}$, $i_1$ and $v_1$, and the character of the integral gains, it is appropriate to select $K_i$ as 500, since the phase margins are over 70° and $K_i$ is sufficiently large to provide rapid system response and eliminate the steady-state error.

The system response under step changes of $i_{12ref}$ is simulated, which is similar to that of Case A1 in Section VI. Initially, the DC CFC is in bypass mode. The initial value of $i_{12}$ can be calculated at 1.85 kA. The DC CFC is activated at 0.5 s with $i_{12ref}$ and $i_{12ref}$ both at 1.6 kA and $v_{1ref}$ at 5 kV. At 1.5 s, $i_{12ref}$ is stepped down to 1.2 kA and resumes 1.6 kA at 2.5 s. Simulation results with different parameters of $K_p$ and $K_i$ are presented in Fig. 36 and Fig. 37.

When the DC CFC is in bypass mode, no current flows through the common capacitor, thereby resulting $v_1$ at zero before 0.5 s as shown in Fig. 37. The DC currents are naturally distributed. Fig. 36 shows that $i_{12}$ is 1.85 kA before 0.5 s, which is consistent with theoretical analysis. At 0.5 s, the DC CFC is activated. When $K_p$ is 0.015 and $K_i$ is 50, both $i_{12}$ and $v_1$ have significant oscillations indicating instability of the system, which is consistent with the theoretical analysis of the Bode diagram in Fig. 34. When $K_p$ is 15 and $K_i$ is 50, $i_{12}$ can be stabilized within 0.8 s. Both $i_{12}$ and $v_1$ can be controlled with stepping up/down control. When $K_p$ is 15 and $K_i$ is 500, both $i_{12}$ and $v_1$ can be stabilized within 0.1 s without overshoot, which demonstrates desired performance with the proposed optimized parameters. When $K_p$ is 15 and $K_i$ is 5, although the dynamic behaviors of both $i_{12}$ and $v_1$ are stable, $i_{12}$ cannot reach the steady state within 1 s. This is because the integral gain is selected too small resulting in slow system response. When $K_p$ is 15 and $K_i$ is 500, obvious overshoots can be observed in both $i_{12}$ and $v_1$, since a large integral gain can enhance the system response while may lead to the significant overshoot.

The simulation results shown in Fig. 36 and Fig. 37 verify the effectiveness of the proposed optimized parameters ($K_p = 15$, $K_i = 500$). In addition, the validity of the proposed analytical approach for a multi-line DC CFC in the MTDC grid is also justified. It is identified that the parametric selection of a multi-line DC CFC has more coupling effect on the system dynamic behaviors due to more interactions and energy exchanges within the common capacitor. Therefore, the robustness, reliability and advanced controller design for multi-line DC CFCs deserve further research.

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