Investigation into the nonlinear characteristics of a high-speed drive circuit for a proportional solenoid controlled by a PWM signal

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This work was supported by the NSFC-Zhejiang Joint Fund for the Integration of Industrialization and Informatization under Grant U1509204, and the National Natural Science Foundation of China under Grant 51475462 and Grant 91748210.

ABSTRACT This paper analyzes the unique nonlinear characteristics of a high-speed drive circuit for proportional solenoid, i.e., the inverse discharging drive circuit (IDDC), which has a faster discharging speed than a traditional drive circuit. The experimental results clearly show the piecewise nonlinear relationship between the current and the pulse-width modulation (PWM) duty ratio of the control signal of the IDDC. The mathematical model of the IDDC working processes in one PWM period is constructed in detail to analyze the IDDC nonlinear characteristics. The computational equations of the significant nonlinear features including the critical PWM duty ratio, the steady-state current, the amplitude of the current oscillation, and the response time of the circuit are deduced through algebraic analyses, which are verified by a comparison between the experimental and calculated results. These analyses aid the design and control of a solenoid drive circuit for a hydraulic proportional valve. Finally, a modified PI controller that considers the nonlinear characteristics of the IDDC is designed, and the experimental results show that the designed controller significantly improves the response speed of the solenoid current.

INDEX TERMS Solenoid, pulse width modulation, nonlinearity, drive circuit.

I. INTRODUCTION

Hydraulic proportional valves are widely used in electro-hydraulic systems involving high-precision proportional control systems [1]. A proportional solenoid is the most important electro-mechanical converter for hydraulic proportional valves, which uses a PWM signal drive circuit that controls the solenoid current. Two different drive circuits are widely used. One is the classical direct discharging drive circuit (DDDC), and the other one is the inverse discharging drive circuit (IDDC), as shown in Fig. 1, where the solenoid is simplified as the equivalent resistor $R_L$ and an inductance $L$ in series. In the DDDC, the flywheel diode $D_2$ for current discharging is directly connected to the solenoid in parallel. In IDDC, the flywheel diodes $D_2$ and $D_4$ for current discharging are connected with the power terminal. The special structure of the IDDC renders the current discharging speed much faster, which results in a higher response speed of the valve spool and improves the performance of the valve [2] [3].

FIGURE 1. Schematics of the drive circuits. (a) the direct discharging drive circuit (DDDC); and (b) the inverse discharging drive circuit (IDDC).

The studies to improve the proportional valves control performance have always been based on establishing the mathematical model of the valve. The valve model contains an electromagnetic model of the solenoid, the fluid-
dynamic model and the mechanical model [4]-[9]. In these models, scholars consider the hysteresis of the solenoid and the inductance, which changes with displacement and current [10] [11] and the dead zone of the valve spool [12] [13] [14]. These studies seldom mention the drive circuit of the valve because they assume that the drive circuit dynamics are much faster than the dynamics of the overall valve. However, this circuit should not be ignored for improving the response speed of valve, especially high speed valves. In addition, this paper focuses on the detailed modeling and analyses of the IDDC, and its effect on the control performance of the proportional solenoid. The studies to improve solenoid control performance can be divided into two parts.

The first part focuses on the control method of the solenoid. K.W. Lim et al. used a dual rate cascade control method to convert a switching solenoid into a proportional actuator [15]. G. Liu et al. [16] and B.J. Kang et al. [17] optimized the parameters of the PWM signal for solenoid control. R. Amirante et al. [18] combined the different forms of a drive signal for energy saving. E. E. Topcu et al. [19] employed the switching input and holding input methods for a quick response and energy saving. W. Shen et al. [20] employed a compensation network to adjust the amplitude of the current chatter of the driving circuit. Q. Xu et al. [21] pointed out that the control of the dither current can efficiently reduce the hysteresis effect of the solenoid valve. In these studies, the solenoids are driven by the DDDC whose current characteristics are proportional to the PWM duty ratio.

The second part focuses on the drive circuits of the solenoid. These drive circuits can be divided into three categories. The first category applies an inverse voltage to improve the discharging speed of the solenoid when power is removed. This kind of drive circuit includes the IDDC whose inverse voltage is introduced by a combination of diodes and capacitors, and the drive circuits that apply a Zener diode to introduce an inverse voltage [22]-[24].

The second category applies multiple supply powers to guarantee an enhanced response time and low power consumption. This kind of circuit initially supplies a higher actuation voltage for a brief period of time to improve the response speed and then switches to a lower voltage to maintain the solenoid in an energized state for an extended time to decrease the power consumption [23]-[25].

The third category applies special circuit designs to improve the response time or increase the power consumption. T. Kajima et al. [26] focused on the electrical circuits for the purpose of energizing the solenoid valve, and developed a pre-energize method, which was highly effective in speeding up the operation of the solenoid valves. Y. Fuhao et al. [27] presented a bi-state modulation method and a half-bridge power drive circuit for a high-speed on/off solenoid valve, which improved the current step response. X. Kong et al. [28] used parallel coils to energize the solenoid valve, which provided enough force and decreased the switching time of the valve. M.-S. Kim et al. [29] designed a power saving circuit with a combination of an additional resistor and a triode, which greatly improved the efficiency by providing an optimal current according to mechanical load. C. Sheng-Nian et al. [30] used a soft-switching drive circuit in a high speed solenoid valve, which greatly reduced switching device losses and switching noise.

These drive circuit studies have focused on the on/off characteristics of the circuits but hardly involve the analyses of the proportional control performance of the drive circuit controlled by the PWM signal, especially the IDDC whose relationship between the solenoid current and PWM duty ratio are not the same as the DDDC. In the previous paper [31], it is point out that the IDDC relationship between the solenoid current and the PWM duty ratio is nonlinear, and a solenoid current controller considering the nonlinearity is proposed to eliminate the zero lag by adding an offset PWM duty radio. In this paper, the reasons for this nonlinearity and the characteristics of the IDDC controlled by the PWM signal are analyzed mathematically in more details. The mathematical model, which is improved compared with the simplified drive model of the previous paper, is established based on the more detailed IDDC working processes in one PWM period. The computational equations of the significant nonlinear features including the critical PWM duty ratio, the steady-state current, the amplitude of the current oscillation, and the response time of the circuit are deduced through algebraic analyses. These analyses can aid the design of solenoid drive circuit and the modeling of the hydraulic proportional valve. What’s more, the current controller is improved from the previous simplified way by adding an offset PWM duty ratio to consider the whole nonlinearity of IDDC.

The remainder of this paper is organized as follows. Firstly, the unique nonlinear relationship between the current and the pulse-width modulation (PWM) duty ratio of the IDDC is pointed out based on experiment results in Section II. Then we establish the mathematical model of the IDDC based on the working processes in one PWM period to explain and simulate the IDDC nonlinear phenomena in Section III. Next, based on the state equations of the mathematical model, we analyze the nonlinear characteristics of the IDDC deeply in an algebraic way, and the corresponding equations for calculating the IDDC characteristic parameters are deduced in Section IV. Finally, to verify the necessity of analyzing the nonlinear characteristics of the IDDC, comparative experiments of the PI current controllers considering the nonlinearity are carried out in Section V. And several conclusions are presented in Section VI.

II. NONLINEAR CHARACTERISTICS OF THE IDDC

VOLUME XX, 2018 9

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The test facility used to investigate the IDDC characteristics is shown in Fig. 2. A computer records the experimental data and compiles the program. The J-link downloads the program into the valve controller. The data acquisition card collects the PWM signal data and the voltage data of the solenoid, and its sample frequency is 100 kHz. The oscilloscope monitors the related parameters of the experiment. The power supplier supplies electrical power to the valve controller and the drive circuit, and its upper limit of supply current is 4.8 A. The proportional solenoid used in the experiments is fixed in a certain position by the experiment setup to guarantee that the solenoid inductance is not affected by solenoid electromagnetic interactions.

With the test facility, the curves of the solenoid steady-state current vs. the input PWM duty ratio ($D$) at different PWM frequencies are obtained. The curves are nonlinear, as shown in Fig. 3. First, the current is saturated when the input PWM duty ratio is close to 100%. The saturation is caused by a limitation of the current supply. Second, the curves keep the same nonlinear characteristics, but shift to the left as the PWM signal frequency ($F$) increases. Furthermore, an interesting phenomenon is worth noting, i.e., there is a turning point of each curve as the PWM duty ratio increases. In this paper, the PWM duty ratio of the turning point is referred to as the critical PWM duty ratio $D_0$. When $D < D_0$, the steady-state current of the IDDC is only a few mA, and its slope is small. When $D > D_0$, the steady-state current of the IDDC shows a linear relationship to the PWM duty ratio of the control signal, and its slope is greater.

In Fig. 4, the inlet and outlet voltages of the solenoid in one PWM period are useful to comprehend the shifting of the curves and the critical PWM duty ratio $D_0$. There is a time delay from the moment of the PWM signal falling edge to the moment that the inlet voltage of the solenoid switches to a low level. This delay means that the actual PWM duty ratio is higher than the input PWM duty ratio of the control signal. Since this time delay is mostly a constant value due to the drive circuit hardware, the steady-state current curves shift to the left as the PWM signal frequency increases. What’s more, the voltage attenuates when $D < D_0$, as shown in Fig. 4(a).

The experimental current step responses of the IDDC at different PWM duty ratios with 2000Hz PWM frequency are shown in Fig. 5. When $D > D_0$, the current is in the steady-state as the current increment equals to the current decrement in one PWM period, as shown in Fig. 5 (a). And the current...
is in the rising-state as the current increment is more than the current decrement in one PWM period, as shown in Fig. 5 (b). When \( D < D_0 \), the steady-state current of the IDDC is only a few mA, since the time as the PWM signal is at a low level is long enough to let the current fall to zero in one PWM period, as show in Fig. 5 (c). These solenoid current details in Fig. 5 and the voltage attenuation in Fig. 4 (a) both indicate that the IDDC working processes in one PWM period with different PWM duty ratios can facilitate the exploration of the in-depth mechanism of the nonlinear characteristics.

In the following section of this paper, we will investigate these characteristics and experimental phenomena in a mathematical way, which is based on the analysis of the IDDC working processes in one PWM period.

### III. MATHEMATICAL MODEL OF THE IDDC AND SIMULATION

#### A. IDDC parameters and simplifying assumptions

The circuit schematic of the IDDC is shown in Fig. 1, where the solenoid (Anyang Kaidi GP37) can be simplified as an inductance \( L \) and a resistor \( R_t \) in series [7]. The proportional control of the solenoid current is realized by adjusting the PWM signal duty ratio. The IDDC working processes can be divided into the charging processes and the discharging processes as the PWM signal level changes. When the PWM signal is at a high level, the IDDC works during the charging processes. The photocoupler \( P_1 \) (TOSHIBA TLP521-1) and the MOSFET’s \( Q_1 \) (FAIRCHILD FQD17P06) and \( Q_2 \) (FAIRCHILD RFID16N06) are ON. In this case, the solenoid is charged by the power supply with a voltage \( U_p \) and the current flows through \( D_1 \), \( Q_1 \), \( R_t \), \( L \), and \( Q_2 \). When the PWM signal is at a low level, the IDDC works during the discharging processes. The photocoupler \( P_1 \) and the MOSFET’s \( Q_1 \) and \( Q_2 \) are OFF. The current is discharged through the diodes \( D_1 \) and \( D_2 \) to the capacitors \( C_1 \) and \( C_2 \).

The major current flows through \( D_1, R_t, L, D_2, \) and \( C_1 \) to the ground, and the minor current flows through \( D_3, R_t, L, D_2, \) and \( C_2 \). The diodes in the circuit are ES3D from TOSHIBA.

#### TABLE I

<table>
<thead>
<tr>
<th>Item</th>
<th>Value of parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{D1} )</td>
<td>0.15 ( \Omega )</td>
<td>The equivalent resistor of diode ( D_1 )</td>
</tr>
<tr>
<td>( R_{D2} )</td>
<td>0.15 ( \Omega )</td>
<td>The equivalent resistor of diode ( D_2 )</td>
</tr>
<tr>
<td>( R_{D3} )</td>
<td>0.15 ( \Omega )</td>
<td>The equivalent resistor of diode ( D_3 )</td>
</tr>
<tr>
<td>( R_{D4} )</td>
<td>0.15 ( \Omega )</td>
<td>The equivalent resistor of diode ( D_4 )</td>
</tr>
<tr>
<td>( R_L )</td>
<td>3.03 ( \Omega )</td>
<td>The equivalent resistor of solenoid</td>
</tr>
<tr>
<td>( L_{max} )</td>
<td>110 mH</td>
<td>The equivalent inductance of the solenoid</td>
</tr>
<tr>
<td>( L_{min} )</td>
<td>60 mH</td>
<td>The equivalent inductance of the solenoid</td>
</tr>
<tr>
<td>( R_{Q1} )</td>
<td>0.14 ( \Omega )</td>
<td>The equivalent resistor of MOSFET ( Q_1 )</td>
</tr>
<tr>
<td>( R_{Q2} )</td>
<td>0.03 ( \Omega )</td>
<td>The equivalent resistor of MOSFET ( Q_2 )</td>
</tr>
<tr>
<td>( C_1 )</td>
<td>880 ( \mu F )</td>
<td>The value of capacitor ( C_1 )</td>
</tr>
<tr>
<td>( C_2 )</td>
<td>230 ( \mu F )</td>
<td>The value of capacitor ( C_2 )</td>
</tr>
<tr>
<td>( k_1 )</td>
<td>150</td>
<td>Inductance correction coefficients</td>
</tr>
<tr>
<td>( k_2 )</td>
<td>145</td>
<td>Inductance correction coefficients</td>
</tr>
</tbody>
</table>

#### TABLE II

<table>
<thead>
<tr>
<th>Element</th>
<th>Turn-on time ( t_{ON} )</th>
<th>Storage time ( t_s )</th>
<th>Turn-off time ( t_{OFF} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photocoupler (( P_1 ))</td>
<td>3( \mu s )</td>
<td>15( \mu s )</td>
<td>25( \mu s )</td>
</tr>
<tr>
<td>P-channel MOSFET (( Q_1 ))</td>
<td>0.24( \mu s )</td>
<td></td>
<td>0.18( \mu s )</td>
</tr>
<tr>
<td>N-channel MOSFET (( Q_2 ))</td>
<td>0.1( \mu s )</td>
<td></td>
<td>0.115( \mu s )</td>
</tr>
</tbody>
</table>

To analyze the circuit, the photocoupler, the diodes, and the MOSFETs are simplified. When the PWM signal is at a high level, the photocoupler and the MOSFETs are ON. In this case, the MOSFETs are equivalent to resistors. The diodes are equivalent to the resistors when the voltage is forward and equivalent to a high impedance state when the voltage is reversed. Considering the electromagnetic interaction of the solenoid, especially the equivalent inductance of the solenoid changing with different positions of the plunger [6], the solenoid inductance \( L \) can be calculated by [32]

\[
L = \frac{N^2 A \mu_e}{l_e + \frac{\mu_e}{\mu_0} l_g}
\]

where \( N \) is the number of coil turns of the solenoid; \( \mu_e \) and \( \mu_0 \) are the permeability of the core and air, respectively; \( A_e \) is the effective cross-sectional area of the flux path; and \( l_e \) and \( l_g \) are the length of magnetic circuit inside the solenoid core and in the air gaps, respectively. Because the proportional solenoid used in the experiments is fixed in a certain position, which means that \( l_g \) is not changed, then the inductance of the solenoid is only affected by the permeability of the core \( \mu_e \).
The parameter $\mu_c$ is nonlinear due to the hysteresis of the ferromagnet, then is significantly affected by the current of the solenoid. Then, the nonlinearity of inductance is expressed by

$$L = \frac{L_{\text{max}} - L_{\text{min}}}{1 + \exp\left(-\frac{i_l}{i_s}\right)} + L_{\text{min}}$$  \hspace{1cm} (2)

where $i_l$ is the solenoid current; $i_s$ is the steady-state current in a fixed PWM duty ratio; $L_{\text{max}}$ is the inductance when the solenoid current is at a steady-state; $L_{\text{min}}$ is the inductance when the solenoid current is rising and has not reach the steady-state current; and $k_1$ and $k_2$ are the correction coefficients. This equation renders the solenoid inductance $L$ be approximately $L_{\text{min}}$ when the solenoid current does not reach the steady-state current, and makes $L$ be approximately $L_{\text{max}}$ when the solenoid current is near the steady-state current. The corresponding parameters are listed in TABLE I.

When the frequency of the PWM signal is at a several kHz level, the time delay of the photocoupler $P_1$ and MOSFETs $Q_1$ and $Q_2$ will produce an actual PWM duty ratio higher than the input PWM duty ratio in experiments, as shown in Fig. 4. The actual PWM duty ratio reflects the ON/OFF time of the solenoid drive circuit, and the input PWM duty ratio is the input signal of the photocoupler. In the simulation, the PWM signal of the mathematical model exactly reflects the ON/OFF time of the solenoid drive circuit, and the time delay of the electrical elements, which causes a shift in the PWM duty ratio, is added to the input PWM duty ratio. The related parameters of the time delay are shown in TABLE II according to the electrical element datasheet. In addition, the shift in the PWM duty ratio $D_{\text{shift}}$ can be determined by

$$D_{\text{shift}} = \Delta t_{\text{delay}} = (t_{\text{t1}} + t_{\text{OFF}} - t_{\text{ON}}) F_c$$

which means that the actual PWM duty ratio is always 7.4% higher than the input PWM duty ratio when $F_c = 2000$ Hz. Notably, there may be some deviation in this $D_{\text{shift}}$ due to the time delay drift of the photocoupler and MOSFETs. This time delay of the electrical element causes a control dead zone of the actual PWM duty ratio, but the existence of $D_0$ in the IDDC can avoid this effect on the current controller.

**B. Mathematical model of the IDDC working processes and simulation results**

The mathematical model of the circuit working processes is useful for understanding the IDDC characteristics. The processes can be described as six equivalent circuits in one period of the PWM signal, as shown in Fig. 6. The notations in Fig. 6 are listed in TABLE I. The equivalent circuits (a), (b), and (c) represent the working processes when the PWM signal is at a high level, and the equivalent circuits (d), (e), and (f) represent the working processes when the PWM signal is at a low level. The corresponding mathematical models of the six working processes are described below.

![FIGURE 6. The working processes of the IDDC.](image)

**Process (a):**

When the PWM signal is at a high level, the MOSFETs are ON. The voltages $U_{C1}$ and $U_{C2}$ of capacitors $C_1$ and $C_2$ are zero initially. The major current of the IDDC flows through $D_1$, $Q_1$, $R_L$, $L$, $Q_2$, and lastly to ground, and a part of the current is charged into the capacitors $C_1$ and $C_2$, as shown in Fig. 6 (a). According to Kirchhoff's law, this working process can be described by

$$\begin{align*}
    i_l &= U_s - U_{C2} - C_2 \frac{dU_{C2}}{dt} \\
    U_{C2} &= \left( i_l - \frac{dU_{C1}}{dt} C_1 \right) R_{Q2} + \frac{di_l}{dt} L + i_l (R_L + R_{Q1}) \hspace{1cm} (3)
\end{align*}$$

$$\begin{align*}
    i_l - \frac{dU_{C1}}{dt} C_1 R_{Q2} = U_{C1} + \frac{dU_{C1}}{dt} C_1 R_{C2}
\end{align*}$$

where $i_l$ is the current flowing through the solenoid.

**Process (b):**

When the charging process of capacitor $C_1$ is completed, the current only flows through $D_1$, $Q_1$, $R_L$, $L$, $Q_2$, and lastly to ground, as shown in Fig. 6 (b). According to Kirchhoff's law this working process can be described by

$$\begin{align*}
    i_l &= U_s - U_{C2} - C_2 \frac{dU_{C2}}{dt} \\
    U_{C2} &= i_l \left( R_L + R_{Q1} + R_{Q2} \right) + L \frac{di_l}{dt} \hspace{1cm} (4)
\end{align*}$$

For the working process (b), solving (4), the solution of $i_l$ is

$$i_l(t) = \frac{U_s}{R_L} \left[ 1 - e^{-\frac{R_{Q1} + R_{Q2} + R_L}{L} t} \right]$$  \hspace{1cm} (5)

where $R_L = R_{Q1} + R_{Q2} + R_{Q1} + R_{Q2}$ is the total resistance of the process (b) and the initial condition is $i_l(0) = 0$.

**Process (c):**

When $U_{C1} > U_s$, the equivalent circuit diagram is shown in Fig. 6 (c). Then, the mathematical model of this working process is

$$\begin{align*}
    i_l &= \frac{U_s}{R_L} \left[ 1 - e^{-\frac{R_{Q1} + R_{Q2} + R_L}{L} t} \right]
\end{align*}$$
When the charging current equals zero, the charging process of the capacitor is completed. The remaining energy will oscillate in the circuit. The equivalent circuit diagram is shown in Fig. 6 (f), where this working process can be described by

\[
\begin{align*}
\frac{dU}{dt} &= -i_L \\
U_{c2} &= U_s - R_d C_2 \frac{dU_{c2}}{dt} \\
di_L L + i_L R &= U
\end{align*}
\]

where \( C \) is the equivalent capacitor of the oscillating circuit; \( R \) is the equivalent resistor; and \( U \) is the voltage between the inlet and outlet of the solenoid.

Solving (11), the solution of \( i_L \) follows the same form as (10). However, according to the electrical parameters, the equivalent resistor is very high, and the equivalent parasitic capacitor is very small. Therefore, the working process (f) is an overdamped RLC circuit in this case \( C_1 R_5^2 - 4 C_1 L > 0 \).

Based on the mathematical model of the IDDC, the simulation model of the drive circuit is constructed. The simulate program is written in the MATLAB Script environment. The ODE45 function with 1e-6s step time and conditional program control are used to simulate the state equations of the mathematical model. The simulated current step responses at the frequency of 2000 Hz with different PWM duty ratios are shown in Fig. 7. The results of the experiments and simulations show that the IDDC has a high current discharging speed. The consistency of the simulated and experimental current step responses verifies the correctness of the mathematical model. The differences between the simulated and experimental current step responses are due to the simplification of the electrical parameters, especially the equivalent inductance of the solenoid which changes due to hysteresis.

\[
L_0 = -C_1 \frac{dU_{c1}}{dt} - C_2 \frac{dU_{c2}}{dt}
\]

\[
U_{c2} = \frac{di_L}{dt} + i_L \left( C_1 + R_{d4} C_1 \right)
\]

(6)

Process (d):

When the PWM signal is at a low level, the MOSFETs are OFF. The energy stored in the solenoid will be charged into the capacitors \( C_1 \) and \( C_2 \) until the voltage of capacitor \( C_1 \) is higher than the outlet voltage of the solenoid. In this case, the major current flows through \( D_2, R_1, L, D_2 \) and is charged into \( C_1 \) at last. The remaining current is charged into \( C_2 \). The equivalent circuit diagram is shown in Fig. 6(d), where this working process can be described by

\[
\begin{align*}
i_L &= C_1 \frac{dU_{c1}}{dt} + C_2 \frac{dU_{c2}}{dt} \\
U_{c1} &= -i_L \left( R_1 + R_{d2} + R_{d3} \right) - \frac{di_L}{dt} L \\
U_{c2} &= U_{c1} + \frac{dU_{c1}}{dt} R_{d4} C_1
\end{align*}
\]

Process (e):

When \( U_{d2} > U_{c2} > U_{c1} \), the energy stored in the solenoid is only charged into \( C_1 \). The equivalent circuit diagram is shown in Fig. 6(e), where this working process can be described by

\[
\begin{align*}
i_L &= C_1 \frac{dU_{c1}}{dt} \\
\frac{dU_{c2}}{dt} C_2 &= U_s - \frac{U_{c2}}{R_{d1}} \\
U_{c1} &= -i_L \left( R_1 + R_{d2} + R_{d3} \right) - \frac{di_L}{dt} L
\end{align*}
\]

(8)

Solving (8), the solution of \( i_L \) is

\[
i_L(t) = i_0 e^{\alpha t} \cos(\omega t) - \left( \frac{2 U_0 + R_i L_0}{2 \alpha \omega L} \right) e^{\alpha t} \sin(\omega t)
\]

(9)

where \( \omega = (C_1 R_5^2 - 4 C_1 L)^{1/2} / (2 C_1 L) \); \( \alpha = R_5 / L_0 \); \( i_0 \) is the initial solenoid current in the working process (e); \( U_0 \) is the initial voltage of capacitor \( C_1 \); and \( R_5 = R_{d2} + R_{d3} + R_L \) is the total resistance of the process (e).

According to the electrical parameters in TABLE I, the working process (5) is an underdamped RLC circuit. In this case, \( C_1 R_5^2 - 4 C_1 L < 0 \); thus, \( \omega \) is a pure imaginary number defined as \( \omega = \beta i \), and \( i_0 \) can be calculated by

\[
i_L(t) = i_0 e^{\alpha t} \cos(\beta t) - \left( \frac{U_0}{L \beta} + \frac{R_i L_0}{2 L \beta} \right) e^{\alpha t} \sin(\beta t)
\]

(10)

Process (f):

\[
\begin{align*}
i_L &= C_1 \frac{dU_{c1}}{dt} \\
\frac{dU_{c2}}{dt} C_2 &= U_s - \frac{U_{c2}}{R_{d1}} \\
U_{c1} &= -i_L \left( R_1 + R_{d2} + R_{d3} \right) - \frac{di_L}{dt} L
\end{align*}
\]

When the charging current equals zero, the charging process of the capacitor is completed. The remaining energy will oscillate in the circuit. The equivalent circuit diagram is shown in Fig. 6 (f), where this working process can be described by

\[
\begin{align*}
\frac{dU}{dt} &= -i_L \\
U_{c2} &= U_s - R_d C_2 \frac{dU_{c2}}{dt} \\
di_L L + i_L R &= U
\end{align*}
\]

\[\text{FIGURE 7. Simulated and experimental current step responses of the IDDC at a frequency of 2000 Hz with different PWM duty ratios.}\]
We can more accurately learn the circuit characteristics by analyzing the functions of the circuit working processes in an algebraic way.

A. Critical PWM duty ratio

To obtain an analytical method to solve the critical duty ratio $D_0$, it is useful to zoom in on a few PWM periods to observe the current variation in the solenoid with the PWM duty ratios $D<D_0$. In this case, ignoring the infrequent working processes (a), (c), and (d), the working processes contain (b), (e) and (f), as shown in Fig. 8 (a). As shown in Fig. 4, there is a voltage attenuation when $D<D_0$. The attenuation occurs because the circuit works during the process (f) when the PWM signal is at a low level. In this case, during one PWM period, the time when the PWM signal is at a low level is long enough for the charging current of the working process (b) to decline to zero as the circuit works during the process (e). After the current declines to zero, the voltage of the solenoid attenuates as the circuit works during the process (f). Thus, the steady-state current of the IDDC is only a few mA. As the PWM duty ratio increases to the critical value $D_0$, the increment in the charging current during the working process (b) is equal to the decrement in the discharging current during the working process (e) as the PWM duty ratio increases to the critical value $D_0$. Thus, $D_0$ satisfies

$$
i_{up} = \frac{U_i}{R_2} \left( 1 - e^{-\frac{R_i D_T}{L}} \right)
$$

$$
i_{up} e^{\alpha (1-D_0)T} \cos \left( \beta (1-D_0)T \right)
$$

$$
- \left( \frac{U_0}{L \beta} + \frac{R_i}{2 \beta} \right) e^{\alpha (1-D_0)T} \sin \left( \beta (1-D_0)T \right) = 0
$$

where $i_{up}$ is the maximum current of the solenoid when the PWM signal is at the falling edge during one PWM period and $T$ is the cycle time of the PWM signal. To obtain the input critical PWM duty ratio $D_0$ of the input PWM signal, the real $D_{shift}$ should be subtracted.

A simpler calculated equation for $D_0$ can be deduced, as shown below. The derivations of Equations (5) and (10) are

$$\frac{d i_L(t)}{dt} = \frac{U_i}{L} e^{-\frac{R_i}{L} t}
$$

$$\frac{d i_L(t)}{dt} = -\alpha i_L e^{-\alpha t} \cos(\beta t) - \beta i_L e^{-\alpha t} \sin(\beta t)
$$

As the frequency of the PWM signal is high, the cycle time of the PWM signal is short enough to calculate the current by

$$t \to 0, \quad \frac{d i_L(t)}{dt} = \frac{U_i}{L},
$$

$$t \to 0, \quad \frac{d i_L(t)}{dt} = -\frac{3 R_i}{2 L} \frac{U_0}{L}.
$$

With the same analysis method as (12) and the condition that $i_0=0$, $D_0$ satisfies

$$\begin{cases}
i_{up} = \frac{U_i}{L} D_0 T \\
i_{up} = \frac{U_i}{L} (1-D_0) T = 0
\end{cases}
$$

Solving (17), $D_0$ is

$$D_0 = \frac{U_i}{U_0 + U_c}.
$$

According to (18), the value $D_0$ is affected by the relative size between $U_0$ and $U_c$. In addition, in the actual working
state, the circuit is always activated, thus the capacitor has enough time to charge to the voltage that \(U_0 = U_{i_w}\) and \(D_0\) is approximately 50%.

Since the frequency of the PWM signal has little influence on the actual critical PWM \(D_0\) according to (18), the real time delay \(t_{\text{delay}}\) of the electrical elements can be deduced based on the experimental steady-state current of solenoid with two different frequency PWM signals,

\[
\begin{align*}
D'_{01} + D'_{\text{shift1}} &= D'_{02} + t_{\text{delay}}F_1 = D_0 \\
D'_{02} + D'_{\text{shift2}} &= D'_{02} + t_{\text{delay}}F_2 = D_0 \\
\end{align*}
\]

(19)

where \(F_1\) and \(F_2\) are different frequencies of the PWM signal; \(D'_{01}\) and \(D'_{02}\) are the input critical PWM duty ratios at the corresponding frequencies; and \(D'_{\text{shift1}}\) and \(D'_{\text{shift2}}\) represent the shift in the PWM duty ratios at the corresponding frequencies.

According to the experimental results of Fig. 3, the input critical PWM duty ratios \(D'_{01}\) and \(D'_{02}\) of the solenoid steady-state current at frequencies \(F_1=1500\) Hz and \(F_2=5000\) Hz are 40% and 26%, respectively. Thus, the real time delay \(t_{\text{delay}}\) is 40 \(\mu\)s calculated by (19). The real time delay is longer than the parameters of the TABLE II according to the datasheet of the electrical element. This longer delay may be because of electrical element degradation. In addition, the real shift in the PWM duty ratio at a frequency 2000 Hz is modified to 8%.

### B. Steady-state current and its oscillation amplitude of the IDDC

Two states can be considered to calculate the steady-state current \(i_c\) of the IDDC. First, when \(D < D_0\), the current is a few mA. The parameter \(i_c\) can be calculated by

\[
i_c = \frac{i_{\text{up}}}{2}
\]

(20)

where \(i_{\text{up}}\) is calculated by (12).

Second, when \(D > D_0\), as the time of step response increases, the increment in the charging current is equal to the decrement in the discharging current in one PWM period. Thus, the steady-state current \(i_c\) is achieved (Fig. 8 (b)), which satisfies Equations (21), (22). In the equations, \(i_0\), \(i_{\text{up}}\) and \(i_c\) are unknown parameters, where \(i_0\) is the current when the PWM signal is at the rising edge and \(i_{\text{up}}\) is the current when the PWM signal is at the falling edge as shown in Fig. 8(b). The parameter \(t_0\) is the corresponding time of \(i_0\) when the circuit works in only process (b).

\[
i_0 = \frac{U_i}{R_2}\left(1 - e^{-\frac{R_0L}{L}}\right)
\]

(21)

\[
i_{\text{up}} = \frac{U_i}{R_2}\left(1 - e^{-\frac{R_0L}{L}}\right)
\]

(22)

The steady-state current of the solenoid calculated by (20), (21), and (22) are shown in Fig. 9 (a). The black dashed curve of the current is calculated by the equations, in which the time delay of the electrical elements is not considered. The black solid curve of the simulated current is shifted to left by 8% PWM duty ratio considering the time delay of the electrical elements, which is consistent with the experimental steady-state current except the saturation caused by the power supplier.

In the case of the high frequency PWM signals, the equations calculating the steady-state current can be simplified by

\[
i_0 = \frac{U_i}{R_2}\left(1 - e^{-\frac{R_0L}{L}}\right)
\]

\[
i_{\text{up}} = \frac{U_i}{L} e^{-\frac{R_0L}{L}} DT + i_0
\]

\[
i_c = i_0 + \frac{i_{\text{up}}}{2}
\]

(23)

Solving (23), we can obtain

\[
i_0 = \frac{2(DU_0 - U_0 + DU_{i_0})}{3R_s + 2DR_2 - 3DR_3}
\]

(24)

\[
i_{\text{up}} = \frac{2(D\frac{2\Delta V_0}{3R_s}\frac{3R_s}{3R_s} + 2L + 3R_s T - 3DR_s T)}{3R_s [L(3R_s - 3DR_s) + 2DLR_3} - \frac{2U_{i_0}}{3R_s - 3DR_3}
\]

(25)

When \(U_0 = U_{i_0}, R_s = R_s = R\), we can obtain

\[
i_0 = \frac{4D - 2 U_i}{3 - D} R
\]

(26)

\[
i_{\text{up}} = \frac{U_i(2L - 4DL - 5DRT + 5D^2RT)}{LR(D - 3)}
\]

(27)
As we have analyzed the steady-state current of the IDDC, its oscillation amplitude $\Delta i$ can be calculated by $\Delta i = i_{wp} - i_0$, where $i_0$ and $i_{wp}$ can be gotten by (21), and the result is shown in Fig. 9 (b).

In the case of high-frequency PWM signals, $\Delta i$ can also be calculated by

$$\Delta i = \frac{5(D-D^3)U_i T}{3-D} \frac{L}{L} \tag{28}$$

As shown in Fig. 9 (b), the current oscillation amplitude increases as the PWM frequency decreases, and varies with the PWM duty ratio. This result can also be concluded from (28).

The current oscillation amplitude affects the energy consumption of the IDDC in one PWM period, which can be calculated by

$$E = \int_0^{DT} \left[ i_0 + \frac{\Delta i}{DT} t \right]^2 R_s dt + \int_0^{(1-D)T} \left[ i_{wp} - \frac{\Delta i}{(1-D)T} t \right]^2 R_s dt \tag{29}$$

Simplifying (29), we obtain

$$E = i_0^2 D T R_s + i_0 \frac{\Delta i}{DT} T R_s + \frac{\Delta i^2}{3} (DT)^2 R_s + i_{wp}^2 (1-D) T R_s - i_{wp} \frac{\Delta i}{(1-D)T} T R_s + \frac{\Delta i^2}{3} ((1-D)T)^2 R_s \tag{30}$$

According to (30), the increment in the PWM frequency can decrease the energy consumption.

C. Discrete and continuous state equation of the IDDC current

To obtain the discrete and continuous state equation of the IDDC current when $D>D_0$, it is useful to analyze the working processes (b) and (e) in one PWM period. Assuming that the voltages of the capacitors $C_1$ and $C_2$ are charged to the level of the power supply, and according to (4), the derivative of the current in process (b) is

$$\frac{di_k}{dt} = \frac{U_s - i_k R_s}{L} \tag{31}$$

In the case of a high frequency PWM signal, according to (16), the discrete state equation of the IDDC current is

$$i_{k+1} = i_k + \Delta i = i_k + \frac{U_s - i_k R_s}{L} DT \tag{32}$$

where $i_k$ is the current of the solenoid at the rising edge of a PWM signal.

When $R_c = R_2 = R$, we can obtain

$$i_{k+1} = \left[ 1 + \frac{RT}{2L} \left( D - 3 + \frac{3RT}{L} (D - D^3) \right) \right] i_k + \frac{U_s T}{2L} (2D - 1) \tag{33}$$

Additionally, ignoring the high-order term of $T$, the discrete state equation of the current can be simplified as

$$i_{k+1} = i_k + \frac{RT}{2L} (D - 3) i_k + \frac{U_s T}{L} (2D - 1) \tag{34}$$

Based on the discrete state equation of the current, the continuous state equation of the IDDC current can be deduced by $\frac{di}{dt} = (i_{k+1} - i_k) / T$. In the case of $R_c = R_2 = R$, it is

$$\frac{di}{dt} = \frac{R}{2L} \left( D - 3 + \frac{3RT}{L} (D - D^3) \right) i_k + \frac{U_s T}{L} (2D - 1) + \frac{3RU_i^2 T^2}{2L^2} (D^2 - D) \tag{35}$$

The simplified equation when ignoring the term of $T$ is

$$\frac{di}{dt} = \frac{R}{2L} (D - 3) i_k + \frac{U_s T}{L} (2D - 1) \tag{36}$$

Let (36) equal to zero, Eq. (26) calculating the IDDC steady-state current can be got.

D. Rising time and falling time of the IDDC current step response

According to the continuous state equation of the IDDC current, the rising time of the IDDC current step response in a certain steady-state current $i_0$ can be estimated. The
following deduced process is in the case of \( R_S=R_L=R \) and ignore the term of \( T \).

The current of the solenoid in a fixed duty ratio can be calculated according to (36) as

\[
i = \frac{4DU_s - 2U_s + (2U_s - 4DU_s)e^{\frac{(3R - DR)}{2L}}}{3R - DR}.
\] (37)

Then, the time when the current of the solenoid rises to \( i_m \) can be calculated by

\[
t = \frac{2L}{3R - DR} \ln \left( \frac{i_m (3R - DR)}{2U - 4DU_s} + 1 \right).
\] (38)

The duty ratio of the IDDC at a certain steady-state current \( i_0 \) can be calculated according to (26) as

\[
D = \frac{3Ri_0 + 2U_s}{Ri_0 + 4U_s}.
\] (39)

Substituting (39) into (38), the time when the current increases to \( i_m \) is

\[
t = \frac{4LU_s + LRI_0}{5RU_s} \ln \left( \frac{i_0 - i_m}{i_0} \right).
\] (40)

If we define the rising time as the current \( i_m \) increase to 90% of \( i_0 \), then it can be calculated by

\[
t_{up} = \frac{4LU_s + LRI_0}{5RU_s} \ln (0.1).
\] (41)

Additionally, the rising time of the DDDC can be also deduced in the similar method, and can be calculated by

\[
t_{up} = -\frac{L}{R} \ln (0.1).
\] (42)

Substituting the relative parameters \( L=85 \) mH, \( R=3.3 \) \( \Omega \), \( U_s=24 \) V, the rising times of the IDDC and the DDDC in the case of \( i_0=2 \) A are 50.7 ms and 59.3 ms respectively.

![FIGURE 10. Current discharging of the DDDC and the IDDC](image)

The falling time of the current step response of the IDDC can be analyzed as below. The current discharging working process (e) of the IDDC is an underdamped RLC circuit, while the current discharging working process of the DDDC is an RL circuit, as shown in Fig. 10. The falling time of the IDDC is the first time when the oscillating current of the RLC circuit reaches zero, while the falling time of the DDDC is the time when the current attenuates to zero. Thus, the falling time of the IDDC is shorter than the DDDC. The specific values of falling time can be calculated mathematically.

The current at the falling moment of the DDDC satisfies

\[
i_L = i_{f0} e^{\frac{-R_L}{L}}
\] (43)

where \( R=R_{D2}+R_L \) and \( i_{f0} \) is the initial current of the circuit at the current discharging working processes.

If the current decreases to \( e^{-0.95} (\approx 5\%) \) of the steady-state current, the falling time \( t_{down} \) of the DDDC is

\[
t_{down} = \frac{3L}{R}.
\] (44)

Substituting the relative parameters, \( t_{down}=77.3 \) ms.

The current at the falling moment of the IDDC satisfies

\[
i_L (t) = i_L e^{-at} \cos \left( \beta t \right) - \frac{U_{a0} + R_{i0}}{L\beta} e^{-at} \sin \left( \beta t \right)
\] (45)

\[
< i_L \cos \left( \beta t \right) - \frac{U_{a0} + R_{i0}}{L\beta} \sin \left( \beta t \right)
\] (46)

We can conclude that the falling time of the IDDC is longer than the falling time of the assumptive current with the initial slope and is shorter than the 1/4 cycle of the current calculated by (45), which satisfies

\[
\frac{3}{2} i_0 \frac{U_{a0}}{L} < T_{down} < \frac{\pi}{2\beta} = \frac{\pi}{2} \frac{1}{LC} \frac{R_S}{4L^2}.
\] (46)

Substituting the relative parameters when \( i_0=2 \) A, we get 5 \( \text{ms} < t_{down} < 13.8 \) ms. According to (46), decreasing the value of the capacitor \( C_1 \) appropriately can improve the response speed of the IDDC.

V. PI CURRENT CONTROLLER DESIGN WITH THE IDDC INVERSE STEADY-STATE CURRENT NONLINEARITY INTEGRATED

A. Design of PI current controller

To verify the necessity of analyzing the nonlinear characteristics of the IDDC, comparative experiments of the PI current controllers considering the nonlinearity were carried out. To simplify the design of the controller, the IDDC and the proportional solenoid are simplified as an RL circuit driven by voltage \( U_{i0} \). The PI current controller can be designed based on this simplification, and the input \( U_i \) can be calculated by the controller. Then, the input PWM duty ratio \( D \) for the current control can be calculated according to \( U_{i0} \). The relationship \( f(D) \) between \( U_{i0} \) and \( D \) depends on the current characteristic of the drive circuit as shown in (47), where \( i_t \) is the steady-state current of the solenoid when \( D=100\% \). The PI current controller with the PWM signal
input can be designed, as shown in Fig. 11, where \( f^{-1}(U_L) \) is the inverse function of \( f(D) \).

\[
U_L = f(D) = U_s \frac{i(D)}{i_I} \tag{47}
\]

![Schematic of the PI current controller with the PWM signal input.](Image)

The classical current controller considers that the current is proportional to the PWM duty ratio as

\[
i(D) = D i_I \tag{48}
\]

However, the IDDC characteristic of current vs. PWM duty ratio is nonlinear, so a better current controller can be designed when the nonlinearity is considered. The nonlinear characteristic \( i(D) \) can be written as (49), where \( i_{D0} \) is the solenoid steady-state current when \( D=D_0 \).

\[
i(D) = \begin{cases} 
D \frac{i_{D0}}{D_0}, & D < D_0 \\
\left(D-D_0\right) \frac{i_I-i_{D0}}{1-D_0}, & D > D_0
\end{cases} \tag{49}
\]

And \( f^{-1}(U_L) \) can be written as

\[
D = f^{-1}(U_L) = \begin{cases} 
\left(U_L - i_{D0} \frac{1}{U_s} \right) D_0, & U_L i_I \leq i_{D0} \\
\left(U_L - i_{D0} \frac{1}{U_s} \right) + D_0, & U_L i_I > i_{D0}
\end{cases} \tag{50}
\]

which is the IDDC inverse steady-state current nonlinearity control law integrated in the PI current controller.

**B. The experimental results**

Fig. 12 shows the current tracking results of the PI controllers with and without the nonlinear characteristic. The parameters of the PI controllers are adjusted by the Ziegler Nichols tuning procedure initially and manually optimized later. In the experiment, the proportional gain and integral gain of the PI controller with the IDDC nonlinearity are 20.8 and 2.12 respectively, and those of the PI controller without the nonlinearity are 24.2 and 2.45, respectively in the case that current unit is in mA and 100% PWM duty ratio is equivalent to 10000. The controllers are implemented in an ARM processor based MCU with a cycle time of 120 \( \mu \)s. As shown in Fig. 12, the response time is shorter when the PI controller considers the nonlinear characteristic. This behavior is because the controller compensates for the IDDC nonlinearity. This compensation causes the controller output PWM duty ratio to step over the segment in which the corresponding steady-state current is as small as \( D<D_0 \); thus, the current increases more rapidly.

**VI. CONCLUSION**

This paper analyzes the nonlinear characteristics of the IDDC for the proportional solenoid. The mathematical models of the working processes of the circuit are constructed, which helped to understand the principles of the IDDC nonlinear characteristics in detail and improve the control performance of the solenoid controller. The following conclusions are reached.

1. The calculation equation of the critical PWM duty ratio \( D_0 \) that is crucial for the nonlinear relationship between the steady-state current and the PWM duty ratio \( D \) of the IDDC is established. When \( D>D_0 \), the current of the solenoid is only a few mA which is too small to push the core of solenoid. When \( D>D_0 \), the current has a linear relationship with the PWM duty ratio of the controlling signal. The left shift in \( D_0 \) with an increasing PWM frequency is due to the time delay of the photocouplers and MOSFETs.

2. The computational equations of the steady-state current of the solenoid and the amplitude of the current oscillation are deduced and verified by the comparisons between experimental and calculated data. Moreover, the high PWM frequency helps to decrease the amplitude of the current oscillation and energy consumption of the IDDC.

3. The computational equations of the rising time and falling time corresponding to the IDDC and the IDDC are deduced, which helps to reveal the reason why the IDDC has a faster response speed than the DDDC. This reason is because that the current discharging working process of the IDDC is an under-damped RLC circuit, while that of the DDDC is an RL circuit. In addition, it is pointed out that the value of the capacitor \( C_1 \) is the key parameter for determining the falling time of the IDDC.

4. The PI current controller, which considers the nonlinear characteristics of the IDDC, has a much faster response speed than a traditional PI controller.

**REFERENCES**

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