Abstract— Due to the fruitful growth in the industry of medical devices especially in Implantable Medical Devices (IMD), the research in this area has grown in the past few years. This paper presents an embedded processor platform chip suitable for medical applications requiring minimal power consumption. While this paper focuses on the key electronic features of implantable circuits and the integration of these features into silicon, it covers a proposed chip-architecture in design. This proposed design explores the partitioning of a chip as well as the trade-offs associated with design choices especially intelligent power management. Finally, it briefly covers the key attributes required in the silicon technology used for implementing implantable integrated circuit (IC) designs.

Index Terms—Cardiac Implant, Neural Implant, Ultra Low Power (ULP), Implantable Medical Device (IMD) System Architecture, Power Management, Signal Processing, Energy Harvesting.

I. INTRODUCTION

THE recent Implantable Medical Devices (IMDs) are basically devices or objects that are surgically inserted into the human body for medical reasons [1]. With the ever increasing clinical need for implantable devices comes the continuous sequence of challenges, with the need to reduce size, weight and power. Thus, creating an integrated chip for implantable medical device becomes a necessity. These IMDs need to provide therapy to treat numerous conditions reliably at minimal cost, such as cardiac disorder, pain management, Parkinson’s disease, epilepsy, bladder control, gastrointestinal disorders, numerous autoimmune diseases and psychological disorders. On the top of it has become possible to positively affect the physiological processes at sub-micron scales initiated upon implantation, due to the advancements in the field of nanotechnology.

Implantable medical devices are greatly required for the survival of patients suffering from above cited diseases, enabling normal quality of patients’ lives with various IMDs, such as the implantable cardiac pacemaker, cochlear implant, and implantable deep brain stimulator (DBS) [2-18]. These IMDs need several requirements to be addressed such as small volume (minimal size and weight), long lifespan, low power consumption, high biocompatibility, and good reliability. With recent medical and engineering advances, there is a miniaturization process going on in the implantable medical devices field. So, Medical devices are now a pervasive part of modern medical care, and have extended the ability of physicians to diagnose and treat diseases, making great contributions to health and quality of life [1].

Recent IMD applications demand higher performance and power efficiency to enable sophisticated treatment paradigms [9-12]. This intensive integration of system-on-chip (SoC), drives the research of solutions towards an emerging implantable product application area characterized by critical design methodologies and power requirements, called Ultra Low Power (ULP) Electronics in analog as well as digital domain [1,2,25]. As the industry of the IMDs develops, lowering the power consumption as much as possible is essential in improving the service time of the battery, which cannot be replaced frequently.

For achieving ULP design, it requires innovations in all aspects of the IC Design including system architecture, microarchitecture, circuit design, digital implementation, and process selection. At the system architecture level as shown in Fig. 1, a judicious combination of programmable and hard-wired processing elements is needed to ensure the ability to map different algorithms, while consuming significantly lower power.

![Fig. 1. Generic System Architecture and Functional Modules for Implantable Medical Device](image)

A large part of the costs associated with IMD arises from the surgical implantation itself. Thus, one key objective for future IMD’s is the development of a technology that would combine the reliability and simplicity of use of an implanted interface with the low cost and low morbidity of a non-surgical approach. Another important objective for future implantable devices is increased reliability and reduction of the side effects. For this purpose, these devices are perfectly sealed by biocompatible materials.

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In Section II, the requirements for system architecture are discussed. Section III describes the proposed System architecture. Section IV describes power management algorithm demonstrated in this architecture, with results, followed by conclusions in Section V.

### II. DESIGN REQUIREMENTS

For the system to be fully implantable in the tissue its total volume needs to be limited by the amount of tolerable tissue displacement to avoid significantly disrupting the physiological system. For the architecture shown in Fig. 1, the most optimal design for future generations of the ULP and biocompatible IMDs should be based on modules with the following key properties:

i) Optimized in size to be located directly at the site where stimulation and sensing occur, thus eliminating the need of a separate Implanted Pulse Generator (IPG), and the leads for improved efficiency as a consequence.

ii) Should have some basic self-targeting and adaptive properties to only stimulate the specified tissue in appropriate places, help in initial placing and adapt if the stimulation needs a change, thereby reducing surgical intervention.

iii) Programmable by the treatment provider for optimal functioning, capable of receiving and transmitting data to the control unit and/or other implanted devices

iv) Capable to run autonomously for prolonged period of time (ideally lifetime of the patient).

v) Temperature protection for the survival of the surrounding tissues.

The first requirement implies presence of ultra small volume of IPG unit, while the second requirement gives improved spatial as well as temporal resolution of multiple site electrodes for both sensing and stimulation. The third requirement implies even more critical design of sophisticated electronic components in the system: it needs to have integrated package containing all the main components of the traditional implants, like interface electronics, pulse generator, power source, and telecom. The fourth requirement for the autonomous operation for several years can be satisfied with Energy Harvesting for batteryless designs [3,4,5] including intelligent power management techniques to support continuous performance of IMDs having an array of electrodes [12][13].

In fact, the battery is one of the main limiting factors in miniaturization of the implantable devices and is the main hurdle in satisfying the first requirement. Therefore, supplying the IMDs with primary batteries will be a secondary option because of their large volume, limited lifetime, difficult replacement, and cost [13][15][16]. Therefore, the power consumption of the new IMDs is going to be major concerns as compared to the traditional IMDs [14], hence making Power Management Unit (PMU) and batteryless design, a critical requirement for an IMD.

The fifth requirement considers the temperature at the outer surface of the IMD, which should not increase more than 2 °C for the surrounding tissue to survive [17], it is of utmost importance for the inductive link and the IMD power management circuitry to maintain performance without generating excessive heat. So, the necessity of a temperature control in IMDs is evident.

#### A. Biomedical Interface and Signals

Regarding the interface between electronic device and electrogentic cells, it is understood that electrical currents in integrated circuits, sensors and stimulating electrodes are carried by free electrons, while electrical currents in biological tissues are carried by the motion of ions. However, basic interface mechanism for passing current from one medium to the other is done through electrochemical reaction [2,9].

However, biomedical signals normally have slow dynamics with useful information at frequencies less than 1 kHz [3,4,5], while clock frequencies required for processing of such signals are normally lower than 1 MHz. Owing to extremely low ionic mobility, all the possible electrical signals in the humans are limited to sub 10kHz band. On the higher side of this spectrum, spike signals are distributed, while collective signals, such as local field potentials (LFP), fall into sub-kHz range with amplitudes in µV to mV range [3,5,6,10,11,12]. Due to this, pre-processing [4,8,24] is required to get the desired stimulation.

Depending on the physiological application, the spatial resolution can vary, ranging from few mm to few µm for both sensing and stimulation interfaces [11]. To keep the volume on the lower side, a needle shape electrode interface can be plausible [11,33].

#### B. Functional Modules

Towards motivation of having an efficient multi-site sensing and stimulation capabilities, the proposed SoC basically an application engine for IMD applications. It features processing of extensive physiological signals, with communication facilities to outside equipments. Fig. 2 shows the generic functional view.

The most critical factor is the need to contain in one package all the functional modules of the IMD, like interface electronics, pulse generator, power source, and communication protocol.

![Fig. 2. Generic Application View of IMD](image-url)
to have extra amplification and, perhaps, additional signal to noise discrimination and signal filtering. The critical modules shown in Fig. 1 are described as following:

**Sensing and Analog Front End (AFE):** signal acquisition, amplification and conversion into digital data stream. This function allows a medical device to determine what action to take and/or what therapy to deliver. In sensing, the signals are generated by the organism and are only collected by the sensing elements, so there is no power needed for this purpose. The inefficiency of the sensing elements will be reflected in need to have extra amplification and, perhaps, additional signal to noise discrimination and signal filtering. Assuming that appropriate filtering and multiplexing is done, we will only have ~100 recording channels at a given time with 10kHz bandwidth each (sufficient to record any physiological signals), the best solution for total chain of amplification [4,24] and domain-specific analog-to-digital converter (ADC) [5,6,12,15,27] is expected to fall into the range of μW to nW.

**Signal Processing:** to reduce the power consumption needed for the communications to the outside, some data processing should be done before. A low power 32-bit processing core in this work having flexible and on-chip memory architecture can perform a range of DSP (digital signal processing) instructions for the implantable devices. In this architecture, the processor clock frequency may be in the 10–100 kHz range, thus enabling frequency and voltage scaling into subthreshold and near threshold voltages [7]–[11].

**Communication:** support the connectivity standards and communication protocols, approved by the Federal Communications Commission (FCC) has recently allocated 402–405 MHz medical implant communication service (MICS) RF band [17], characterised by capability of achieving 100’s of Kb/sec data transfer rates at a range of around 2m. This eliminates the need for outside controller to be in close vicinity as in the case of inductive links. MICS facilitates the higher data rates, as required to upload patient events captured in the IMD’s memory to the base station for analysis and gives improved measurements and control in different IMD applications especially cardiac and neural applications.

**Stimulation electronics:** defines the output or response of the implanted device, as decided by the signal processor. This function module includes several channels of stimulation, multiplexers, and DAC’s and pulse generators. The power consumption of this circuitry can be estimated by equaling it to the value needed for sensing signal acquisition and processing. The stimulation levels depend on the tissue type and stimulation spot size and varies from 1mA@2V for DBS to 2.5mA@4V for cochlear [4,7, 31, 32].

**C. Performance budgets**

A complete analysis of the best electronics architecture will require optimized design and testing of the components, and we will only estimate here the possibilities provided by modern silicon (Si) technologies in integration of such system.

### III. PROPOSED SYSTEM ARCHITECTURE

It is expected that future IMD systems will have to be smarter, easier to place and operate as well as be MRI safe [8]. The proposed system architecture is shown in Fig. 3. These are interconnected by a shared system bus, where 32-bit CPU, direct memory access (DMA), and ADC interface have the ability to initiate a memory transaction, while all the other peripherals can only receive a transaction. The control of the AFE output is often derived from the analysis of the incoming data digitized by an ADC and read by the processor. In addition, a processor unit may also have a companion DSP that allows for more detailed analysis of the incoming sensed data. An application specific Intellectual Property (IP), or any intelligent circuit techniques [26,32], can also be integrated in this architecture platform easily.

This section describes the top-level design aspects of the system architecture. An orthogonal strategy to maximize energy efficiency is the use of dedicated hardware blocks [9,18,20,30,34] to efficiently support computationally-intensive segments of applications.

#### A. Architectural Description

From a functional point of view, this system consists of one or two multi-layer AHB sections, connected to each other in a transparent way using a cascad, and lower-speed VPB busses for interfacing of the peripherals. The proposed system architecture has a multi-layer AHB bus, with at least one 32-bit CPU, and external or internal memories. More multi-layer AHB’s are required in case another bus-master such as dedicated DSP processor for high computations is required, which is not covered in this work.

This architecture implemented in 65 nm technology, however, can be scaled into any other process easily.

#### B. Bus technology

Each multi-layer AHB section offers full point-to-point connections of all masters to all slaves, supporting zero-waitstate operation. In this way, a very high bandwidth can be achieved. This structure has several features: i) High bandwidth by allowing multiple parallel accesses, ii) Reduced access latency by removing ‘bus request’ pipeline stage, iii) Reduced power as each master has a private connection to each slave at the cost of 10% extra chip-size than ‘regular’ AHB, keeping the same operating speed as ‘regular’ AHB.

![Fig. 3. Generic System Architecture and Functional Modules for Implantable Medical Device](image-url)
Each of these sections are then cross-connected using AHB cascaders. The AHB cascaders operate as a transparent bridge between two AHB section. All masters in all sections can access all slaves in all sections using a unified memory map across the cascaders.

C. CPU and DMA Engine

A 32-bit ARM CPU is the heart of this system architecture. These ARM processors are well suited for ULP applications, such as IMD devices. This system architecture offers direct support for many debugs through the ARM JTAG Multi-ICE protocol as well as Embedded Trace.

Optionally, this SoC supports the use of a centric DMA engine, which offers 8 fully programmable channels, and two fully independent master interfaces on the multi-layer AHB bus.

D. Memories

The main usage for internal SRAM/ROM is for storing relatively small amounts of data, while still having fast access at low power consumption compared to off-chip memory. For typical IMD applications, the overall size of internal RAM and ROM can be around 25% of the chip area (including CPU caches). The amount of internal RAM/ROM is therefore a main cost-driver of the total SoC price. Simulation model of 64 KB SRAM is used in this work, which is easily extendable.

IV. Power Management

Proposed Power management is shown in Fig. 4 with conditions explained in Table 1. It has impact on the hardware as well as on the software architecture of SoC, both implementing an infrastructure for energy management. A trend continues towards Dynamic Power Management (DPM), where hardware technologies for frequency scaling, and voltage scaling are being introduced to reduce the power consumption at run-time. However, crucial to the success of this approach is a presence of intelligent software with operating modes, which adjusts the system performance level to maximize energy savings while still meeting application real-time deadlines.

A. Programmable voltage supply configurations

Because the system architecture has different voltage supply domains, which are actually separate, this system architecture supports advanced programmable voltage supply configurations in which a user can choose these advanced voltage supply configurations at system level in accordance with specific functional needs.

It is possible to feed only the needed components and, as a consequence, to reduce power consumption power leakage due to voltage supplies. In particular, switching off unneeded I/O pads makes it possible to cut down power consumption, enabling/disabling different modules to reduce leakage power.

B. Start-up Modes

As shown in Fig. 4, the state-machine allows a controlled start-up of this SoC, and remains in the start-up modes until the processor configures the state-machine with its application specific properties by entering normal mode. As the start-up mode this architecture distinguishes between a cold-start and warm-start.

The system starts up from the cold-start mode when the 32-bit CPU needs to be initialized. The system registers receive the default configuration.

The system starts up from the warm-start when the 32-bit CPU was supplied, but a fall-back mechanism caused a reset to restart the processor.

C. Operation Modes

The system can be programmed into one of the three basic operation modes:

![Fig. 4. State Diagram for Power Management in proposed architecture](image-url)
Normal mode: The system operating in the cold-start or warm-start mode has to be initialized by the processor via entering the normal mode. The normal mode is the standard and full operation mode. The transceiver is active for transmitting and receiving of transceiver messages. The processor is working and is monitored by the watchdog. The watchdog expects a trigger within the defined trigger window. A missing or wrong trigger results in a reset. The local input ports are sensed continuously and detected edges can launch an interrupt.

Standby mode: The system can save power in standby. The processor is still supplied, but other parts can be on HOLD. The watchdog may be triggered, and the watchdog time-out results in a cyclic wake-up of the CPU. The communication transceiver is in auto-standby. The local input ports monitoring occurs by continuously or cyclic sensing. The wake-up response to the CPU is either as interrupt or reset with a fall back to warm-start.

Sleep: In sleep mode the system achieves the maximum power saving. The transceiver is in auto-standby. The local input ports monitoring occurs by continuously or cyclic sensing. The wake-up response to the CPU is always as reset with a fall back to cold-start.

D. Fail-safe Operation

During severe fault situations the system minimizes the power consumption. System malfunctions leading to fail-safe are:

- the system fails to initialize, in this case the system hasn’t left cold-start when the watchdog init period expires for the second time. The system falls back to fail-safe when the transceiver bus is quiet and the transceiver switches to off-line. If activity on the transceiver bus is detected or a transition on the local input ports is detected the system enters cold-start again to give the CPU a new chance to start-up.
- the die temperature exceeds the over-temperature protection level that guards the system against unrecoverable damage. The temperature protection is released when the temperature has dropped below the over-temperature warning level. The system enters cold-start to restart the CPU.

E. Power Analysis

Since the goal of the experiments was to evaluate the effect on energy consumption of proposed design, the amount of energy spent had to be measured. Data collection for this measurement is done with LabVIEW, which measures the instantaneous current and voltage of the SoC.

The measurements are based on a neural and cochlear signal being input to the system, after which the target system remains idle for 5 seconds. Just before the processing starts, the neural application sends a trigger to start the LabVIEW measurement as shown in Fig. 5.

The LabVIEW measurement then runs for a fixed duration of 250 seconds. As can be seen from the power consumption plotted in Fig. 6 and Fig. 7. The start, and especially the ending of the application does not occur at a fixed time position (for different frequencies of the SoC). In order to find the start and end times of power consumption for neural signals, the first and last peak of power consumption in the measurement is searched. The energy is than calculated from the detected start to end times, by integrating instantaneous power between the found start end and times. The estimated error introduced by this energy calculation method is less then 2%.

![Fig. 5. Application Prototype setup](image1)

![Fig. 6. Application startup Variation](image2)

![Fig. 6. Application end Variation](image3)
V. CONCLUSION

Ultra-low-power is critical in implementing signal processing algorithms for IMDs and requires optimization in all stages including architecture, circuit design, and process selection. The proposed architecture provides a good framework for supporting implantable medical platform having intelligent dynamic power management. The framework has been implemented on a SoC equipped with required functions with power management simulation for typical startup and finish of the stimulation task. In this paper, a medical platform SoC is described with low power consumption. The concepts presented in this work can be extended to other medical and wireless sensor applications. Such an SoC platform could be used for mapping a variety of applications.

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REFERENCES


