Guest Editorial for the Special Section on Emerging Computational Paradigms

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Multicore and many core embedded architectures are emerging as computational platforms in many application domains ranging for high performance computing to deeply embedded systems. The new generations of parallel systems, both homogeneous and heterogeneous that are developed on top of these architectures represent what is called the emerging computing continuum paradigm. A successful evolution of this paradigm is however imposing various challenges from both an architectural and a programming point of view. The design of embedded multicore/manycores requires innovative hardware specification and modeling strategies, as well as low power simulation, analysis and testing. New synthesis approaches, possibly including reliability and variability compensation, are key issues in the coming technology nodes. Furthermore, thermal aware design is mandatory to manage power density issues. The design of effective interconnection networks is a key enabling technology in a many-core paradigm. New solutions such as photonics and RF NoCs architectures are emerging solutions on this regard. At the same time, these new interconnection systems have to be compliant with innovative 3D VLSI packaging technologies involving vertical interconnections in 3D and stacked ICs. These design solutions enable the integration of more and more IPs, resulting in heterogeneous platform where reconfigurable components, multi-DSP engines and GPUs collaborate to provide the target performance and energy requirements. Along with design and architectural innovations, many challenges have to be faced to enable an effective programming environment to many core systems. These challenges call from innovative solutions at the various levels of the programming toolchain, including compilers, programming models, runtime management and operating systems aspects. Holistic and cross-layer programming approaches have to be targeted considering not only performance, but also energy, dependability and real-time requirements. Finally, on the application side, multicore/manycore embedded systems are pushing developments in various domains such as biomedical, health care, internet of things, smart mobility, and aviation.

This special section includes seven articles focusing on memory-based computing and 3D stacked hybrid memory architectures, on many-core neuromorphic platforms and clustered many-core accelerators, on emerging technologies for on-chip interconnects and signal reconstruction algorithms running on a heterogeneous mobile SoC and on the efficient parallelization of GPU primitives.

In particular, the first article, “Approximate Computing using Multiple-Access Single-Charge Associative Memory”, proposes a new Multiple-Access Single-Charge (MASC) TCAM architecture which is capable of searching TCAM contents multiple times with only a single pre-charge cycle.

The second article, “Optimizing Network Traffic for Spiking Neural Network Simulations on Densely Interconnected Many-Core Neuromorphic Platforms”, describes a new Partitioning and Placement methodology able to maps Spiking Neural Network on parallel neuromorphic platforms. This methodology improves scalability/reliability of Spiking Neural Network (SNN) simulations on many-core and densely interconnected platforms.

The third article, “Runtime Support for Multiple Offload-Based Programming Models on Clustered Manycore Accelerators”, presents a runtime system for a cluster-based manycore accelerator, optimized for the concurrent execution of offloaded computation kernels from different programming models.

The fourth one, “Towards Maximum Energy Efficiency in Nanophotonic Interconnects with Thermal-Aware On-Chip Laser Tuning” proposes to jointly tune the on-chip lasers and MRs in order to align the wavelengths of the emitted signals with the resonant wavelengths of the MRs. This method allows significant improvements of the power consumption with regard to the related methods, while meeting the BER requirement.

The fifth article, “Network-on-Chip Multicast Architectures Using Hybrid Wire and Surface-Wave Interconnects”, addresses the system level challenges for intra-chip multicast communication in a proposed hybrid interconnects architecture. This hybrid NoC combines and utilizes both regular metal on-chip interconnects and new type of wireless-NoC (WiNoC) which is Zenneck surface wave interconnects (SWI).

The sixth article, “Energy-Aware Bio-signal Compressed Sensing Reconstruction on the WBSN-gateway”, evaluates the energy cost and real-time reconstruction feasibility on the
WBSN gateway, considering different signal reconstruction algorithms running on a heterogeneous mobile SoC.

Finally, the seventh article, “Pro++: A Profiling Framework for Primitive-based GPU Programming”, presents a profiling framework for GPU primitives that allows measuring the implementation quality of a given primitive by considering the target architecture characteristics. The framework collects the information provided by a standard GPU profiler and combines them into optimization criteria. The criteria evaluations are weighed to distinguish the impact of each optimization on the overall quality of the primitive implementation.

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