Received 12 July 2019; revised 18 August 2019; accepted 28 August 2019. Date of publication 18 September 2019; date of current version 30 September 2019.
The review of this article was arranged by Editor N. Collaert.

Digital Object Identifier 10.1109/JEDS.2019.2940606

Self-Limited Low-Temperature Trimming and Fully Silicided S/D for Vertically Stacked Cantilever Gate-All-Around Poly-Si Junctionless Nanosheet Transistors

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This work was supported in part by the Ministry of Science and Technology, Taiwan, under Project MOST106-2221-E-009-151-MY3 and Project MOST-107-2633-E-009-003, and in part by the Taiwan Semiconductor Research Institute under Project JDP107-Y1-036.

ABSTRACT A self-limited low-temperature trimming process is demonstrated without surface morphology degradation. It shows great potential to control the trimming process with a large process window (400–900 s). Subthreshold characteristics are improved and I_{off} is drastically reduced (~two orders of magnitude) with increasing trimming cycles. Full silicidation on the source/drain (FUSI-S/D) is performed to improve I_{on}. Surprisingly, after silicidation, both I_{on} and μ_{FE} shows degradation despite that the series resistance is improved. An ultrathin body junctionless (UTB-JL) device is fabricated to investigate the degradation cause by direct CV measurement on the device, which can give us an insight into the details of the change with the silicidation.

INDEX TERMS Self-Limit, low-temperature trimming, fully silicided-S/D, vertically stacked, poly-Si, junctionless, nanosheet, monolithic 3D-ICs.

I. INTRODUCTION

Development of "More-than-Moore" systems has highlighted a new aspect of multifunctional device integration by monolithic 3D integrated circuits (M3D-ICs). Many studies have shown its feasibility by using poly-Si to realize functional M3D-ICs, owing to its CMOS process compatibility, maturity, fabrication simplicity, low cost, and low processing temperature [1]–[3]. Different functionalities require different driving currents. Conventional lateral multi-channels offer different effective widths for current tuning; however, they also occupy a greater wafer footprint, which is not suitable for scaling. Vertically stacked channels offer the possibility of adjusting driving current within the same footprint while maintaining subthreshold performance [4]–[6].

Junctionless (JL) transistors have uniform doping profile throughout the source–channel–drain [7]. The absence of a p/n junction makes it less sensitive to thermal budget, which is suitable for M3D-ICs [8]. A JL device has to be turned off by depleting the channel carriers. As a result, the channel dimension has to be smaller than the maximum depletion width of the associated doping concentration (~11 nm with $N_D = 1\times10^{19}$ cm^{-3}). In order to trim down the channel dimension to the full-depletion region and to improve gate controllability, Tezuka *et al.* [9] used H_2 thermal etching to scale down the nanowire, and Chen *et al.* [10] used thermal oxidation to trim down the top/bottom nanosheets. However, both methods require a high-temperature process (>900 °C), which may not meet the requirements for low temperature of M3D-ICs. Yeh *et al.* [11] proposed a trench structure fabricated by dry etching to trim down the channel. However, this may cause plasma damage to the channel and the interface. Previously, our group have proposed the use of heated-phosphoric-acid (HPA-140 °C) [12] and standard ammonium hydroxide acid solution (SC1-75 °C) [8] to trim down the channel. Both methods show the advantages of batch processing,

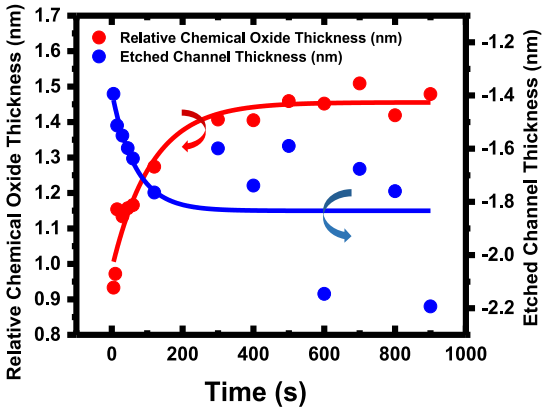

FIGURE 1. **Relative chemical oxide thickness and etched channel thickness measured by an ellipsometer showing the self-limiting property.**

low temperature, and near-atomic-scale etching, however, the etching rate is not linear and the surface morphology will slightly change after trimming. In this work, we will use a new approach involving growing a self-limited chemical oxide and etching by selective buffered oxide etching solution (BOE) as cyclic trimming.

We have found that series resistance is increased with each trimming cycle which is caused by the current crowding effect and spreading resistance, since the current is passing through a thin channel. Fully silicided Source/Drain (FUSI-S/D) process is adopted to compensate the effect. Note that the FUSI-S/D can also solve the vertical series resistance problem pointed out in our previous work [13]. Though silicidation is a widely used technology in VLSI fabrication, to our knowledge, there have been few studies addressing its effectiveness when used with JL devices. In this paper, we will discuss how the silicidation compensates the series resistance and its side effects with high-k metal gate stack.

The following section of this paper is divided into three parts (A, B, and C). In part A, the self-limited chemical oxidation process and its impact on channel surface morphology are presented. In part B, JL devices with different trimming cycles are compared. In part C, the effects of silicidation on device electrical characteristics are discussed. Capacitance-Voltage (CV) analysis was also shown in this section. Finally, the conclusion is given with an overview of the results.

II. RESULTS AND DISCUSSION

A. SELF-LIMITED LOW-TEMPERATURE TRIMMING PROCESS

Diluted H_2O_2 (31%) was heated up to 75 °C, and the samples were immersed in the solution for different periods of time to grow a layer of chemical oxide consuming the channel. The measured chemical oxide thickness and the etched-off in situ phosphorus doped poly-Si channel thickness are shown in Fig. 1. We can clearly see the self-limiting property with longer immersion time. It shows the potential to control

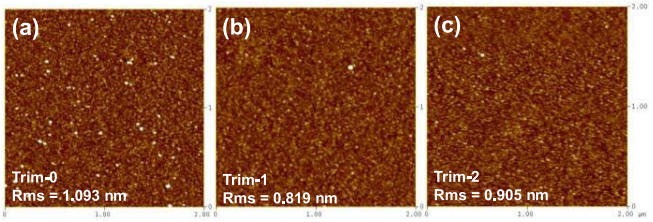

FIGURE 2. **Surface roughness measured by atomic force microscopy (AFM) showing no surface morphology degradation between (a) Trim-0, (b) Trim-1, and (c) Trim-2.**

the trimming process with a large process window (400–900 s). Surface roughness is a crucial factor for nano-scale device. The surface morphology of different trimming cycles, Trim-0 (as the deposited channel film), Trim-1 (1 cycle), and Trim-2 (2 cycles) are presented in Fig. 2. It can be seen that the self-limited trimming process does not change the surface roughness, and root-mean-square roughness is controlled within 1 nm.

B. DEPENDENCE OF TRIMMING CYCLES ON DEVICE PERFORMANCE

In this part, devices with different trimming cycles are compared. The main device fabrication flow is listed in Fig. 3(a). Fig. 3(b-f) are the cross-sections at the green arrow in Fig. 3(g) with different fabrication step. After wet oxidation and SiN_x etching stop layer (ESL) deposition, series of films with space-oxide (TEOS, 40 nm)/in situ doped-poly (DP) channel (10 nm)/oxide-hard mask (TEOS, 50 nm) were deposited. Then a dummy region was deposited and patterned. Spacer hard mask was formed by conformal TEOS oxide deposition and anisotropic dry etching [Fig. 3(b)]. After the dummy region was selectively removed [Fig. 3(c)], channel patterning was carried out by dry etching, followed by wet surface cleaning and DP raised source/drain (S/D) deposition [Fig. 3(d, e)]. S/D patterning was conducted by selective dry etching. While S/D pads were protected by photoresist, channels were protected by the oxide hard mask above, and the cross-section became as Fig. 3(d) again. Channels were then suspended by selective wet etching (BOE solution). Cyclic self-limited low-temperature trimming process with diluted (31%) H_2O_2 (75 °C) chemical oxide growth for 600 s and BOE selective etching off the grown chemical oxide was then performed at this stage. Note that after each trimming cycle, there was no chemical oxide on the channel. After various cycles, an additional chemical oxide was grown with the same condition as interfacial layer (IL), followed by 2.5/4.5 nm of AlO_x/HfO_x deposition by ALD system and PDA with 500°C, 60 s in N_2 ambient. An ALD-TiN was firstly deposited with 60 cycles (~3.8 nm) to fully surround the nanosheet in order to realize gate-all-around (GAA) electrostatic control, then a thicker PVD-TiN (~50 nm) was deposited and patterned as gate electrode [Fig. 3(f)]. An interlayer dielectric was deposited and contact holes were opened by BOE for electrical measurement. Device with

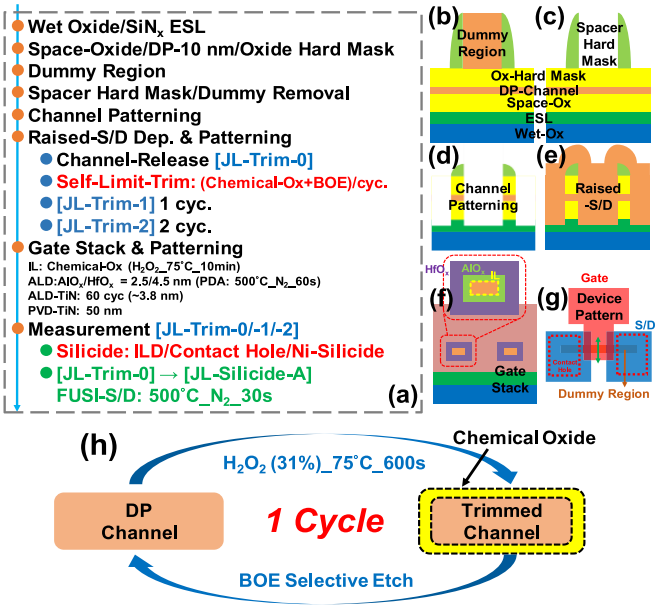

FIGURE 3. **(a) Main process flow of device fabrication. The control device (without trimming) and device with different trimming cycles are denoted as Trim-0, Trim-1, and Trim-2. After first electrical measurement, Trim-0 was sent to silicidation and became Silicide-A. (b-f) Are the cross-sections at the green arrow in the top view pattern (g). Details of the cyclic trimming process is depicted in (h). Note that after each cycle, there are no chemical oxide on the DP channel.**

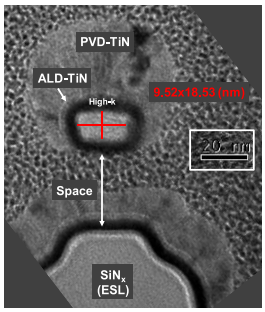

FIGURE 4. **TEM image of JL Trim-1 channel cross-section. Dimension of the channel is around (Left) 9.52 x 18.53 (nm). ALD-TiN did not fully surround the bottom of the channel, which may cause the rather high subthreshold swing.**

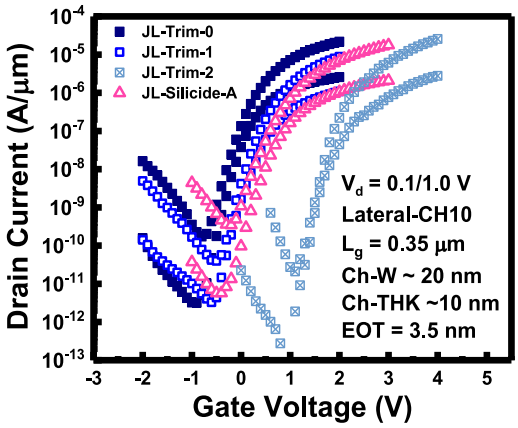

FIGURE 5. **Transfer (I_d-V_g) characteristics of different devices. The bias condition and various factors are listed in the picture. Threshold voltage positive shift and I_{off} (I_{min}) reduction can be observed. I_d is normalized to effective width (W_{eff}).**

as deposited channel thickness is denoted as Trim-0, and devices underwent 1 and 2 cycles of trimming are denoted as Trim-1 and Trim-2. After the first electrical measurement, Ni lift-off and silicidation(500°C_N_2_30s) were conducted to form FUSI-S/D.

The annealing condition was confirmed to fully silicide the S/D by EDS line scan (not shown). Tirm-0 then went through a second electrical measurement and the data is denoted as Silicide-A. Comparison between Trim-0 and Silicide-A will be discussed in the next part. Finally, the top view of the device pattern is shown in Fig. 3(g). TEM image of the cross-section of the JL Trim-1 channel is shown in Fig. 4. We found that the ALD-TiN did not fully surround the channel as we intended, which may cause the rather high drain-induced barrier lowering (DIBL) and subthreshold swing (S.S.) value shown later. Variation were also observed with the channel dimension within the same condition (Trim-1), in order to minimize its effect to electrical characteristics, device with 10 lateral channels were used throughout the paper.

The transfer characteristics are shown in Fig. 5. It is obvious that the threshold voltage is positively shift and I_{off} is reduced with channel trimming. Note that the thickness/width of the junctionless device will affect the I_{on}, I_{off}, and subthreshold performance, and I_d is normalized with effective width (W_{eff}) [14], [15]. As the channel is scaled down, less surface potential is needed to fully deplete the channel, that is, less negative gate voltage from flat band voltage is required for depletion width reaching the channel thickness. Therefore, V_{th} will positively shift as shown in Fig. 6(a). At the same time, the improved gate controllability will reduce subthreshold swing (S.S.) [Fig. 6(b)]. DIBL, however, shows no improvement as indicated in Fig. 6(c). It is thought to be a transient effect during measurement. As shown in Fig. 5, we started the gate voltage sweep from a value that gate-induced drain leakage (GIDL) is observed. Due to the depletion operation of JL device, high transverse electric field occurred at the off-state, hole trapping in high-k will occur at this stage and cause negative V_{th} shift with the next measurement. As a result, DIBL is independent with trimming cycle. I_{on} gradually decreases with trimming cycle as expected [Fig. 6(e)]. As the channel is trimmed down, the channel resistance rises and reduces the on-state current. Meanwhile, we discovered that the extracted series resistance by Campbell *et al.* method [16] increases with each trimming cycles, which is ascribed to the current crowding effect and spreading resistance adding up to the overall R_{sd}. These effects will further lower the I_{on}. I_{off}, on the other hand, is drastically reduced by two orders of magnitude owing to the improved gate controllability, and it dominates the overall on/off current ratio [Fig. 6(f, g)]. It is expected that I_{off} and S.S. will further improve as thicker ALD-TiN is used to

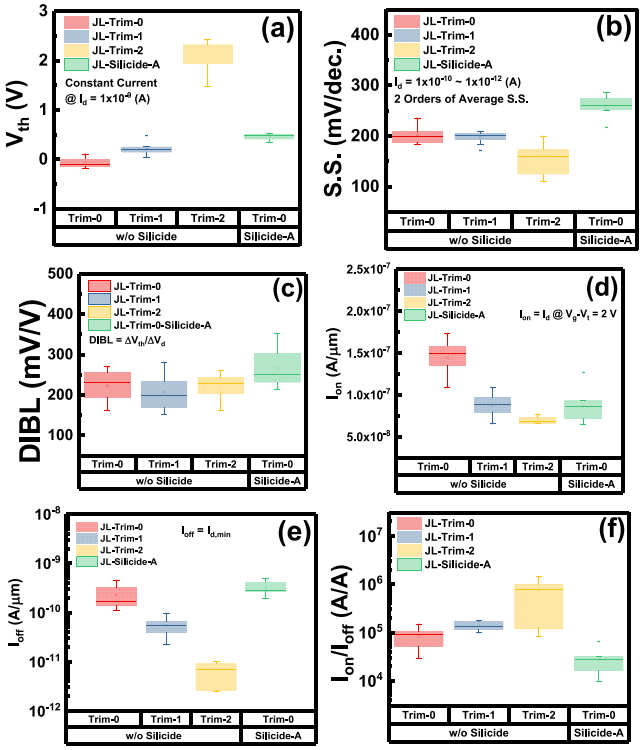

FIGURE 6. (a) Threshold voltage comparison. Large threshold voltage shift suggested that the channel is doped with high concentration. (b) Subthreshold Swing (S.S.) is improved as channel trimmed down, however, for Silicide-A, degradation is observed. It is inferred that the stress induced by TiN during thermal annealing will cause interface state generation. (c) Drain-induced barrier lowering (DIBL) shows no change. (d) I_{on} decreases with channel trimming. Surprisingly, after silicidation, I_{on} of Silicide-A is lower than Trim-0. (e) I_{off} reduced 2 orders of magnitude with 2 cycles of trimming thanks to the improved gate controllability. (f) Overall I_{on}/I_{off} ratio show improvement with trimming.

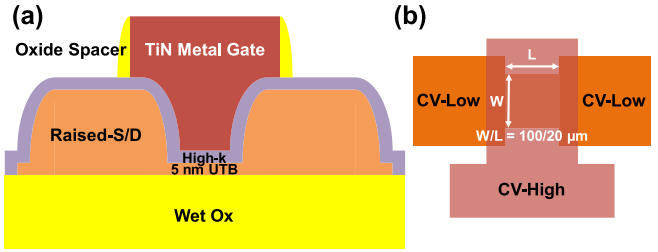

FIGURE 7. (a) Cross-section of the UTB planar poly-Si JL device. (b) Top view of the device structure. For CV measurement, voltage high and voltage low are connected to metal gate and S/D respectively.

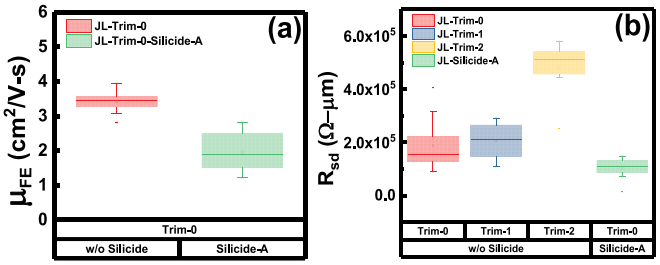

FIGURE 8. (a) Field-effect mobility of Trim-0 and Silicide-A. The latter shows decreased mobility, due to the degraded interface after silicidation/PMA. (b) R_{sd} extracted by Campbell method [ref]. Spreading resistance adds up to R_{sd} as channel scaled, which can be compensated by the FUSI S/D.

truly surround the nanosheet channel. Nevertheless, the benefits of low-temperature cyclic trimming process with device performance are shown.

C. SILICIDATION

Full silicidation (FUSI) technology was formerly proposed to improve the sheet resistance of a gate line and reduce the equivalent oxide thickness by eliminating the poly depletion effect [17]. It also has the advantage of process integration simplicity [18]. Here, we adopt this technology for raised-S/D.

In order to support and analyze the changes after silicidation, an additional device, a 5 nm thick ultrathin body (UTB) planar poly-Si JL device with Width/Length 100/20 (μm), was made and measured for its Gate-Channel/Source/Drain CV characteristics. Note that 5 nm was chosen due to single gate structure of UTB. If we considered 10 nm nanosheet as double gate structure, each side of the gate controls 5 nm of channel. Device structure and measurement setup are shown in Fig. 7(a, b). The cyclic trimming process for trimming down the channel to 5 nm and high-k/metal gate stack, including IL/AlO_x/HfO_x/PDA/TiN, of UTB JL device were all the same as samples Trim-0/-1/-2. The final UTB device before and after silicidation will be denoted as UTB-Trim-0 (5 nm channel, before silicidation), and UTB-Silicide-A respectively. Channel doping concentration (N_d) and flat-band voltage (V_{fb}) were calculated by iteration. Average interface state density was derived from conductance method with the V_g range aligned to the range S.S. was extracted. Details of the calculation will not be mentioned here.

From Fig. 6(a-c), we can see that V_{th} of Silicide-A is positively shifted with 0.53 V from Trim-0, which is due to a combination of doping concentration change, interface degradation, and flat-band voltage shift. Channel doping concentration is slightly higher might due to further dopant activation. S.S. and DIBL are both degraded for Silicide-A in Fig. 6(b, c) suggesting that the gate controllability is degraded by higher doping concentration and generated interface states after silicidation. Silicidation serves as a post-metal annealing (PMA) for the high-k gate dielectric. The stress induced by the PVD-TiN gate electrode during PMA deteriorates the channel/high-k interface. D_{it} of UTB-Trim-0 and UTB-Silicide-A shown in the inset table of Fig. 9 suggests the same. As shown in Fig. 9, after silicidation, CV curve shows two slopes in the depletion region, the second slope further away from the V_{fb} is contributed by the generated interface states as we used to call a "hump" or "pack". Field-effect mobility of the nanosheet device is also degraded with Silicide-A in Fig. 8(a) compared

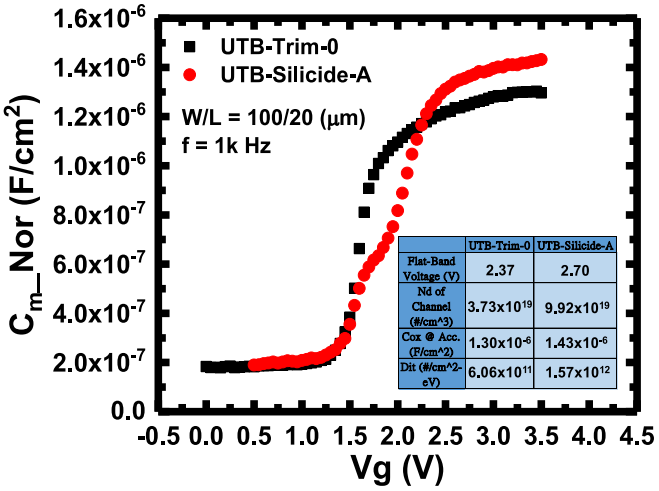

FIGURE 9. Measured normalized CV curve (C_m_Nor) for UTB-Trim-0 and UTB-Silicide-A. Flat-band voltage (V_{fb}), channel doping concentration (N_d), C_{ox} at accumulation, and interface state density (D_{it}) are listed in the inset table.

to Trim-0. The carriers of JL device conduct via bulk transport and its mobility is thought to be less affected by surface scattering, however, the channel thickness is somewhat thin (∼10 nm), and therefore, the interface scattering cannot be ignored. As a result, even though the series resistance (R_{sd}) is reduced with Silicide-A [Fig. 8(b)], the I_{on} is still degraded compared to Trim-0 [Fig. 6(d)]. Nevertheless, FUSI-S/D can improve the current increment problem pointed out in previous work [13] and compensate the increased R_{sd} as channel scaled.

III. CONCLUSION

A self-limited low-temperature trimming process was demonstrated with the advantage of large processing window (400 ∼ 900 s). Vertically stacked poly-Si JL nanosheet transistors showed improved subthreshold swing and I_{off} with trimmed channels owing to the improved gate controllability. Nearly 2 orders of magnitude I_{off} reduction is reached. The FUSI-S/D could effectively compensate for the current crowding effect and spreading resistance resulting from channel trimming and is thought to be able to solve the current increment limit for vertically stacked nsnosheet device. Extensive CV analysis through the UTB device further confirm the degradation of the interface by silicidation thermal process (PMA) which needs further investigation for its suppression. Overall, the developed process is suitable for low temperature required M3D-IC applications.

ACKNOWLEDGMENT

The authors like to thank Uni-edit (www.uni-edit.net) for editing and proofreading this manuscript.

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