Abnormal Bias-Temperature Stress and Thermal Instability of $\beta$-Ga$_2$O$_3$ Nanomembrane Field-Effect Transistor

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ABSTRACT In this paper, we report on the electrical and thermal instability of $\beta$-Ga$_2$O$_3$ nanomembrane field-effect transistor with a bottom-gate configuration. The fabricated device exhibits high electrical performance of field-effect mobility of up to 60.9 cm$^2$/V·s, on/off-current ratio of $10^9$, and subthreshold slope of 210 mV/dec. However, we observe abnormal positive threshold voltage ($V_{TH}$) shifts under negative bias-temperature stress at an elevated operating temperature of 80 °C as well as under temperature-dependent transfer characteristics up to 200 °C. This abnormal instability is significantly influenced by the surface depletion effect, and is discussed using energy band diagram. The opposite $V_{TH}$ shift was achieved by applying atomic-layer deposited Al$_2$O$_3$ passivation layer.

INDEX TERMS $\beta$-Ga$_2$O$_3$, bias stress, stability.

I. INTRODUCTION

Beta-gallium oxide ($\beta$-Ga$_2$O$_3$), which has attracted great attention in recent years, exhibits superior electrical properties for next generation power electronics; Its ultra-wide bandgap estimated to be about 4.6 $\sim$ 4.9 eV allows high-temperature and high-voltage operation attributed to a large breakdown field ($E_{br}$) of up to 8 MV/cm [1]–[3]. Consequently, $\beta$-Ga$_2$O$_3$ possesses high Baliga’s figure-of-merit (FOM), which is commonly used for evaluating applicability of a material to power device performance, and the estimated FOM is several times higher than that of current viable solutions including silicon carbide (SiC) and gallium nitride (GaN) [3], [4]. In addition to these materials properties, cost-effective high quality Ga$_2$O$_3$ wafer from bulk single crystal obtained from melt-growth methods, such as Czochralski and edge-defined film-fed growth (EFG), provides a significant advantage over those wideband gap materials because SiC and GaN wafers require expensive high-pressure and -temperature synthesis [5]–[8]. Otherwise, a non-native substrate has to be adopted in sacrifice of epitaxial quality with various defects. Furthermore, in spite of its relatively lower saturation velocity, $\beta$-Ga$_2$O$_3$ of the very large $E_{br}$ exhibits a comparable Johnson figure-of-merit (FOM) intended for high-frequency operation [9], [10]. These unique properties have been facilitating intensive research efforts in the field of $\beta$-Ga$_2$O$_3$-based high-power and radio-frequency (RF) electronics [10]–[15].

In order to facilitate further researches in those fields, instead of an expensive epitaxy wafer, several works have been reported using a mechanical exfoliation method to utilize $\beta$-Ga$_2$O$_3$ thin-flake or nanomembrane, which is enabled by its monoclinic crystal structure; Relatively large lattice constant along [100] direction allows a simple cleavage into flakes or nanomembranes similar to two-dimensional layered materials [16]–[20]. Although the mechanical exfoliation method is not a scalable approach, it preserves high crystal quality of $\beta$-Ga$_2$O$_3$ and allows a simple device fabrication to investigate its electrical and material properties including device instability studied in this work; Instability under bias-temperature stress (BTS) conditions as well as elevated operating temperatures is crucial for power device applications.
In this paper, we fabricated bottom-gate unpassivated β-Ga2O3 FET from unintentionally n-doped (UID) bulk crystal substrate using a mechanical exfoliation method, and investigated its electrical and thermal instability under negative- and positive-BTS at an elevated operating temperature of 80 °C. We also studied thermal instability by characterizing temperature-dependent current-voltage (I-V) measurements up to 200 °C. Finally, by comparing with results of negative-BTS measurement in a vacuum condition as well as for a device with atomic-layer deposited Al2O3 passivation layer, we proposed a model and discussed the observed abnormal instability of the β-Ga2O3 FET based on energy band diagram.

II. EXPERIMENTS
Mechanically exfoliated β-Ga2O3 flakes from 15 mm x 10 mm (~201) surface β-Ga2O3 bulk substrate with unintentional n-type doping (UID) concentration of 4.8 x 10^17 cm^-3 (Tamura Corp., Japan) by a conventional scotch-tape method were transferred on to a heavily doped p-type Si substrate by setting the stress temperature (TSTR) at 80 °C. The total stress time (tSTR) was 10,000 sec, and we only interrupted the applied stress to measure the transfer characteristics. We also performed current-voltage (I-V) measurements at various operating temperatures up to 200 °C.

III. RESULTS AND DISCUSSION
Fig. 1(a) shows a schematic illustration of the fabricated β-Ga2O3 FET with bottom-gate configuration, and (b) its optical microscope image of the β-Ga2O3 FET with a channel thickness profile via AFM in the inset.

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II. EXPERIMENTS
Mechanically exfoliated β-Ga2O3 flakes from 15 mm x 10 mm (~201) surface β-Ga2O3 bulk substrate with unintentional n-type doping (UID) concentration of 4.8 x 10^17 cm^-3 (Tamura Corp., Japan) by a conventional scotch-tape method were transferred on to a heavily doped p-type Si substrate with thermally grown 300 nm SiO2 layer. Then source and drain (S/D) electrodes of Ti/Au (20/80 nm) were deposited by thermal evaporation and patterned using a conventional photolithography and lift-off process. Finally, the fabricated device was annealed at 450 °C in N2 for 10 min using a rapid thermal annealing to improve contact resistance. The device characterizations were performed with a semiconductor analyzer (HP 4145B) connected to a probe station with a temperature controlled vacuum chuck; a series of negative (VGS = −70 V) and positive (VGS = 0 V) BTS measurements were carried out under an accelerated stress condition by setting the stress temperature (TSTR) at 80 °C. The total stress time (tSTR) was 10,000 sec, and we only interrupted the applied stress to measure the transfer characteristics. We also performed current-voltage (I-V) measurements at various operating temperatures up to 200 °C.

![FIGURE 2. (a) Transfer characteristics (IDS-VGS) for VDS = 1 and 10 V, and (b) Output characteristics (I DS-VGS) for VGS = −80, −60, −40, −20, and 0 V, and for low VDS regime of 0 ~ 2.0 V in the inset. (c) Hysteric behaviors in an ambient and vacuum conditions at VDS = 1 V. (d) Extracted total resistance (RON), calculated channel (RCH) and contact resistance (RC) as a function of VGS − VTH.](image)

Hysteretic behaviors both in an ambient and a low vacuum (~1 mTorr) condition are compared in Fig. 2(c). The transfer curves were obtained by sweeping VGS from −100 V to 0 V (forward sweep) and then back to −100 V (backward sweep) while maintaining a constant VDS = 1 V. The amount of hysteresis (∆V) in the air and vacuum, which is calculated by the maximum voltage shift between the transfer curves in the forward and backward sweeps, were 2.34 V and 1.61 V, respectively, because of the reduced surface absorbates such as oxygens and water molecules in the vacuum. The interface trap density (∆Qit) responsible for the hysteresis can be
deduced from the amount of charges captured and released by the traps in the vacuum, which is given by \( \Delta Q_{\text{int}} = C_{\text{OX}} \times \Delta V \). In comparison to the \( \Delta Q_{\text{int}} \) of 1.15 x 10\(^{11} \) cm\(^{-2} \), \( \Delta Q_{\text{int}} \) in the air is estimated to 1.68 x 10\(^{11} \) cm\(^{-2} \), which is attributed to the additional surface absorbates induced charge (\( \Delta Q_{\text{srf}} \approx 0.53 \times 10^{11} \) cm\(^{-2} \)). The \( \Delta Q_{\text{srf}} \) results in less positive \( \Delta V_{\text{TH}} \) under negative bias-temperature stress as discussed in the following.

Fig. 2(d) presents extracted on-state resistance \( (R_{\text{ON}}) \) and channel resistance \( (R_{\text{CH}}) \) calculated from \( R_{\text{CH}} = L/\mu \text{FE} \cdot W \cdot C_{\text{OX}} \cdot (V_{\text{GS}} - V_{\text{TH}}) \) where \( W/L, C_{\text{OX}}, \mu \text{FE}, \) and \( V_{\text{TH}} \) from a linear region is also presented. Based on the extracted \( R_{\text{ON}} \approx 3.2 \) k\( \Omega \) mm and calculated \( R_{\text{CH}} \approx 1.3 \) k\( \Omega \) mm, contact resistance \( (R_{\text{C}}) \) of \( \approx 0.98 \) k\( \Omega \) mm was obtained from \( R_{\text{ON}} = R_{\text{CH}} + 2R_{\text{C}} \) at \( V_{\text{GS}} - V_{\text{TH}} = 22.4 \) V. The \( R_{\text{C}} \) is reduced to 60 \( \Omega \) mm, which is lower by more than one order of magnitude, at an elevated operating temperature of 200 °C due to enhanced thermionic emission across the Schottky barrier [22]. Although the low SS indicates that high quality interface between \( \beta\)-Ga\(_2\)O\(_3\) and SiO\(_2\) can be successfully formed without specific surface treatment, the Schottky contact-like large \( R_{\text{C}} \) needs to be further reduced for high performance \( \beta\)-Ga\(_2\)O\(_3\) FETs.

To evaluate thermal stability, we characterized the device for variable operating temperatures up to 200 °C, and Fig. 3 (a) shows the change of \( \Delta V_{\text{TH}}(V_{\text{DS}} - V_{\text{GS}}) \) curves. With the increasing operating temperature, \( \Delta V_{\text{TH}} \) increased by more than one order and the curves shifted toward a positive direction. The variations of extracted \( \mu \text{FE}, \text{SS}, \) and \( V_{\text{TH}} \) as a function of stress time \( (t_{\text{STR}}) \) are presented in Fig. 3 (b), 4(c), and 4(d), respectively. \( \mu \text{FE} \) decreased from 61.3 cm\(^2\)/Vs to 38.5 cm\(^2\)/V-s due to phonon scattering and current drifting by the surface absorbed oxygen and water molecules, and SS increased from 0.22 V/dec to 0.82 V/dec. As in most semiconductors, \( V_{\text{TH}} \) is supposed to shift toward a negative direction as the temperature increases due to thermally activated donor induced carriers in the channel. However, \( V_{\text{TH}} \) shifted toward positive direction by \( \Delta V_{\text{TH}} = 33 \) V. The observed abnormal positive \( \Delta V_{\text{TH}} \) of the \( \beta\)-Ga\(_2\)O\(_3\) FET might be attributed to the followings: thermal activation of oxygen vacancies in deep donor levels, which is expected to form a low concentration of vacancies, is mostly captured by the surface absorbed oxygen and water molecules, thermally created defects, and surface states [23].

In order to investigate electrical instability, we performed transfer characteristics measurements under positive and negative BTS (i.e., PBTS and NBTS) during the given stress time. We set \( t_{\text{STR}} = 80 \) °C as an accelerated stress condition, and placed the device on the heated vacuum chuck for several minutes to ensure thermal equilibrium prior to starting measurements. We only interrupted applied stress for the measurement at predetermined steps by sweeping \( V_{\text{GS}} \) at \( V_{\text{DS}} = 1 \) V, and extracted \( \Delta V_{\text{TH}} \) from \( \Delta V_{\text{TH}} = V_{\text{TH}} (t = t_{\text{STR}}) - V_{\text{TH}} (t = 0) \). Fig. 4(a) shows the shift of transfer curves under a constant bias stress \( V_{\text{GS}} = -70 \) V (\( V_{\text{GS}} - V_{\text{TH}} < 0 \)), and the off-current \( (I_{\text{OFF}}) \) increased by about two orders. Under NBTS condition, negative \( V_{\text{TH}} \) shift is typically observed due to released-charges from interface traps into the channel (i.e., net positive charged traps) [24], [25]. However, abnormal positive \( V_{\text{TH}} \) shift from \(-57.6 \) V to \(-32.9 \) V (i.e., \( \Delta V_{\text{TH}} = 24.7 \) V) was observed and plotted as a function of \( t_{\text{STR}} \) in Fig. 4(b). Fig. 4(c) shows positive \( V_{\text{TH}} \) shifts of transfer curves under a constant bias stress \( V_{\text{GS}} = 0 \) V (\( V_{\text{GS}} - V_{\text{TH}} > 0 \)). In Fig. 4(d), \( \Delta V_{\text{TH}} \) was 40.6 V even for \( 3 \times 10^3 \) sec and 54.5 V for \( 7 \times 10^3 \) sec which is not plotted in the Fig. 4(c). The observed abnormal \( V_{\text{TH}} \) shift of the \( \beta\)-Ga\(_2\)O\(_3\) FET is attributed to the predominant surface depletion effect of the unpassivated \( \beta\)-Ga\(_2\)O\(_3\) FET, which is...
reported to induce significant $V_{TH}$ variations depending on the channel thickness [20].

In order to corroborate the proposed model, we performed the NBTS measurements in the vacuum condition and for an ALD-$\text{Al}_2\text{O}_3$ passivated $\beta$-$\text{Ga}_2\text{O}_3$ FET. 20 nm of $\text{Al}_2\text{O}_3$ passivation layer was deposited on the finished device at 200 $^\circ$C. Fig. 5(a) presents $\Delta V_{TH}$ as a function of stress time. In the PBTS, charge trapping at the interface traps under a positive gate bias stress, captured charges in the channel by absorbed oxygens, and the surface depletion effect explained in Fig. 5(b) deplete charges in the channel and thus result in the largest positive $\Delta V_{TH}$ [25]. The amount of depleted charge concentration ($\Delta n$) after PBTS was estimated at $3.92 \times 10^{12}$ cm$^{-2}$. We calculated the charge concentration ($n$) using a parallel-capacitor model with $n = Q / e = C_{OX} (V_{GS} - V_{TH}) / e$. For the NBTS in the air, although released charges into the channel during the desorption process of oxygen and water molecules result in negative $\Delta V_{TH}$, the surface depletion effect exceeded the released charges from both surface absorbates and interface traps into $\beta$-$\text{Ga}_2\text{O}_3$ channel as schematically illustrated in Fig. 5 (c), and this is because the nanomembrane $\beta$-$\text{Ga}_2\text{O}_3$ has conceivable surface oxygen vacancy and defect states. The $\Delta n$ after NBTS was estimated at 1.78 x 10$^{12}$ cm$^{-2}$. However, in the low vacuum condition (i.e., less surface absorbates), $\Delta V_{TH}$ shifts toward more positive direction since the negative shift effect of the released charges from the oxygen and water molecules is reduced. From the NBTS measurement of a device with ALD-$\text{Al}_2\text{O}_3$ passivation layer, however, we obtained a reduced and opposite $\Delta V_{TH}$ of $-7.85$ V which is a conventional negative $V_{TH}$ shift under a negative gate bias. It is primarily because the surface states of $\beta$-$\text{Ga}_2\text{O}_3$ channel are passivated and reduced by the ALD-$\text{Al}_2\text{O}_3$ passivation process as presented in Fig. 5(d) [26]. The surface depletion effect due to dangling bonds and surface states significantly influence electrical and thermal stability of the $\beta$-$\text{Ga}_2\text{O}_3$ FET with bottom gate configuration, and the abnormal and large $\Delta V_{TH}$ can be mitigated and changed to a normal negative shift under NBTS through the ALD-$\text{Al}_2\text{O}_3$ surface passivation. Further experimental studies for $\beta$-$\text{Ga}_2\text{O}_3$ surface property and passivation are suggested to improve device stability.

IV. CONCLUSION

We have demonstrated high-performance $\beta$-$\text{Ga}_2\text{O}_3$ nanomembrane FET with $\mu_{FE} \sim 61$ cm$^2$/V·s, $I_{ON}/I_{OFF} \sim 10^9$, and $SS \sim 210$ mV/dec using the mechanical exfoliation method from UID bulk crystal substrate, and evaluated its electrical and thermal instability under BTS as well as variable operating temperatures up to 200 $^\circ$C. Whereas threshold voltage shift ($\Delta V_{TH}$) under positive BTS follows conventional $\Delta V_{TH}$ properties, abnormal positive $\Delta V_{TH}$ is observed under negative BTS as well as temperature-dependent transfer characteristics, which is attributed to significant surface depletion effects. Through the ALD-$\text{Al}_2\text{O}_3$ passivation layer on $\beta$-$\text{Ga}_2\text{O}_3$ surface, a negative $\Delta V_{TH}$ shift was achieved. High-quality passivation is suggested to ensure electrical performances of $\beta$-$\text{Ga}_2\text{O}_3$ FET under electrical and thermal stress conditions.

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REFERENCES


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