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A Novel Gate-Normal Tunneling Field-Effect Transistor With Dual-Metal Gate

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ABSTRACT In this combined experiment and simulation study we investigate a SiGe/Si based gate-normal tunneling field-effect transistor (TFET) with a pillar shaped contact to the tunneling junction which brings forth two significant advantages. The first, is improved electrostatics at the boundary of the tunneling junction which helps to diminish the influence of adverse tunneling paths, and thus, substantially sharpens the device turn on. The second, is a simplified fabrication of a dual-metal gate using a self-aligned process. We demonstrate the feasibility of the process and show the positive effect of a dual-metal gate in experiment. Overall the paper provides general guidelines for the improvement of the subthreshold swing in gate-normal TFETs which are not restrained to the material system.

INDEX TERMS Tunnel FET, dual-metal gate, gate-normal tunneling, work function tuning, field-induced quantum confinement.

I. INTRODUCTION

The study of tunneling field-effect transistors (TFETs) has been driven by the need for steep slope devices with the capability to be integrated in ultra-low power circuits [1]. The underlying idea is to reduce power consumption by supply voltage (V_{dd}) scaling (<0.3V). This can be achieved by using transistors with a subthreshold swing (SS) lower than 60 mV/dec that is the physical limit of MOSFETs, stemming from their operation principle based on thermal emission over a potential barrier. Physically, the operation of TFETs, based on band-to-band tunneling is fundamentally different from MOSFETs and not restrained to 60 mV/dec at 300K. Ideally a density of states (DOS) switch is realized, which refers to the condition that the current flow sets in abruptly, as soon as an energetic alignment of source valence band and channel conduction band (or vice versa) is achieved by applying a gate voltage. In an ideal semiconductor with sharp band edges and without non-idealities the increase of DOS around the band edge can reach many orders of magnitude within a few meV. Thus, theoretically the massive increase in available and empty states contributing to the tunneling current, when aligning the band edges, should make an increase of current by one order of magnitude possible with much less than 60 mV. However, experimentally it has been difficult to achieve according results. Therefore, a lot of research is focused on identifying the limiting issues. One major obstacle are traps. According to [2] the avoidance of bulk traps is crucial, even though there may exist device geometries which are more trap tolerant than others [3]. Moreover, the device geometry determines the abruptness of the turn-on even principally. Agarwal and Yablonovitch [4] have theoretically analyzed possible dimensional combinations at the tunneling junction, e.g., 1D/1D, 2D/2D or 2D/3D making use of abrupt changes in DOS. Gate-normal or line tunneling FETs ideally show a very sharp turn-on and on-currents scalable with the overlap area [5]–[9]. But there is always a competition between gate-normal tunneling and parasitic tunneling at edges [10], [11]. Counter doping inside the channel was proposed and has been proven to be beneficial in terms of SS and I_{on} in experiment [12]. On the

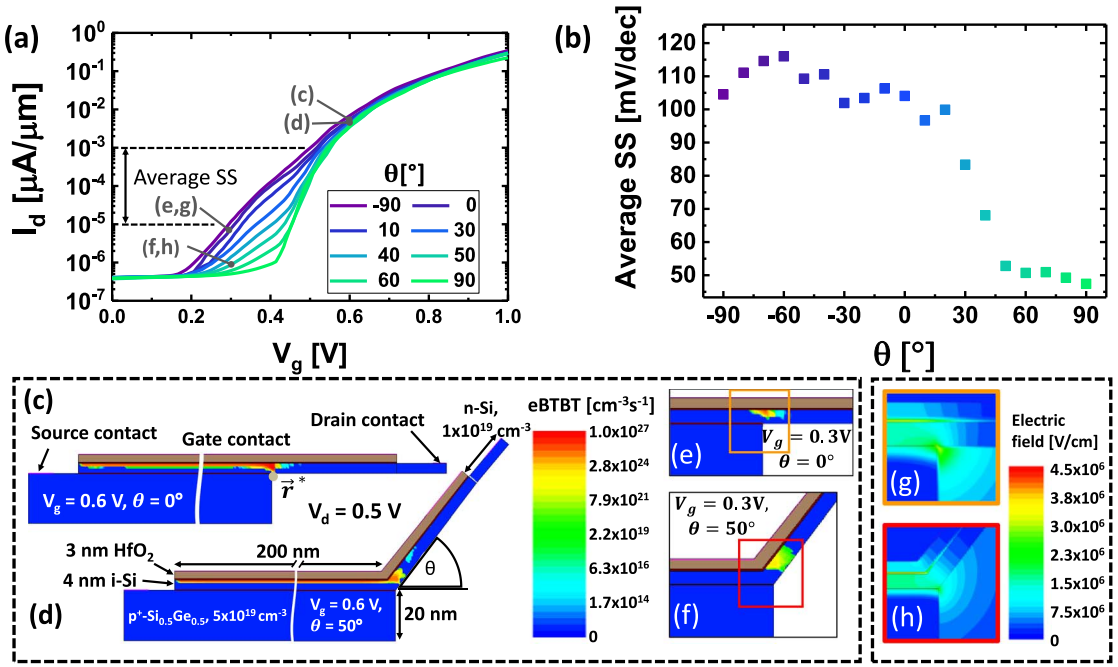

FIGURE 1. **(a) Simulated $I_d - V_g$-characteristics for different contact arm angles θ as defined in (d). By bending the contact arm upwards the unwanted tunneling generation at the right boundary of the SiGe-Source decreases, right-shifting the onset and thus uncovering the sharp turn-on stemming from gate-normal tunneling. Curves between $-90°$ and $0°$ do not vary from each other significantly and are thus not displayed. (b) The average SS between 10^{-5} μA/μm and 10^{-3} μA/μm greatly improves with increasing θ, especially between $20°$ and $50°$. (c,d) eBTBT contour plots for a simulated structure with $\theta = 0°$ and $\theta = 50°$ at $V_g = 0.6$ V, $V_d = 0.5$ V evincing that gate-normal tunneling dominates the on-state in the complete overlap region independent of θ. (e,f) Adverse eBTBT generation at the right SiGe boundary in the early subthreshold region ($V_g = 0.6$ V, $V_d = 0.5$ V). (g,h) Electric field corresponding to the eBTBT plots in (e,f) illustrating that the reduced electric field at the corner for increasing θ is the reason for smaller parasitic eBTBT generation. (Quantization neglected).**

other hand counter doping needs restrictions in order to avoid band-tails [13]–[15]. Another approach is the use of a dual-metal gate, which has been analyzed theoretically in many publications [16]–[20]. Though experimental feasibility is often considered [18], [21] for a possible fabrication of dual-metal TFETs, process requirements, like lithographic alignment precision of the gate to a few nm, are often very harsh. In this paper we elucidate a revised architecture for a gate-normal TFET employing a self-aligned fabrication process to create a dual-metal gate.

II. PRELIMINARY CONSIDERATIONS

We begin our considerations with a recapitulation of the basic gate-normal TFET architecture as described in [11], [22] shown in Fig. 1 (c) [dimensions and doping in Fig. 1(d)]. The source region which consists of boron-doped p^+-SiGe (in this example) is electrically contacted on the left. It is overlapped by a 4 nm thin i-Si channel and a high-k/metal gate, forming a vertical gate-normal tunneling junction in the overlap region. The channel and the gate extend over the right boundary of the SiGe region towards the n^+-Si drain. We will refer to this extension as the contact arm hereafter. It is commonly assumed that a buried oxide is placed below the horizontally extending contact arm [23]. For our first consideration we neglect the experimental feasibility and introduce the parameter θ which describes the angle between the contact arm and the horizontal. Using Sentaurus technology computer aided design (TCAD) we have analyzed the impact of θ on the electric field and parasitic tunneling at the position, where the contact arm and the right SiGe boundary meet. The behavior at this point has been shown to be very critical for the device performance [10], [11]. We employed the dynamic non-local path BTBT model from the TCAD Sentaurus environment [24]. The BTBT model constants were obtained from strained Si/SiGe band diagrams with adjusted effective density of states and effective masses calculated with a 30-level k.p-model [25]. Quantization is neglected for now, to underline that the effect is of electrostatic origin, but will be taken into account at a later stage [see Fig. 4(b)]. Fig. 1 (a) displays the simulated $I_d - V_g$ characteristics for $-90° < \theta < 90°$. Between $-90°$ (equivalent to the contact arm being bent vertically downwards) and $0°$ [Fig. 1(c)] the curves agree with each other quite decently. Between $0°$ and $50°$ the onset shifts to the right and significantly sharpens the turn-on. Above $70°$ no further changes are obvious. The drain-current I_d is independent of θ for $V_g > 0.6\ V$ and likewise is the on-current I_{on}. This independence from θ illustrates that I_{on} derives its value from the properties of the gate-normal tunneling junction and not from the geometry at the contacting point of the extension arm. This is further emphasized by the contour plot in Fig. 1(c,d), which clearly displays strong eBTBT generation along the complete overlap length below the gate at $V_g = 0.6\ V$. Contrary to that, the early subthreshold region

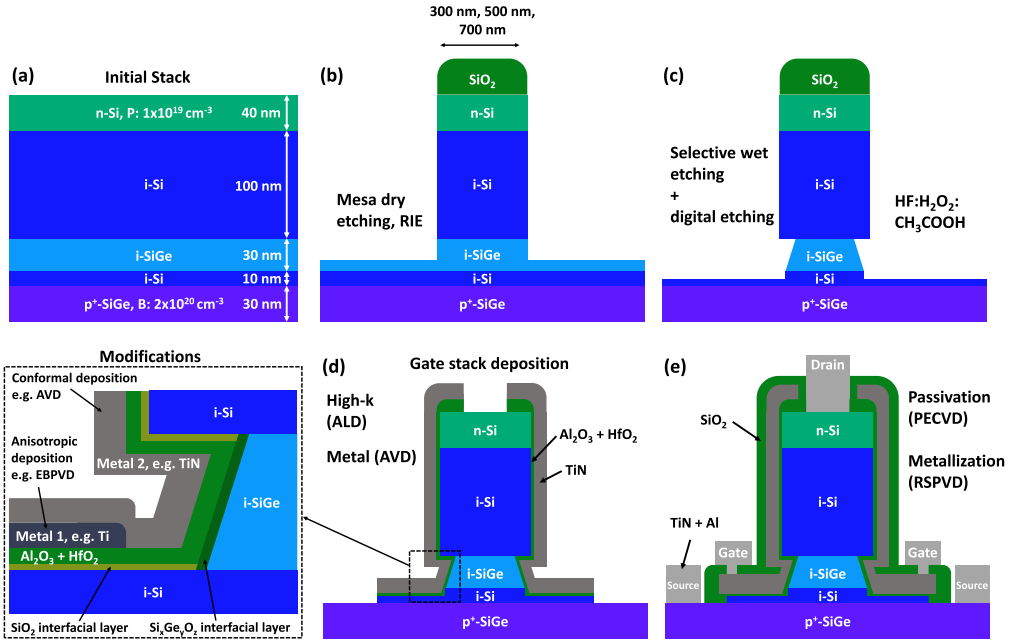

FIGURE 2. **(a-e) Fabrication steps of a vertical gate-normal TFET (L-shape with rotational symmetry). (a) Initial stack composed of SiGe and Si layers as grown by CVD, where the two bottom layers form the tunneling junction. (b) Deposition (by PECVD) and patterning of a SiO_2 hard mask, followed by EBL and RIE used to form pillars with 300 nm, 500 nm and 700 nm diameter. The i-SiGe layers serves as an etch-stop. (c) i-SiGe is removed with selective wet chemistry, resulting in an undercut and exposing a smooth Si surface. Then, the channel thickness is reduced with digital etching. On top of the Si channel the gate stack is deposited subsequently, as shown in (d) and its inset. After Al_2O_3+ HfO_2 deposition with ALD, in an optional step metal 1 (Ti) can be deposited anistropically with EBPVD covering horizontal planes only (inset). Independent of the deposition of metal 1, AVD is (subsequently or exclusively) used to uniformly cover all surfaces with metal 2. EBL and RIE are used to define the gate area. In the gate surrounding area the i-Si layer is removed with TMAH subsequently. (e) SiO_2 is used as a passivation layer, contact openings are patterned into it with EBL and RIE. TiN + Al metal contacts are applied in a lift-off process.**

is heavily influenced by parasitic tunneling into the contact arm as shown in Fig. 1(e,f). However, the upward-bending of the contact arm leads to significantly improved average SS between 10^{-5} μA/μm and 10^{-3} μA/μm reaching well below 60 mV/dec as evidenced in Fig. 1(b) for $\theta > 60°$. To understand this, consider the electric field created by the gate at the point $\vec{r}^*$ [Fig. 1(c)], which is depicted in Fig. 1(g,h). When θ is increased, which is equivalent to the contact arm being bent upwards, the magnitude of the electric field at the point $\vec{r}^*$ decreases and with it the parasitic eBTBT generation rate. Therefore, for $\theta > 60°$ the gate-normal and the parasitic tunneling paths set in at a similar gate voltage and SS is significantly improved.

III. FABRICATION

From a fabrication point of view simply changing the angle θ is not possible, but an analogous structure can be defined, as depicted in Fig. 2. The contact arm is replaced by a pillar located in the middle of a circular-symmetric source-channel-gate overlap region (see also Fig. 3). The actual devices were created according to the process steps listed in Fig. 2. The initial stack, grown by chemical vapor deposition (CVD), consists of a highly doped p^+-SiGe source (Boron doped, 30 nm, $p = 2 \times 10^{20}$ cm^{-3}), on top of which the tunneling layer is positioned which is composed of i-Si (10 nm). The mesa is defined with e-beam lithography (EBL) and reactive ion etching (RIE). Etching is stopped in the i-SiGe-layer [Fig. 2(b), Fig. 3(a)], which is subsequently removed with selective wet chemistry ($HF:H_2O_2:CH_3COOH$, 1:2:3), resulting in a smooth Si surface [Fig. 2(c), Fig. 3(b)]. A smooth interface to the gate [see TEM micrograph in Fig. 3(e)] is crucial, because considerable roughness deteriorates the turn on by smearing out the sharp discrete 2D DOS leading to inferior SS similar to band-tails [22]. Due to the high selectivity of the etching solution an undercut of the i-SiGe layer below the i-Si in the pillar is realized. Next, the Si channel thickness was reduced by a digital etching process, comprising a dry plasma oxidation step and oxide etching in HF to achieve a target thickness of 5 nm or less, by removing 1-2 nm every cycle [see Fig. 3(e)]. Thicker layers are not feasible since the electrostatic control at the tunneling junction, which decreases exponentially with layer thickness, will be insufficient. The high-k layer (Al_2O_3, HfO_2) is conformally deposited by atomic layer deposition. Now one of two options was chosen. In the first option, the gate metal deposition (TiN) is carried out by atomic vapor deposition (AVD) [Fig. 2(d)] only, covering all surfaces conformally. By contrast, in the second version of the process an anisotropic metal deposition process (Ti) is inserted before AVD to create two distinctly separated regions with metals exhibiting different work functions [inset of Fig. 2(d)]. In this non-conformal deposition step, e.g., using electron beam physical

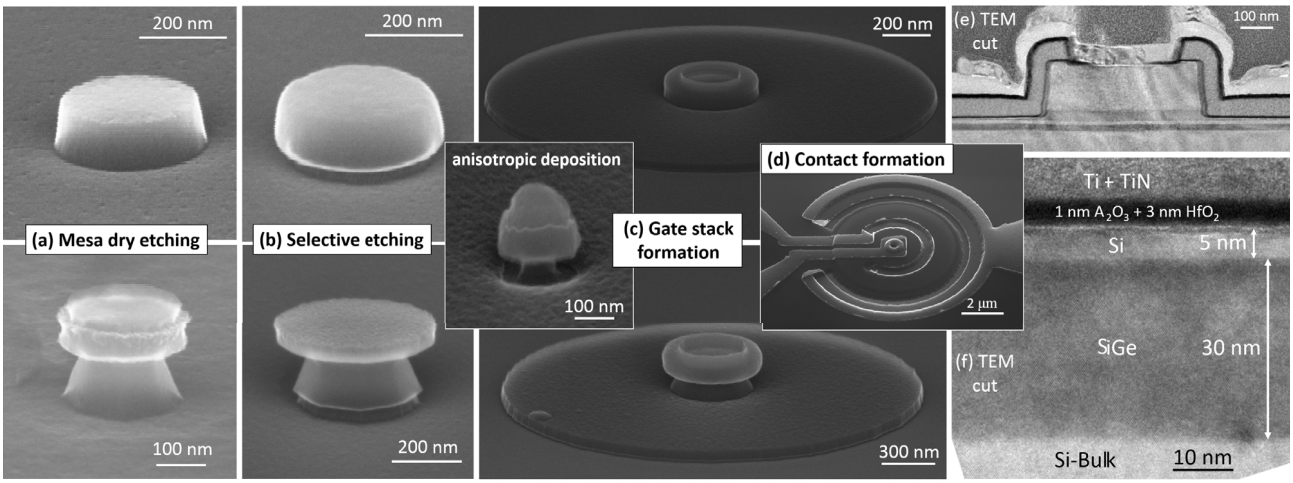

FIGURE 3. **(a-c) SEM images taken at different stages of the fabrication process, as indicated in the images. The lower panels show the same fabrication process steps with a tapered side wall profile below a TiN-disk on top of the pillar. The inset in (c) shows a test structure where the shadowing effect during anisotropic deposition is illustrated with a thicker metal layer than used on actual devices to enhance visibility. (d) SEM view after metal contacting. (e-f) TEM cross section of processed devices showing an overview (e) and a close-up of the tunneling junction (f).**

vapor deposition, Ti covers all but the sidewalls of the pillar and especially not the undercut region. Secondly, the conformal atomic vapor deposition (AVD) process was used to cover the sidewalls and the undercut region with TiN. Next, EBL and RIE are used to etch the gate metal, thereby defining the dimensions of the gate and opening a contact window in the center of the pillar [Fig. 2(d), Fig. 3(c)]. Then, the exposed gate oxide after TiN-etching and the Si channel on the plane are removed by HF and TMAH etching respectively. At last a 100 nm SiO_2 passivation was deposited with plasma enhanced chemical vapor deposition (PECVD), contact openings into the passivation are created with EBL and RIE, and finally TiN+Al contacts were formed in a lift-off process [Fig. 2(e), Fig. 3(d)].

IV. CHARACTERIZATION

Fig. 4(a) shows the transfer characteristics of a device with single gate metal as often observed in experiment. The turn-on starts at $V_g = 0.5\ V$, from where I_d increases slowly until about $V_g = 1.35\ V$. After that, a steeper slope is observed until the current starts to saturate eventually. According to the conclusion from Fig. 1 we can exclude a purely electrostatic origin for the bipartite increase of I_d. Indeed, simulations without quantization [Fig. 4(b)] on the specific structure qualitatively reproduce the $I_d - V_g$ characteristics in Fig. 1(a) for $\theta > 70°$. However, when corrections due to (field-induced) quantum confinement are taken into account, using the density gradient quantization model incorporated in Sentaurus TCAD [24], the traits from experiment can be reproduced [Fig. 4(b)]. The consequences are illustrated in Fig. 4 (b). The green trace exhibits a similar shape as the experimental curve [Fig. 4(a)], comprising a slow initial turn-on followed by a steeper region. The eBTBT generation evaluated in this region (at $V_g = 0.5\ V$) shown in Fig. 4(d) confirms that the problem is caused by tunneling into the pillar, before gate-normal tunneling has commenced. This is a consequence of a non-uniform quantization condition. The 2DEG in region 1 is confined to a triangular potential well induced by the gate, whose width is given by the channel thickness (4 nm in the simulation). At the bottom edge of the pillar the distance from the gate to the source increases and thus the potential-well width. Hence, the correction of the potential due to quantization in the narrower well in region 1 is larger than in region 2 at the bottom of the pillar, where eBTBT generation can be seen in Fig. 4(d). This is in part related to the width of the pillar being large compared to the thin Si channel, so that the physics in the middle of the pillar are almost bulk-like. The stronger quantization in region 1 leads to a delay of the alignment of states from the conduction and valence band [26]. Additionally, the hole BTBT generation [Fig. 4(d)] stems exclusively from SiGe underneath the pillar, owing to the weaker gate-control in this region compared to SiGe underneath the gate.

While the shape of the curves is well reproduced by simulations the magnitude of the current is different, because smaller, but realistic EOT was used for simulations (0.5 nm SiO_2 interfacial layer + 3 nm HfO_2) in addition to a reduced channel thickness (4 nm) to exemplify the feasible performance of such TFETs. Yet, we point out that the employed, basic quantization model may overestimate the current and refer to more elaborate treatments of quantization such as [27], noting that therein gate-normal tunneling shows a similar delay to parasitic edge tunneling as observed here. Fig. 4(c) also contains a solution to the problem, which is a dual-metal gate as proposed before e.g., in [16] and [18]. Like we described in the fabrication section a metal with lower work-function can be deposited self-aligned on the plane with an anisotropic deposition [compare inset of Fig. 3(c)]. Therefore, the metal gate in simulations was split accordingly. The work function Φ_{M1} is applied to

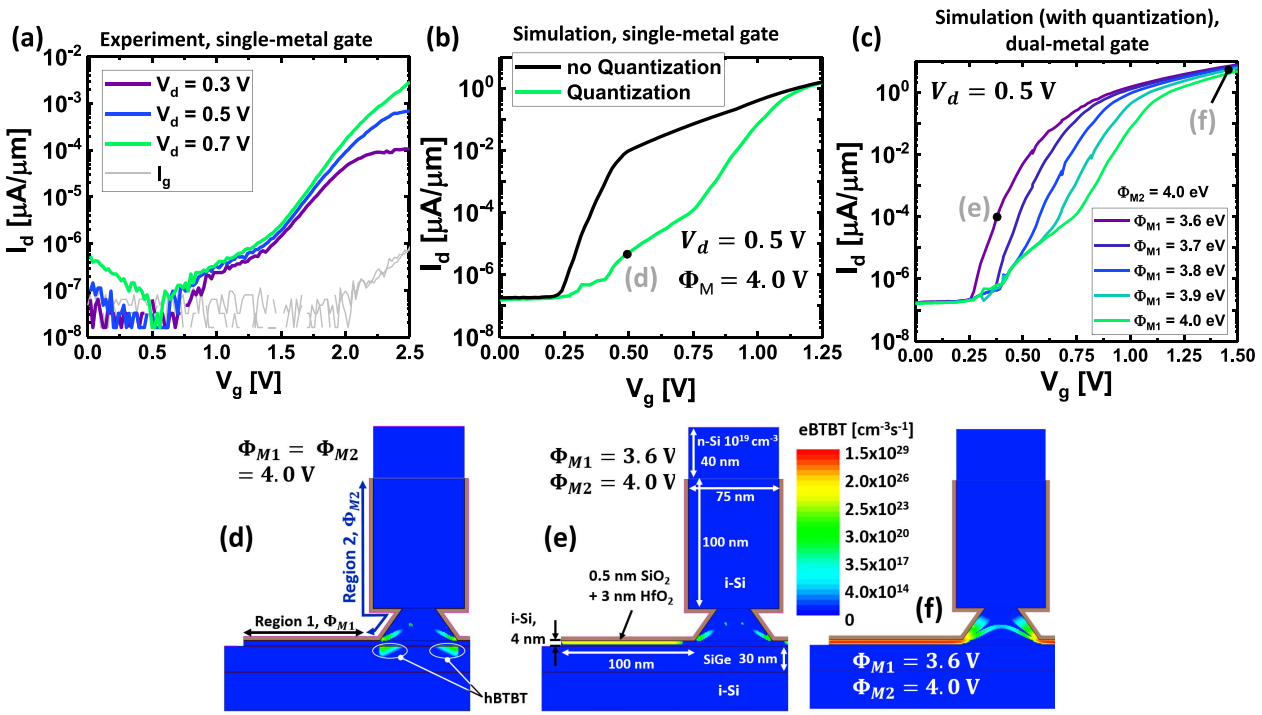

FIGURE 4. **(a) Experimental transfer characteristics, exhibiting a considerably delayed onset of gate-normal tunneling. (b) Comparison of simulated transfer characteristics, evincing that the shape of the experimental transfer characteristics are only reproduced when including quantization corrections. (c) Simulated transfer characteristics employing quantization and two different metal work-functions, on the plane (Φ_{M1}) and in the undercut and sidewall regions (Φ_{M2}). Due to quantum confinement the onset of gate-normal tunneling is delayed substantially ($\Phi_{M1} = \Phi_{M2} = 4.0$ eV), resulting in degraded SS. As can be seen in the contour plot (d), the cause of the degraded SS is eBTBT generation inside the pillar at the point specified in (b). Improved SS can be restored by reducing the gate work function Φ_{M1} to 3.6 eV, leading to a simultaneous onset of eBTBT inside the pillar and in the source-gate-channel overlap region (e). (f) The on-state is dominated by gate-normal tunneling. The structure in (d-f) is symmetric to a vertical axis through the middle of the pillar but cut off for better visibility.**

region 1, extending over the plane as indicated in Fig. 4(d) and stopping right at the corner of the pillar. Region 2 with Φ_{M2} covers the undercut region and the sidewalls of the pillar up to the n-type drain region. When Φ_{M1} is reduced, so is the onset of gate-normal tunneling, as seen in Fig. 4(c,e) for $\Phi_{M1} = 3.6$ V and $\Phi_{M2} = 4.0$ V. By this measure, a non-interrupted sharp turn-on with small SS is recovered. Note, that for the on-state the work-function difference does not play a major role [Fig. 4(c,f)].

In experiment the choice for the two metals fell on Ti and TiN. By this we can estimate the range of possible work-function combinations for different nitrogen incorporation between stoichiometric TiN and Ti. TiN is a well-established material in the semiconductor industry and it is known that the work-function of TiN can be tuned by the amount of incorporated nitrogen [28]. Hence by varying the nitrogen content a whole range of work-functions should become accessible for fine tuning. Other viable options are the additional incorporation of aluminum [29] to manipulate the work-function of TiN. Fig. 5(a) presents capacitance-voltage (CV) characteristics of MOSCAPs with Ti and TiN as gate metal on SiO_2. Clearly, the curves are shifted with respect to each other. Using the inflection point method [30] we determined the flat-band voltage to calculate the difference in metal work-function $\Delta\Phi_M$ between the two MOSCAPs. The obtained value of 0.65 V (in good agreement with [28]) is larger than the 0.4-eV-difference that is needed according to Fig. 4(b) to completely avoid any influence from parasitic edge tunneling on the transfer characteristics. Yet, $\Delta\Phi_M = 0.4$ eV is absolutely contained in the range that is experimentally feasible when tuning the nitrogen content.

The effect of the Ti/TiN dual-metal gate is exemplified in Fig. 5(b,c). The $I_d - V_g$-characteristics show that the turn-on was effectively left-shifted and no region of slowly increasing current in the early subthreshold region is obvious. To reinforce this assessment, we have plotted *SS* vs. V_g obtained from Fig. 5(b) (blue curve) and Fig. 4(a) (green curve) in Fig. 5(c). It is evident that by reducing the onset of gate-normal tunneling with the help of a second metal with lower work-function a smaller SS is achieved. However, the absolute values of SS and I_{on} remain yet to be improved in further research, e.g., by reducing the equivalent oxide thickness, avoiding trap-assisted tunneling, exploiting other material combinations with lower (pure Ge source) or direct bandgap and other measures that have been discussed elsewhere [2]–[4], [13], [31]. It is worth noting that the experimental $\Delta\Phi_M$ may be too large. In the worst case, BTBT uniformly occurs in region 1, whereas region 2 is still highly resistive. Thus, the switching characteristics would be dominated by the resistance in this region and not by the tunneling junction. Though, as pointed out before the issue can be resolved by adjusting Φ_{M1} by controlling the

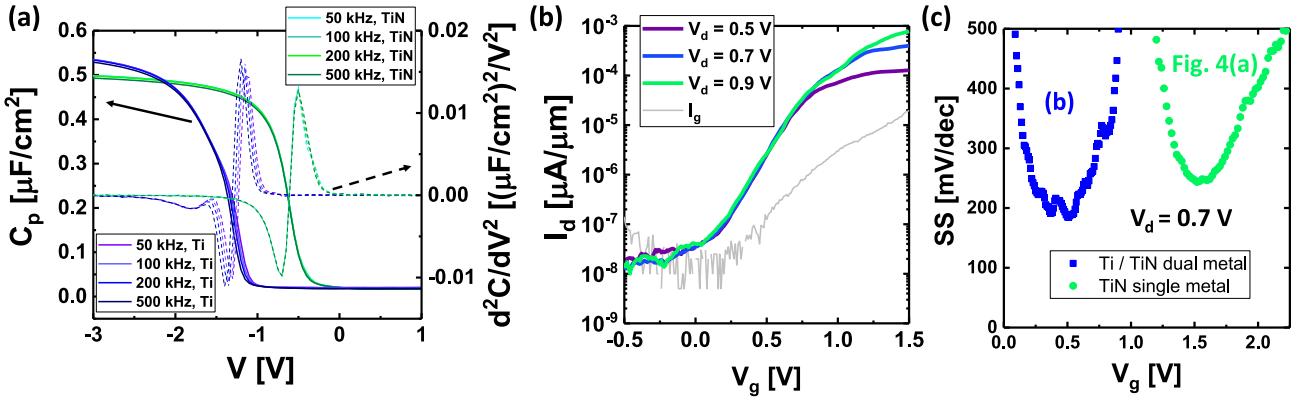

FIGURE 5. **(a) CV characteristics (solid lines, left y-axis) of a MOSCAP with Ti and TiN as gate metal on 8 nm thermal SiO_2/Si-Bulk. The flat band voltage for both metals is determined via the inflection point method [30], where the zero-crossing of the second derivative of the capacitance (dashed line, right y-axis) corresponds to V_{FB}. $V_{FB}^{Ti} \approx -1.26$ V and $V_{FB}^{TiN} \approx -0.61$ V, corresponding to a V_{FB}-Difference and thus a work function difference of about 0.65 V. (b) $I_d - V_g$-characteristics of a device with Ti / TiN dual metal gate. (c) Due to the lower work-function of Ti, gate-normal tunneling sets in earlier in the dual-metal TFET (for otherwise identical parameters) and thus a better SS is achieved.**

nitrogen content. Anyhow, the general inferences that were made on TFET shape and the use of a dual-metal gate are neither mitigated by the performance nor restrained to the SiGe/Si material system. Therefore, they should be transferable to other material combinations like SiGeSn/GeSn or other material systems like III-V semiconductors.

V. CONCLUSION

We have presented a physical analysis for a gate-normal TFET with a pillar-shaped contact to the tunneling junction and elucidated its advantages regarding a viable and self-aligned fabrication process. In addition, the pillar shape is beneficial in terms of electrostatics to reduce the negative influence of parasitic tunneling paths. Because quantum confinement delays the onset of gate-normal tunneling, we have shown that the utilization of a Ti/TiN dual-metal gate becomes necessary to restore an unobstructed turn-on. Our findings obtained on SiGe/Si TFETs are not limited to the specific material combination and thus provide directives for future research with lower bandgap materials such as GeSn/SiGeSn.

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