On the Understanding of Cathode Related Trapping Effects in GaN-on-Si Schottky Diodes

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ABSTRACT Cathode related current collapse effect in GaN on Si Schottky barrier diodes is investigated in this paper. Capacitance and current relaxation measurements on diodes and gated-Van Der Pauw are associated with temperature dependent dynamic $R_{ON}$ transients analysis to identify the parasitic trapping locations in the devices. We show here that the main part of the current collapse at the cathode comes from a combination of electron trapping in the passivation layer and in a carbon related trap in the GaN buffer layers ($E_A = E_T - E_V \approx 0.9 \text{eV}$) that can be studied independently by using the appropriate stress configurations. These two parasitic effects can lead to long recovery time (>1 ks) after reverse bias stress.

INDEX TERMS Power semiconductor devices, gallium nitride, AlGaN/GaN, Schottky diodes, dynamic $R_{ON}$, field plates, trapping dynamics, test structures, gated Van der Pauw.

I. INTRODUCTION GaN-on-Si Schottky barrier diodes have emerged during the last decade as candidates to replace silicon based devices in medium power applications (100-1200V / 10-100A). Recently, promising results have been demonstrated on both HEMTs (High Electron Mobility Transistor) [1]–[3] and SBDs (Schottky Barrier Diode) [4]. However, a “current collapse” effect related to electron trapping can induce an $R_{ON}$ increase and thus a high power dissipation during switching. Consequently, recoverable processes remain a matter of concern at the same level as long-term reliability. Academic and R&D efforts are focused on reducing and even removing this effect [1], [3] and also on understanding its origins [5]–[7]. Optimization of the epitaxial buffer [5], [6], [8] and the introduction of field plates in the device structure [7], [9], [10] can significantly improve the dynamic behavior of GaN-on-Si power devices. In particular, the effect of drain field plates in transistor configuration has been explored in [7] and related to electron trapping under the field plate in interface states between the passivation layer and the front barrier.

In this paper, different cathode field plate (FPC) configurations are studied using dynamic $R_{ON}$, capacitance and current relaxation measurements. An in depth analysis will be presented on associated relaxation transients to give a novel insight into cathode field plate related current collapse. Section II describes the devices configurations used in this work for capacitance and current relaxation transients, Section III focuses on the recovery of capacitance and pinch-off voltage $V_{po}$ shift. Current characteristics on gated-VDP (Van Der Pauw) with different stress configurations to differentiate trapping effects consistent with a FPC diode structure are shown in Section IV. Finally, temperature dependent measurements leading to the extraction of the energies of traps are presented in Section V allowing interpretation of cathode related current collapse effects.

II. DEVICE AND SETUP DESCRIPTION

A. DEVICES DESCRIPTION

200mm GaN-on-Si wafers were grown using metalorganic chemical vapor deposition (MOCVD). A structure consisting of “Transition Layers” is grown directly on a 1 mm thick lightly doped (~ 10 Ω.cm) p-type Si substrate. A Carbon doped GaN (GaN:C) layer is then grown on top to ensure electrical insulation between the substrate and the top active layer while improving GaN breakdown voltage [11], and
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FIGURE 1. GaN on Si SBDs structure, FPC depicts the cathode field plate.

the GaN growth is finished with a thin unintentionally doped GaN layer (GaN:NID) which forms the channel. Next, a 1nm AlN spacer is grown, followed by a 24nm AlGaN barrier (23% in Al content) to form the 2DEG (2-D Electron Gas) at the GaN interface, before a final 10nm in-situ SiN passivation layer is grown.

The diode structure is presented in Fig. 1. Titanium nitride (TiN) is used as a Schottky contact while an Ohmic contact is formed using a Ti/AlCu 875°C annealed stack. The anode metal is deposited on the GaN layer after the AlGaN layer has been fully removed. The AlGaN layer is only partially recessed to make the ohmic contact. Anode to Cathode length is 15 μm to ensure a high lateral breakdown voltage. Three anode field plates (FPAs) are embedded to smooth the electrical field at the edge of the anode during reverse bias electrical stress. On the cathode side, a field plate (FPC) is defined on top of the10nm in-situ SiN/140nm LPCVD SiN stack. The FPC length varies between L_{FPC} = 0.5 and 3.5μm. The nominal width of the power SBD devices is W = 52 mm. The anode and backside contacts are connected in this study.

B. CHARACTERIZATION SETUP

To characterize $R_{ON}$ recovery transients, a microsecond resolved test setup is used [12] giving accurate acquisition in the range of 3μs to several ks after switching. SBDs were reverse biased up to $V_{REV} = -600$V for 10s at 25°C and up to $V_{REV} = -550$V at 150°C then a forward current of $I_F = 1$ A is used to characterize ON-state recovery. Fig. 2. depicts the evolution of normalized $R_{ON}$ extracted at 10μs after switching under increasing reverse voltage for diodes with different FPC configuration. A large increase of dynamic $R_{ON}$ is observed for the devices at different values of voltages depending on the FPC configurations and on the temperature. The devices recovered the $R_{ON}$ fresh value after some time in the ON state. The points missing at 150°C for the 3.5μm and 2μm cathode field plate lengths are due to device breakdown or to a huge current collapse where only current noise is measured (the 2DEG is still fully depleted 10μs after the switch).

Capacitance/current based measurements are performed with a Keysight B1505 combined with a high voltage bias-tee. A Cascade TESLA probe station is used to probe the devices while maintaining a fixed chuck temperature between 25°C and 150°C.

III. TRAPPING EFFECTS THROUGH CAPACITANCE MEASUREMENTS

As shown in Fig 2, a severe $R_{ON}$ increase is observed after a cathode stress above 400V for the configuration with a long FPC, revealing strong electron trapping in the cathode field plate area. Measurement of the global diode reverse capacitance in Fig. 3 shows the direct relationship between FPC length and the depletion regime that occurs at high reverse voltage ($|V_{rev}| > 400$V). Depletion occurs under the FPC, which is emphasized by the vertical cathode-substrate capacitance where depletion arises at the same voltage as for the SBD. Nevertheless, this depletion effect on the cathode side is not straightforward since electrons are attracted by the cathode and repulsed by the anode. To study more precisely the effect of trapping on the device behavior, additional capacitance measurements on specific test structures have been performed.
A. GATED-VDP CAPACITANCE MEASUREMENTS

In-depth analysis has been carried out through recovery measurements on a specific VDP-gated structure (Fig. 4) that reproduces the configuration of a diode FPC. The gated VDP structure enables us to perform both current and capacitance measurements, and three types of electrical stress can be used. In the first case, a pure gate-to-channel stress is applied where the gate is biased at a given $V_G$, so that electrons are injected from the 2DEG directly into the FPC equivalent dielectric stack. In the second stress case, a negative bias is applied to the substrate while the gated-VDP structure is grounded, representing the vertical stress on the SBD cathode when polarized in reverse mode. The third stress case called “Floating gate configuration” is used where the substrate is biased with the contacts grounded and the gate voltage is left floating. In this section, capacitance measurements are made on the gate stress and diode-like (also named substrate stress) configuration. The three configurations will be later compared in terms of current relaxation in Section IV.

Capacitance-voltage $C(V)$ characteristics as a function of relaxation duration after both gate and substrate stresses (with gate grounded ie in a diode-like configuration), [60V, 10s] and [−500V, 60s] respectively, are shown in Fig. 5. The $C(V)$ characteristics shift towards positive voltages for both stress conditions, which is a sign of electron trapping inside the dielectric stack under the FPC. The independence of conductance peaks related to GaN/AlGaN and AlGaN/in-situ SiN interfaces (not shown) implies that the electron trapping arises in the dielectric volume (SiN LPCVD here). There are significant differences between the two stress conditions, in terms of both amplitude and shape of the curves. An additional capacitance is observed after a substrate stress around the pinch-off voltage of the gated-VDP which tends to disappear after a sufficient recovery duration.

B. $V_{p0}$ SHIFT RELAXATION

To further analyse these effects, the pinch-off voltage shift ($\Delta V_{p0} = V_{p0}(t) - V_{p0, fresh}$) is plotted as a function of recovery duration for the two stress types and at two temperatures, 25°C and 150°C (Fig. 6). Gate stress recovery transients show a recovery law $\Delta V_{p0} = A \cdot \ln(1 + B/t_r)$, where $t_r$ represents the recovery time, A and B do not depend on time, and suggesting a self-limiting process, which is well known in the field of BTI (Bias Temperature Instabilities) recovery transients. Substrate stress recovery transients are more complex and exhibit two regimes for both temperatures, with the latter transient following the same trend as a gate stress recovery combined with an additional short time mechanism. This analysis suggests that additional electron trapping towards the substrate under the FPC could act as a second source of $R_{ON}$ increase. We can also consider the so-called FPC depletion in Fig. 3 as a $V_{p0}$ shift under the FPC region induced by electron injection into the passivation dielectric. In the next section we will linked the capacitance $V_{p0}$ shift relaxation to a current relaxation measurement and analyse more deeply the relaxation behavior.
IV. GATED-VDP CURRENT RELAXATION MEASUREMENTS

A. CURRENT RELAXATION: A DIFFERENT WAY TO STUDY TRAPPING EFFECTS

The lateral current relaxation in the gated-VDP structures after a gate stress was also studied. Here we show that the current relaxation measurement enables to extract the $V_{po}$ shift as we did in the capacitance measurement. The trapping effects can be seen as a $V_{po}$ shift or as an increase of resistance. Sheet resistance was measured after the stress by setting the gate voltage to $V_G = 0\, \text{V}$ with a 100nm lateral voltage to get a realistic image of the 2DEG depletion. The $V_{po}$ shift in the FPC stack configuration can be studied using several gate stress voltages. The advantage of the current relaxation measurement is to record faster and more accurately the recovery of the 2DEG under the gate. An $I_{VDP}$ ($V_g$) curve without stress is first recorded to be used as a reference to extract the $V_{po}$ without stress. The $V_{po}$ is chosen arbitrarily at a current of $10^{-7}$ A on this curve. The device is then stressed via the gate (to probe only the FPC stack) and the change of current due to the building of a negative stored charge in the oxide is seen as a change of $V_{po}$. Using the $I_{VDP}$ ($V_g$) curve, we can convert the $R_{\text{sheet}}$ ratio relaxation into a $V_{po}$ shift (Fig. 7). We can see on Fig. 7 at each given voltage, how the change of $V_{po}$ is seen in terms of $R_{\text{sheet}}$ ratio recovery.

The $V_{po}$ transients for different stress voltages at 25°C and 150°C are presented in Fig. 8. We can see that the recovery of the $V_{po}$ follow the same law as in III.B: $\Delta V_{po} = A \cdot \ln(1 + B/t_r)$. So the measurement of the current relaxation and the $R_{\text{sheet}}$ associated is a direct measurement of a $V_{po}$ shift. The power law behavior is typical of trapping events in IMD layer. The recovery times are also very high (above 1000s of seconds). At higher temperature, we can also notice that the shift is higher but follows the same recovery law with respect to time. The change of initial trapping with the increasing gate voltage is consistent with the $V_{\text{th}}^2$ term (acceleration factor) included in the $A$ factor. We also observe that above a 50 V stress on the FPC stack an increase of the detrapping time. More generally when increasing the voltage on the gate, the detrapping time increases also a bit. This could be due to permanent trapping in the oxide. The IMD detrapping behavior can then be identified in more complex recovery mechanisms occurring in SBDs compared to the exponential law of semiconductor traps. We have shown that the $R_{\text{sheet}}$ change obtained from current measurement is also an accurate measure of a $V_{po}$ shift for trapping in IMD. The $R_{\text{sheet}}$ extraction is a better tool to assess the behavior of the other gated-VDP configurations and to compare the configurations together. In the next two subsections, we will then investigate the $R_{\text{sheet}}$ relaxation at 25°C and 150°C of the gated-VDP structure in the three different stress configurations to identify specific trapping locations. The configurations are studied two by two in regards to the diode-like configuration. With this method we can identify the location of trapping events.

B. STUDY OF BUFFER TRAPPING: COMPARISON OF FLOATING GATE AND DIODE-LIKE CONFIGURATIONS

In this section we compare the two stress configurations that implies buffer trapping: the substrate stress configuration diode-like and the floating gate configuration, the $R_{\text{sheet}}$ transients are shown respectively in Fig. 9 and Fig. 10 each at two temperatures (25°C and 150°C).The stress configuration called “floating gate” has been used to really differentiate buffer trapping from surface/passivation layer trapping. This is the same configuration as the substrate stress described previously but with the gate not grounded (Fig. 4). With this configuration, even at high substrate voltages (in absolute value), the 2DEG should not be depleted and we should probe only the buffer layers. For the diode like configuration at 25°C (Fig. 9), there is a huge increase of the $R_{\text{sheet}}$ ratio at $-500\, \text{V}$. Before this voltage, the $R_{\text{sheet}}$ ratio increases with the voltage but does not exceed 10 times the fresh value. We can notice that for all the voltages higher that $-500\, \text{V}$ there is a similar recovery behavior: one main detrapping time constant around a few hundred seconds. At $-500\, \text{V}$ however, in addition to the dramatic increase of $R_{\text{sheet}}$ ratio, the
transient seem to be due to two superimposed mechanisms. If we compare this to the floating gate stress (Fig. 10), we see that the $R_{\text{sheet}}$ ratio in the latter is way lower. This could be due to the configuration that leads to trapping mainly under the contacts where the electric field is higher and not in the entire buffer volume. So the $R_{\text{sheet}}$ ratio may not be compared directly to each other. But the main information to get from this curve is the fact that there is no dramatic increase of $R_{\text{sheet}}$ ratio below $-500$ V and even at $-550$ V at $25^\circ$C. Also there is only one main time constant. This suggests that the additional trapping seen in Fig. 9 is not buffer related. However it is more difficult to interpret the curves at $150^\circ$C with this stress configuration. For the diode-like configuration, the voltage where the huge increase of $R_{\text{sheet}}$ ratio appears is shifted to $-400$ V with a really large time constant compare to the previous voltages. This could be explained because it is easier to inject electrons from the buffer to the GaN:C layer at $150^\circ$C with additional thermal energy. The time constant recorded around 100s seconds at $25^\circ$C for the lower voltages have shifted between 0.1 and 1 s (decrease of detrapping time constants with the temperature which is consistent with the arrhenius law). The additional trapping mechanism appears on the $-350$ V curve and prevails at $-400$ V and above (in absolute value). It is interesting to notice that the voltages where the huge increase of $R_{\text{sheet}}$ ratio occurs at $25^\circ$C and $150^\circ$C is the same as seen on the Ron dyn curve of II.B for the large cathode field plates diodes. We could foresee this behavior because the “diode-like” configuration can be seen as a field plate above the channel but with only 1D effect compare to the diodes stress (2D). The floating gate transients at $150^\circ$C on Fig. 10 do not give more information on the buffer behavior. But it shows an increase of $R_{\text{sheet}}$ ratio around 100s as if trapping occurs during the relaxation time. Also the $-550$ V curve show an increased $R_{\text{sheet}}$ ratio compared to the other voltages but not really similar to what have been discussed above.

**C. STUDY OF DIELECTRIC TRAPPING: COMPARISON OF GATE STRESS AND DIODE-LIKE CONFIGURATION**

By comparing $R_{\text{sheet}}$ relaxation between two stress configurations we have identified the contribution of buffer trapping under the cathode field plate. We can do the same with dielectric trapping by comparing the gate stress configuration to the diode-like configuration. The $R_{\text{sheet}}$ relaxations for the gate stress configurations are presented on Fig. 11.
The relaxation transients with gate stress do not exhibit the same behavior as the buffer transients seen on Fig. 10. We saw in Section IV-A that the $V_{po}$ relaxation after a gate stress is typical of trapping in oxide and is a typical BTI-like relaxation law $\Delta V_{po} = A \cdot \ln(1 + B/t_r)$. The $R_{\text{sheet}}$ relaxations behavior here are then only due to the change of $V_{po}$. Again this behavior is not one of a semiconductor trap where the detrapping $R_{\text{sheet}}$ transient should follow an exponential law (see Fig. 10 left). This behavior is also observed in the “diode-like” configuration with sufficiently high enough substrate voltage stress at 25°C and 150°C. High voltage is necessary to observe trapping in the IMD with a diode-like configuration because the 2DEG must be depleted and the voltage across the FPC stack must be high enough to trap electrons and store a substantial negative charge. This proves that oxide trapping happens in the diode under the cathode field-plate. Increasing again the voltage enables electrons to be trapped further from the 2DEG in the dielectric. The time for these electrons to be emitted in the channel region after the stress increases with the distance to the channel. Then the negative potential stored in the IMD remains longer at higher stress voltages. The diode-like configuration curves are then clearly the sum of these two different mechanisms: trapping in the buffer with relaxation typical of semiconductor traps and trapping in the IMD with BTI-like relaxation law.

V. DYNAMIC RON AND TRAPS ENERGY EXTRACTION

A temperature dependent dynamic $R_{\text{ON}}$ study was performed to confirm the combined effect of trapping in the dielectric under the FPC and in the substrate. The amplitude of the current collapse effect was measured for two designs, with Fig. 12 showing $R_{\text{ON}}$ recovery between 1μs and 600s after cathode stress up to 750V. While the amplitude of the current collapse effect is almost null at 600V on a SBD with $L_{\text{FPC}} = 0.5\mu$m, the amplitude is multiplied by up to 100 when $L_{\text{FPC}} = 2\mu$m. In addition, the relaxation times for the traps appear to be different for these two SBDs structures.

Dynamic $R_{\text{ON}}$ transients were performed for temperatures between 25°C and 120°C on SBD with two FPC lengths, 0.5 (not shown here) and 2μm (Fig. 13). The time constants for the traps were extracted using a multiexponential fit and the derivative of the $R_{\text{ON}}$ vs log(t) after a smart polynomial fit.

An Arrhenius plot (Fig. 14) reveals four traps for the short FPC configuration. The trap extracted at $E_A = 0.56eV$ has been reported to be related to Si-dopants, while the trap extracted at $E_A = 0.75eV$ tends to imply the presence of Nitrogen in an interstitial position in the lattice [13].

Although these two traps are apparent for the short FPC (0.5μm), they play only a minor role in the amplitude of the trapping. On the contrary, a large amplitude of the current collapse in the short FPC diode is related to a trap located at $E_A = 0.92eV$. This trap is related to carbon impurities introduced in the GaN buffer to ensure electrical insulation by creating a deep acceptor (also called a hole-like trap) [8], [13], [14]. This trap signature is also extracted for the long FPC (2μm) configuration and is responsible for the majority of the current collapse effect. This proves
that increased trapping in the GaN:C buffers arises in the case of long FPC in diodes caused by electron trapping due to the vertical electrical field. The deviation from the Arrhenius law at low temperatures observed in this case has been recently related to barrier lowering due to the Poole-Frenkel effect [14] when a charge is stored into the buffer while current relaxation measurement on gated-VDP showed that we can differentiate trapping in the buffer from trapping in the dielectric by using appropriate stress configurations. Temperature dependent analysis on diode recovery transients confirmed that a severe trapping arises in the GaN:C layer (on carbon deep acceptor level $E_A \approx 0.9$ eV) as well as in the dielectric under the FPC.

VI. CONCLUSION

In this paper, we have presented an exhaustive analysis of cathode related current collapse effect in GaN on Si SBDs. Capacitance measurements on power diodes and on gated-VDP confirmed that electron trapping in the passivation dielectric below the FPC can arise under reverse bias stress, while current relaxation measurement on gated-VDP showed that we can differentiate trapping in the buffer from trapping in the dielectric by using appropriate stress configurations. Temperature dependent analysis on diode recovery transients confirmed that a severe trapping arises in the GaN:C layer (on carbon deep acceptor level $E_A \approx 0.9$ eV) as well as in the dielectric under the FPC.

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