Introduction to the Special Section on the 2017 IEEE S3S Conference

This special section of the IEEE JOURNAL OF ELECTRON DEVICES SOCIETY is dedicated to select papers presented at the 2017 IEEE S3S Conference, which was held Oct. 16 – 19, 2017 in Burlingame, CA, USA. The papers were selected based on their technical merits and relevance to the Journal and with the feedback from the Technical Committee of the conference and session chairs.

For over four decades, this conference has been the premier IEEE event where the latest advances in the SOI technology have been discussed. In the past few years, we have expanded the focus of the conference to include 3D integration, building on the synergy between SOI technology and 3D wafer processing and aiming to address the challenges of energy efficient information processing. The papers in this Special Section represent these topics.

The first paper, by Hashemi et al. describes symmetric lateral bipolar junction transistors fabricated on SOI with epitaxially-grown emitter and collector regions. By using a CMOS baseline technology they report lateral NPN transistors with collector-emitter spacing down to 100nm.

In the second paper, Kazemi Esfeh et al. report the small and large signal characteristics of single pole double throw (SPDT) RF antenna switches and demonstrate the advantages of trap-rich SOI substrates over traditional high resistivity SOI in reducing the second harmonics, while enabling a thinner buried oxide (BOX).

Muralidhar et al., in the third paper, describe a U-shaped channel FDSOI device structure to enable extreme channel length scaling. They report TCAD simulations that show feasibility of scaling the physical gate length below 20nm without need to scale the channel thickness.

In the next paper, Deng et al. report SOI interface coupled photodetectors. TCAD simulations and experimental data are provided and the advantages of the structure in suppressing crosstalk between neighboring cells are discussed.

Mori et al., in the fifth paper, report diode characteristics of super-steep subthreshold slope body-tied SOI FETs. They demonstrate sharp turn-on characteristics even in sub-50mV voltage range and position their proposed device for energy harvesting applications.

The next three papers are dedicated to 3D integration. In the first of these, Lee et al. report monolithic integration of CMOS and III-V devices through wafer bonding including a variety of HEMT and LED devices.

In the next paper, Kim et al. report heterogeneous integration of Ge and III-V on Si to enable a wealth of different applications, including InGaAs MOSFETs, GaAs photodetectors, Ge waveguides and GaN light-emitting diodes.

Finally, Abedin et al. describe germanium-on-insulator fabrication process with a maximum temperature of 350°C for 3D monolithic integration. MOSFET fabrication still uses somewhat higher thermal budget of 600°C. Devices demonstrate 60% higher hole mobility compared to Si control.

We would like to thank the authors for contributing their papers and meeting the tight schedule of this Special Section. We also thank the anonymous reviewers for their constructive feedbacks that ensure high quality of the Journal; the JEDS Editor-in-Chief, Prof. Mikael Östling, and the IEEE staff for their support.
Ali Khakifirooz (S’99–M’08–SM’11) received the B.S. and M.S. degrees from the University of Tehran in 1997 and 1999, respectively, and the Ph.D. degree from the Massachusetts Institute of Technology in 2007, all in electrical engineering. As a part of his Ph.D. thesis, he studied performance scaling and carrier transport in advanced MOSFET technologies.

From 2008 to 2014, he was with IBM Research, where he contributed to the development of FDSOI technology and later to the 10-nm and 7-nm pathfinding activities. From 2014 to 2015, he was with Spansion Inc. and subsequently Cypress Semiconductor, where he worked on 32-nm NOR, embedded flash, and 3-D NAND technologies. He is currently with Intel, researching on 3-D NAND pathfinding. He has authored or co-authored three book chapters and over 100 journal and conference papers and holds over 600 issued U.S. patents. He was the Technical Program Chair of the IEEE S3S Conference in 2017 and is the General Chair in 2018.

Nobuyuki Sugii (M’08–SM’15) received the B.S., M.S., and Ph.D. degrees in applied chemistry from the University of Tokyo in 1986, 1988, and 1995, respectively. He joined the Central Research Laboratory, Hitachi Ltd., in 1988. Since 1996, he has been working on the research and development of CMOS devices including strained-silicon and SOI. From 2010 to 2015, he served as a Research-Group Leader for the Low-Power Electronics Association & Project and developed ultra-low-power thin-BOX FDSOI (named SOTB) process and design environment for ICs operating down to 0.4 V. From 2004 to 2015, he also served as a Visiting Professor with the Tokyo Institute of Technology.

He is currently with Research and Development Group, Hitachi Ltd., where he is working on sensing devices and systems. He has been a Technical Committee Member of the IEEE VLSI Technology and the IEEE S3S Conference. He is a fellow of the Japan Society of Applied Physics.