Diode Characteristics of a Super-Steep Subthreshold Slope PN-Body Tied SOI-FET for Energy Harvesting Applications

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ABSTRACT In this paper, the diode characteristics of our newly proposed super-steep subthreshold slope “PN-body tied (PNBT) silicon-on-insulator field-effect transistor” are presented, and compared with conventional diodes. We report that the device possesses super-steep characteristics, low leakage current, and sharp turn-on characteristics, even in the ultralow voltage range (50 mV). These indicate that the PNBT diode can potentially be used in high-efficiency rectification for energy harvesting, particularly in situations where there is ultralow input power. In addition, the hysteresis characteristics and the slight shift of the voltage at zero current are confirmed as specific characteristics of PNBT diodes.

INDEX TERMS Energy harvesting, SOI MOSFET, steep subthreshold slope.

I. INTRODUCTION

The Internet of Things (IoT) envisions spreading billions of sensors globally [1]. For economic and environmental reasons, it is desirable that these ultra-low-power autonomous systems be operational without requiring battery power. Therefore, various energy harvesting technologies have been considered as power sources [2]. For example, Radio-frequency (RF) energy harvesting is a promising power source for such systems because it is contactless and covers a wide area, when compared to other energy harvesting technologies. However, the expected power is very small and reduces to below the microwatt level when the coverage area is increased. Therefore, the most pressing problem, with regards to RF energy harvesting, is high-efficiency rectification, because conventional diodes do not function as rectifiers at such ultralow input powers. To increase the input voltage to the diode, passive enhancements have been proposed, such as the use of the resonance with the inductance of the antenna and the parasitic capacitance of the rectifier [3].

We have also proposed a rectenna with a high-impedance (Hi-Z) antenna [4] for the passive enhancement of the diode. However, the best efficiency achieved so far is approximately 10%, at an input power of $-30$ dBm.

To develop a rectenna with high-rectification efficiency, for an ultralow input power of below $-30$ dBm, it is necessary to reconsider the type of diode technology employed. For example, ultralow-power (ULP) diodes [5] can be used to suppress the reverse leakage current, by the combination of an N-channel metal–oxide semiconductor field-effect transistor (MOSFET) and a P-channel MOSFET. To significantly improve the turn-on characteristics, a new diode mechanism that has a near-zero turn-on voltage is required. This is referred to as a zero-bias diode. The backward tunnel diode is recognized as an ideal zero-bias diode and has already been reported in applications for energy harvesting [6]. However, its rectification characteristics are still insufficient. In this study, we reconfirmed the measured characteristics of conventional diodes, and for the first time, we report the measured diode characteristics of our newly proposed super-steep subthreshold slope (SS) PN-body tied (PNBT) silicon-on-insulator field-effect transistor (SOI-FET). By comparing the measured data, we show the
potential of our proposed PNBT device for ultralow power rectification.

II. ISSUES REGARDING CONVENTIONAL DIODE

Fig. 1 shows the measured $I − V$ characteristics of conventional diodes such as the Schottky barrier diode (SBD; a commercial SBD fabricated by Avago Technologies, model number HSMS285c) which has a low turn-on voltage for low-power, and the metal–oxide–semiconductor (MOS) diodes of 0.18-µm bulk complementary metal–oxide–semiconductor (CMOS) technology. A MOS diode is formed by connecting the gate of the device to its drain. There are three types of MOS diodes, composed of MOSFETs with different threshold voltage values $V_t$ ($V_{t1} = 0.43 \, \text{V}$, $V_{t2} = 0.02 \, \text{V}$, and $V_{t3} = −0.23 \, \text{V}$) [7]. The turn-on voltage of the MOS diode is decreased by reducing the $V_t$ of the MOSFET. However, the reverse leakage current increases for the MOS diode (with $V_{t3}$). The $I − V$ behavior of the MOS diode (with $V_{t2}$) is comparable to the SBD; resulting in the realization of approximately 10% efficiency at −30 dBm with a combination of a 2 kΩ Hi-Z antenna, as shown in our previous simulated studies [7].

![Measured conventional diode $I − V$ characteristics. Three MOS diodes with different $V_t$ ($V_{t1}$, $V_{t2}$, $V_{t3}$) and SBD. (a) Linear scale, (b) Semilog scale.](image1.png)

Fig. 2 shows the calculated result for the passive enhancement of the ultralow input power (−30 dBm and −40 dBm) obtained using the Hi-Z antenna. The input voltage increases to approximately 50 mV for antennas with loads varying from 2 kΩ to 10 kΩ. This represents a significant improvement compared to less than 10 mV for the standard 50 Ω antenna. However, this is still a very low input voltage. Fig. 3 shows the expanded $I − V$ plot of Fig. 1(a) at the region around the input voltage of 50 mV, which shows that both the SBD and the MOS diode (with $V_{t2}$) have a slight non-linearity and that the MOS diode (with $V_{t3}$) behaves like a resistor at the near-zero bias. A backward tunnel diode would improve the results, and we believe that the super-stEEP device will prove to be another candidate that possesses sharp turn-on characteristics at an ultralow voltage.

![Enhancement of input voltage by increasing antenna impedance.](image2.png)

![Expanded $I − V$ of Fig. 1(a) around the 50-mV range.](image3.png)

III. NEW DEVICE STRUCTURE AND MEASUREMENT METHOD

Steep subthreshold slope (SS) devices, such as tunnel FETs (TFETs) [8]–[10] and negative capacitance MOSFETs [11], [12], have been extensively studied as potential candidates for the exploration of ultralow power applications, in order to overcome the theoretical lower limit of the SS at room temperature (60 mV/dec) for conventional MOSFETs. In addition, TFETs have also been considered for use as rectifiers in energy harvesting [13], [14], and achieve high rectification efficiency. However, these are only simulation results. As an alternative, we propose the super-stEEP SS PNBT SOI-FET shown in Fig. 4(a) [15]–[17]. The devices were fabricated using a 0.2-µm SOI CMOS process, with a 50 nm thick SOI, 200 nm buried oxide (BOX), and a 4.4 nm thick gate oxide. The PNBT SOI-FET is a conventional body-tied device with an N-region inserted between a P contact region and a body region, which makes up the PNP bipolar junction transistor (BJT) structure. The P-region under the gate extends into the source and drain regions forming a cross to maintain the overlay accuracy, according to the layout rules of our operational process. Fig. 4(b) shows the plan view and the measurement configuration of a MOS diode with the PNBT (hereinafter, termed as PNBT diode). In this study, both the gate terminal and the drain terminal were connected using a three-way triaxial connector to characterize the MOS diode. The characteristics of the device were measured using an Agilent B1500A semiconductor device parameter analyzer in dark lighting conditions.

![Expanded $I − V$ of Fig. 1(a) around the 50-mV range.](image4.png)

Fig. 5 illustrates the operating principle of the PNBT diode. The purpose of the PNBT approach is to induce floating-body effects (FBEs) using methods other than impact ionization. It is known that the super-stEEP SS occurs in a floating body SOI-FET due to FBEs [18], [19]; however, unlike conventional FBEs, the PNBT approach does not use impact ionization. It is intended that holes are to be injected by the PNP-BJT. When the anode voltage is increased, electrons diffuse from the source to the body and
modulate the N-region potential. As a result, the height of the barrier for hole injection from the body to the channel region is decreased. The injected holes also accumulate in the channel region and modulate the channel region potential. This feedback action causes a super-steep SS in the PNBT SOI-FET. The mechanism of MOS gate-controlled thyristors [15], [20]–[22] is also expected to be involved in the super-steep SS of the PNBT device. We consider the case that the N-region width \( W_b \) affects the injection coefficient of the holes. In this study, the concentration of impurities in the N-region was set to approximately \( 1 \times 10^{18} \) cm\(^{-3} \). Therefore, the diffusion length of minority carriers \( L_d = (kT\mu\tau/q)^{1/2} \) (where \( k \) is the Boltzmann constant, \( T \) is the absolute temperature, \( \mu \) is the minority carrier mobility, \( \tau \) is the minority carrier lifetime, and \( q \) is the elementary charge) is 15.8 \( \mu \)m from the empirical formula [23]. The \( W_b \) should be sufficiently shorter than \( L_d \), so we set \( W_b = 1.2 \) \( \mu \)m in consideration of the value of \( L_d \) and the layout rule.

**IV. PNBT DIODE CHARACTERISTICS**

Fig. 6 shows the \( I_d - V_g \) characteristics of the PNBT SOI-FET. \( V_t \) is controlled by channel impurity doping and is set to a near-zero voltage. It should be noted that the super-steep SS appears with a drain voltage \( V_d = 0.1 \) V and a body terminal voltage \( V_b > 1.0 \) V, even at a near-zero value of \( V_t \).

Fig. 7 shows the measured results of the PNBT diode (the same device used in Fig. 6). It can be seen that the sharp turn-on (\(< 0.1 \) mV/dec) characteristics also appear in the PNBT diode, and the reverse leakage current is \( 5 \times 10^{-8} \) A/\( \mu \)m. Although the leakage current is higher than that for the ULP diode [5], it is 1.5 times lower than the conventional MOS diode (with \( V_{t2} \) in Fig. 1(b)), which is promising for ultralow power rectification. Fig. 8 shows the expanded \( I - V \) plot of Fig. 7, in the region around the low input voltage of 50 mV. The device still exhibits sharp turn-on characteristics, with a turn-on voltage of 41.5 mV. The PNBT diode will therefore function as a rectifier at an ultralow input voltage. Fig. 9 shows the \( I - V \) characteristics with a body terminal current of \( I_b \). The PNBT diode requires \( V_b \), so it is difficult to realize a “cold-start” system. In practice, \( V_b \) should be boosted using a method such as charge pumping. However, when the magnitude of the input voltage is greater than \( \pm 0.1 \) V, \( I_b \) becomes smaller than the anode current. Although it is necessary to decrease \( V_b \) and \( I_b \) further, it is possible that power consumption at \( I_b \) will become lower than the anode power consumption.
In addition, the PNBT diode has the following features. Fig. 10 shows the $I - V$ characteristics of PNBT diodes with various values of $L_g$ and $W_g$. The super-steep SS appears in all of the structures; however, the current of the PNBT diode is non-zero at zero voltage, notably with the high value of $V_b$. Fig. 11 shows the enlarged view of the region near-zero voltage of the measured $I - V$ data of the PNBT diode from Fig. 10. It was confirmed that the voltage at zero current shifts to slightly above zero, because there is a slight current at the body terminal when the voltage between both terminals of the diode is zero. This is a specific characteristic of the PNBT diode. The size of the shift of the zero-current voltage decreases with $L_g$, or when $W_g$ increases. We assume that the super-steep SS characteristics and the voltage shift are influenced by the interaction between $L_g$, $W_g$, and other geometric parameters (e.g., the shape of the gate and the extended P-region into the source and drain regions). These factors require further research.

Fig. 12 shows the double-sweep-measured $I - V$ characteristics. The hysteresis width appears at $V_b = 1.0$ V, and the width increases at $V_b = 1.1$ V. In addition, the reverse current at $V_b = 1.1$ V is larger than the forward current. The PNBT device exhibits hysteresis because the channel potential is maintained by the accumulated carriers when the anode voltage sweeps from the on-state to the off-state [15]–[17]. The high $V_b$ induces a super-steep SS and high $I_{on}/I_{off}$ ratio; however, the $I_{on}/I_{off}$ ratio and hysteresis characteristics are connected through a “trade-off” relationship. The large reverse current poses a potential risk that the rectification performance could deteriorate. It is noted that the hysteresis width should be kept smaller than the input voltage, when designing practical circuits.

Table 1 shows a comparison of three new-concept devices intended for use as rectifiers for energy harvesting. For this comparison, we chose the new mechanism semiconductor
γ has super steep (2.9 mV/dec) characteristics. The curvature characteristics of conventional MOSFETs to a feedback mode and the PNBT SOI-FET shifts from the subthreshold characteristics of TFETs. While the average SS of TFETs is steep (30 mV/dec), SOI-FET is smaller than that of the N-channel heterojunction TFET, and the PNBT diode, but we did not include the ULP diode or other microelectromechanical system (MEMS) devices. It is a cost advantage that the PNBT diode requires over 41.5 mV to achieve sharp turn-on characteristics. In addition, it will be important to investigate the impact of illumination on hysteresis effects and the phenomenon of the slight voltage shift at zero current have been confirmed as specific characteristics that should be considered when designing practical circuits. The PNBT diode is considered a promising candidate for high-efficiency energy harvesting. However, for future study, investigating the potentially detrimental consequences of the hysteresis effects and measuring the AC characteristics of the PNBT diode is necessary. In addition, it will be important to investigate the impact of illumination on hysteresis effects and the effect of process, voltage, and temperature variations.

## V. CONCLUSION

In this study, for the first time, PNBT diode characteristics are reported and compared with those of conventional diodes. The results show a reverse leakage current that is 1.5 times lower compared to a conventional MOS diode and has sharp turn-on characteristics (even for the ultralow input voltage range of 50 mV). However, for this diode, the hysteresis effects and the phenomenon of the slight voltage shift at zero current have been confirmed as specific characteristics that should be considered when designing practical circuits. The PNBT diode is considered a promising candidate for high-efficiency energy harvesting. However, for future study, investigating the potentially detrimental consequences of the hysteresis effects and measuring the AC characteristics of the PNBT diode is necessary. In addition, it will be important to investigate the impact of illumination on hysteresis effects and the effect of process, voltage, and temperature variations.

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## REFERENCES


[8] Y. Khatami and K. Banerjee, “Double-sweep-measured I(V) characteristics, as shown in Fig. 8. We therefore used the ratio of forward current $I_F$ to reverse current $I_R$ at 50 mV. As a result, the $I_F/I_R$ ratio of the PNBT diode is higher than that of the backward tunnel diode in this case.

## TABLE 1. Comparison of various new concept devices for use as rectifiers for energy harvesting.

<table>
<thead>
<tr>
<th>Material</th>
<th>Heterostructure (InAs/AlSb/AlGaSb/GaSb)</th>
<th>Heterostructure (InAs/InP)</th>
<th>Silicon (SOI CMOS Process)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SS (mV/dec)</td>
<td>30 (Average) ($V_F = 0.3$ V)</td>
<td>2.9 (Minimum) ($V_F = 0.1$ V, $V_S = 1.2$ V)</td>
<td></td>
</tr>
<tr>
<td>Zero-Bias Curvature $\gamma$ ($V^{-1}$)</td>
<td>45</td>
<td>31 ($V_S = 1.2$ V)</td>
<td></td>
</tr>
<tr>
<td>$</td>
<td>I_F</td>
<td>/</td>
<td>I_R</td>
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* Calculated using the fitting model in [6].

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FIGURE 12. Double-sweep-measured $I$ (absolute value)–$V$ characteristics. Solid line: forward scan, dotted line: backward scan.


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