Analytical Calculation of Influence of Ferroelectric Properties on Electrical Characteristics Negative Capacitance Germanium FETs

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ABSTRACT Negative capacitance (NC) germanium (Ge) p-channel field effect transistors with different ferroelectric parameters are investigated by the analytical model. The channel surface potential amplification induced by the NC effect, which determines the subthreshold swing (SS) and the drain current $I_{DS}$ of the device, can be tuned by varying the thickness $t_{fe}$, the coercive field $E_{C}$, and the remnant polarization $P_{r}$ of the ferroelectric film. For the logic device, hysteresis phenomenon must be avoided, which is enabled by reducing $t_{fe}$ or $E_{C}$ of the ferroelectric film. Under the condition of $t_{fe} = 30$ nm, $E_{C} = 30$ KV/cm, and $P_{r} = 30 \mu$C/cm$^{2}$, NC Ge transistors display the superior SS and $I_{DS}$ compared to the baseline FETs.

INDEX TERMS Negative capacitance, FET, germanium, ferroelectric, hysteresis.

I. INTRODUCTION

With the continuous scaling of CMOS, the reduction of power consumption in integrated circuits is limited by the Boltzmann’s tranny, which precludes the conventional MOSFETs from achieving a sub-kT/q subthreshold swing (SS) [1]–[3]. The negative capacitance (NC) phenomena in the NCFETs have been extensively studied in silicon (Si) [4]–[7], germanium (Ge) [8], germanium-tin (GeSn) [9], and indium gallium arsenide (InGaAs) [10] channel FETs integrated with various ferroelectrics. The theoretical and experimental studies showed that the NC effect induced by ferroelectrics can improve the SS and drain current ($I_{DS}$) characteristics of the transistors, and the properties of the ferroelectric material played an important role in determining the electrical performance of the devices [11].

The previous theoretical study focused on the Si channel NC transistor. The exploration of NC Ge based transistors has been also very successful [9], [12], [13]. Recently, we reported the NC Ge pFETs, which demonstrated sub-60 mV/decade SS and the higher $I_{DS}$ over the control pMOSFETs [8]. Nevertheless, the undesirable hysteresis induced by the polarization switching of ferroelectric film was also observed in NC Ge pFETs. The NC Ge pFETs exhibited the significant peak in the gate capacitance $C_{G}$ as function of gate voltage $V_{GS}$ curves and the negative differential resistance in the $I_{DS}$ versus $V_{DS}$ curves, which are well consistent with the theoretical results [14]–[19]. In NC transistors, the matching between the capacitance induced by ferroelectric film $C_{fe}$ and the MOS capacitance $C_{MOS}$ is the crucial factor affecting the device performance. Currently, there is still a lack of a detailed study on the impacts of the parameters of ferroelectric, determining the matching between $C_{fe}$ and $C_{MOS}$, and on the performance of NC Ge transistors.

In this paper, we comprehensively study the influence of ferroelectric material properties, including thickness $t_{fe}$, coercive field $E_{C}$, and remnant polarization $P_{r}$, on the electrical characteristics of the NC Ge pFETs utilizing the analytical model. It is demonstrated that, through optimizing design of the ferroelectric properties, improved $I_{DS}$ and SS over...
the baseline device are achieved in the hysteresis-free NC transistor.

II. DEVICE STRUCTURE AND ANALYTICAL MODEL APPROACH

Fig. 1(a) illustrates the schematic diagram of the NC Ge pFET investigated in this work. In our calculation, we use Ge (001) substrate with a n-type carrier concentration of $10^{18}$ cm$^{-3}$. HfO$_2$ is used as the insulator dielectric with an EOT of 1.2 nm. The workfunction of internal and top gates is 4.7 eV. The internal gate layer can average out the potential profile along the channel as well as any charge non-uniformity coming from the domain formation in the ferroelectric film, and thus we can use one-dimensional Landau-Ginzburg-Devonshire’s (LGD) theory to describe the action of FE material in the NC Ge pFET [20], [21]. It is noted that the NC transistors with and without the internal gate have the similar performance, except for the strong inversion region [22]. Fig. 1(b) presents the simplified equivalent capacitance model of the NC Ge pFET.

The series combination of $C_{ox}$ and $C_s$ is referred to the $C_{MOS}$, and the matching between $C_{fe}$ and $C_{MOS}$ determines the electrical performance of the NC device.

As $V_{GS}$ is applied to the top gate of the NC Ge pFET, we have a relation of $V_{GS} = V_{FB} - \phi_s = V_{fe}$, where $V_{FB}$ is the flatband voltage of the underlying MOS capacitor, $\phi_s$ is the channel surface potential, the relation between $\phi_s$ and the channel charge $Q_i$ per unit area can be expressed as [23]:

$$Q_i = \pm \sqrt{2\varepsilon_s kTn_i d} \left[ \left( e^{\frac{\phi_s}{kT}} + \frac{q\phi_s}{kT} - 1 \right) + \frac{n_i^2}{N_d^2} \left( e^{\frac{\phi_s}{kT}} (e^{\frac{\phi_s}{kT}} - 1) - \frac{q\phi_s}{kT} \right) \right]^{1/2},$$

(1)

where, $\varepsilon_s$ is the permittivity of the semiconductor, q is the electron charge, $n_i$ is the intrinsic carrier concentration, $N_d$ is the substrate doping, $V$ is the quasi-Fermi potential at a point in the channel, and $V_{fe}$ is the voltage drop across the ferroelectric insulator. According to the LGD theory, for a given $t_{fe}$, $V_{fe}$ is expressed by

$$V_{fe} = 2t_{fe}\alpha_0 P + 4t_{fe}\beta_0 P^3,$$

(2)

where, $\alpha_0$ and $\beta_0$ are the anisotropy constants, and $P$ is the polarization charge per unit area in ferroelectric layer. $\alpha_0$ and $\beta_0$ are calculated by [11]

$$\alpha_0 = -3\sqrt{3}/4 \times E_c/P_r,$$

(3)

and

$$\beta_0 = -3\sqrt{3}/8 \times E_c/P_r^3,$$

(4)

respectively. $I_{DS}$ of the NC Ge pFETs can be calculated using the Pao-Sah formula [23]:

$$I_{DS} = \mu_{eff} \frac{W}{L} \int_{V_F}^{V_D} (-Q_i(V)) dV,$$

(5)

where, $\mu_{eff}$ is the effective hole mobility, which is assumed as 300 cm$^2$/Vs and $V$ is the quasi-Fermi potential at a point in the channel. Since the polarization in a ferroelectric film is very large, $Q_i$ is approximately equal to $P$. W and L are the channel width and length, respectively, which are 1 $\mu$m and 250 nm, respectively. With the development of surface passivation of Ge, the density of states $D_{it}$ at Ge/high-k interface can be reduced to be about $10^{11}$ eV$^{-1}$cm$^{-2}$ at an equivalent oxide thickness of 0.7 nm, so the impact of $D_{it}$ on device performance is not considered [24].

III. RESULTS AND DISCUSSION

By coupling the relation between $V_{fe}$ and $\phi_s$ to the $Q_i$ and $P$ of the semiconductor and ferroelectric capacitor through Eqs. (1) and (2), $Q_i$ can be solved for a given $V_{GS}$. Then, $\phi_s$ the can be obtained from Eq. (1). Fig. 2(a) shows the curves of $\phi_s$ as a function of $V_{GS}$ for the NC Ge transistors with $P_i = 12\mu C/cm^2$, $E_c = 30$ KV/cm, and $\Delta\phi = 0$. $t_{fe}$ varies from 0 to 100 nm. These values of $P_i$ and $E_c$ are similar to those of perovskite ferroelectric materials such as BaTiO$^3$ [23], SBT [28], and Pb(Zr$_{1-x}$Ti$_x$)O$^3$ [21]. It can be seen that with a $t_{fe} \leq 30$ nm, the correspondence between $\phi_s$ and $V_{GS}$ is single valued function, and it becomes multi-valued in the case of $t_{fe} > 30$ nm. The gate voltage amplification fraction $G$, defined as $d\phi_s/dV_{GS}$, gets reduced as $t_{fe}$ decreases, which can be observed from Fig. 2(b). This indicates that the boosting effect of negative capacitance decreases with decreasing $t_{fe}$. The maximum value of $G$ is 5.8 with a $t_{fe}$ of 30 nm. Later, we will show that, as the $t_{fe}$ is larger than 30 nm, hysteresis in $I_{DS} - V_{GS}$ curves will occur.

Calculations with compact models showed that the significant peaks in $C_G - V_{GS}$ curves are the typical characteristics of the NC transistors [15], [19]. In order to investigate the impact of $t_{fe}$ on $C_G$ in NC Ge pFETs, $C_G$ versus $V_{GS}$ curves for several values of $t_{fe}$ are plotted, as shown in Fig. 3. From the simplified capacitance model of the NC device, we know that $C_G$ is equal to $C_{fe} \times C_{MOS}/(C_{MOS} + C_{fe})$, the peak will appear only if $C_{fe}$ is negative and its magnitude is greater than or approximately equal to the magnitude of $C_{MOS}$. Furthermore, we have experimentally demonstrated that $I_{DS}$ of the NC transistor can be enhanced as the $C_G$ peak gets increased in [25].
Inset of Fig. 3 illustrates that the peak of $C_G$ increases with $t_{fe}$ varies from 10 to 30 nm. The peak of $C_G$ is indicative of the large gain of the devices. Generally, there are two methods to verify the existence of NC effect in the device. One is to measure the $C_G$ of the transistor and a peak in the $C_G$ vs. $V_{GS}$ curve is the signature of the NC effect. The other is to measure the $I_{DS}$ vs. $V_{GS}$ curves and extract the SS, which can be calculated by

$$SS = \frac{\partial V_{GS}}{\partial \left( \log I_{DS} \right)} = \frac{kT}{q} \ln 10 \left( 1 + \frac{C_s}{C_{ox}} + \frac{C_s}{C_{fe}} \right).$$

(6)

Based on Eq. (6), SS less than 60 mV/decade can be achieved as $C_{fe}$ is negative and its magnitude is greater than $C_{ox}$. Fig. 4(a) illustrates the transfer characteristics of the NC Ge pFETs with the different $t_{fe}$. It is clear to see that, when the $t_{fe}$ is smaller than 30 nm, there is no hysteresis phenomenon occurring. The appearing of the multi-valued function in the $\phi_s - V_{GS}$ curves produces the hysteresis in $I_{DS} - V_{GS}$ curves. Fig. 4(b) compares the $I_{DS}$ of the NC devices with the different $t_{fe}$ at $V_{GS} - V_{TH} = V_{DS} = -0.25$ V. Here, $V_{TH}$ is defined as the $V_{GS}$ at $I_{DS}$ of $10^{-6}$ A/$\mu$m. For the forward sweeping of $V_{GS}$, $I_{DS}$ of the devices increases with $t_{fe}$. While for the reverse sweeping, maximum $I_{DS}$ is obtained at a $t_{fe}$ of 80 nm. With a $t_{fe}$ of 30 nm, an $I_{DS}$ of 0.35 mA/$\mu$m at $V_{GS} - V_{TH} = V_{DS} = -0.25$ V, and a steep SS of 37 mV/decade is achieved. It is noted that the steep SS of the devices, which is the evidence of NC effect, appears at the same $V_{GS}$ value where the $C_G$ peaks (Fig. 3) and the maximum $G$ are observed [Fig. 2(b)]. According to the experimental work in [25], the NC device exhibits the peaks in $C_G - V_G$ curves with the forward and reverse sweeping of $V_{GS}$, showing the significantly higher magnitude of $C_G$ compared to the control transistor, which is due to the NC effect. NC transistors with the greater $C_G$ peak obtain the higher $I_{DS}$, which proves that the NC effect promotes the performance improvement of the device. It is noted that these results are well consistent with our simulation.

In addition to the $t_{fe}$, we also investigate the effect of the $E_c$ of ferroelectric film on the device performance. Fig. 5(a) and (b) present the $\phi_s$ vs. $V_{GS}$ and $G$ vs. $V_{GS}$ curves, respectively, for different values of $E_c$ with a $t_{fe}$ of 30 nm and a $P_r$ of 12 $\mu$C/cm$^2$. The ferroelectric film with $E_c > 30$ KV/cm gives rise to the hysteresis behavior, i.e., $\phi_s - V_{GS}$
curves become multi-valued function of $V_{GS}$. From Fig. 5(b), we can see that the $G$ gets reduced as $E_c$ decreases, which manifests that the boosting effect of $C_{fe}$ decreases with the reduction of $E_c$.

Fig. 6 plots the $C_G$ versus $V_{GS}$ of NC transistors with different $E_c$ under the condition of hysteresis free. The significant $C_G$ peaks are also observed, which is indicative of the NC effect and the channel surface potential gain of the NC Ge pFETs. $I_{DS} - V_{GS}$ characteristics of the NC Ge pFETs with different $E_c$ at $V_{GS} - V_{TH} = V_{DS} = -0.25$ V. It is observed that, for both forward and reverse sweeping of $V_{GS}$, $I_{DS}$ of the device increases with $E_c$. With an $E_c$ of 30 KV/cm, a $I_{DS}$ of 0.32 mA/μm at $V_{GS} - V_{TH} = V_{DS} = -0.25$ V, and a steep SS of 37.7 mV/decade are achieved.

We also investigate the dependence of NC Ge pFETs on the values of $P_r$ of the ferroelectric film, which varies from 12 to 50 μC/cm², and $t_{fe}$ and $E_c$ are 30 nm and 30 KV/cm, respectively. Fig. 8(a) shows the $\phi_s$ as a function of $V_{GS}$ curves of the NC Ge transistors with the various values of $P_r$. The relationships between $G$ and $V_{GS}$ with different $P_r$ are shown in Fig. 8(b), which show that the $G$ increases with $P_r$ rapidly. In other words, the boosting effect of $C_{fe}$ increases with $P_r$.

Fig. 9 shows the calculated $C_G$ versus $V_{GS}$ curves of the NC devices with different values of $P_r$. The peaked $C_G - V_{GS}$ characteristics indicate a large gain, which becomes smaller with decreasing $P_r$. The transfer characteristics of the NC Ge pFETs are presented in Fig. 10(a). No hysteresis
FIGURE 9. Influence of \( P_r \) on \( C_{G} - V_{GS} \) characteristics. Inset shows that the peak \( C_{G} \) increases with \( P_r \).

FIGURE 10. (a) Influence of \( P_r \) on \( I_{DS} - V_{GS} \) characteristics of the NC Ge pFETs. (b) \( I_{DS} \) for the NC Ge transistors with different \( P_r \) at \( V_{GS} - V_{TH} = V_{DS} = -0.25 \) V. (c) Point SS versus \( V_{GS} \) characteristics of the NC device with \( P_r \) varies from 12 to 50 \( \mu \)C/cm\(^2\). Steep SS less than 60 mV/decade is achieved at all conditions.

FIGURE 11. Evolution of \( P - V \) characteristics of ferroelectric materials with the variation in (a) \( t_{fe} \), (b) \( E_c \), and (c) \( P_r \). It is clearly to observe the NC effect with the variation of the ferroelectric properties.

phenomenon is observed. The single valued function in the \( \phi_0 - V_{GS} \) curves indicates the hysteresis free in the \( I_{DS} - V_{GS} \) curves. The \( I_{DS} \) of the NC Ge pFETs increases with \( P_r \) at \( V_{GS} - V_{TH} = V_{DS} = -0.25 \) V, as illustrated in Fig. 10(b). From Fig. 10(c), it is found that the SS decrease from 41 to 37 mV/decade with \( P_r \) changing from 12 to 50 \( \mu \)C/cm\(^2\).

According to the above discussion, we know that the hysteresis window of the \( I_{DS} - V_{GS} \) curves of the NC Ge pFETs increases with the values of \( t_{fe} \) and \( E_c \) of the ferroelectric film. And the hysteresis-free can be obtained by increasing the \( P_r \) of ferroelectric film. It was experimentally demonstrated that, the hysteresis of the NC Ge transistors can be reduced by modulating the ferroelectric properties of \( P_r \) and \( E_c \) \cite{12}, which is consistent with our simulation results. As the ferroelectric material exhibits a significant increasing in the ratio of \( P_r \) to \( E_c \), which results in the improvement of the magnitude of ferroelectric NC \( C_{FE} \), leading to the reduction of hysteresis of the ferroelectric NC Ge transistors \cite{12}.

Based on Eq. (2), \( C_{fe} \) can be expressed as

\[
C_{fe} = \frac{dP}{dV_{fe}} = 2\alpha_0 t_{fe} + \frac{12\beta_0 t_{fe}}{P_r^2},
\]

where, the linear term is negative, which dominates the negative capacitance when \( V_{GS} \) is very small \cite{27}. However, as \( V_{GS} \) increases to a certain value, the non-linear term becomes significant and cannot be neglected. Here, we summarize the impacts of \( t_{fe} \), \( E_c \), and \( P_r \) on the \( P - V \) loops of the ferroelectric materials in Fig. 11. The negative slope segment of the \( P-V \) diagram is unstable and exhibits the hysteretic jump in charge \cite{28}. Fig. 11(a) shows the \( P - V \) plots of the ferroelectric materials with different \( t_{fe} \). The peak effect is apparent with a \( t_{fe} \) of 30 nm. From Figs. 4(a) and 2(b), we cannot see the hysteresis in the transfer characteristics but the device obtains the \( G >> 1 \). It proves that if the \( C_{fe} \) is placed in series with the positive capacitor \( C_{MOS} \), the NC effect can be effectively stabilized, which agrees well with the results reported in \cite{5}. This phenomenon can also be observed from the dependence of NC Ge pFETs on \( E_c \) and \( P_r \) of the ferroelectric materials \cite{11}.

In the small range of \( V_{GS} \), the \( Q_1 \) is small and the nonlinear term can be neglected, and then the \( C_{fe} \) can be approximated as \cite{11}

\[
C_{fe} \approx \frac{dP}{dV_{fe}} = \frac{2 P_r}{3\sqrt{3} E_c t_{fe}^2}.
\]
Here, we summarize the $I_{DS}$ of the NC Ge pFETs as a function of $C_G$ with different $t_{fe}$, $E_c$, and $P_f$ in Fig. 12. Note that the enhancement of $C_G$ and $I_{DS}$ can be achieved simultaneously with the increased $t_{fe}$, $E_c$, and $P_f$. Therefore, the large peak $C_G$ can be increased with $t_{fe}$, $E_c$, and $P_f$ of the ferroelectric film. In the meanwhile, we find that the increase of $P_f$ of the ferroelectric material can effectively reduce the hysteresis, but its ability to increase the $I_{DS}$ is restricted compared to the $t_{fe}$ and $E_c$ of the ferroelectric film. However, increasing the $t_{fe}$ and $E_c$ of the FE layer of the NC Ge pFETs arbitrarily will make the hysteresis phenomena become seriously. Therefore, there is a trade-off between enhancing the $I_{DS}$ and suppressing the hysteresis of the NC Ge pFETs.

IV. CONCLUSION

In this paper, the influence of $t_{fe}$, $P_f$, and $E_c$ of the ferroelectric materials properties on the electrical characteristics of the NC Ge pFETs is studied using analytical model. We compare the $I_{DS}$ versus $C_G$ characteristics of the NC Ge pFETs with different $t_{fe}$, $E_c$, and $P_f$. Based on this, a guideline for designing high performance NC Ge pFETs based on the ferroelectric material is presented. Under the condition of $t_{fe} = 30$ nm, $E_c = 30$ KV/cm, and $P_f = 30$ μC/cm², the NC Ge pFETs can obtain the superior electrical properties compared to the baseline FETs, in terms of SS, the value of $I_{DS}$, and hysteresis.

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