Enhanced Hole Injection into Single Layer WSe₂

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Abstract—Electronic devices with light-emitting regions comprised of single layer transition metal dichalcogenides, such as tungsten diselenide (WSe₂), are of great interest due to the formation of a direct bandgap at the single layer limit. Furthermore, increasing injected hole current into the single layer WSe₂ is of great importance due to the resulting increase in electroluminescence. In this work, we demonstrate a 1000x increase in injected hole current into the channel region of a FET comprised of a single layer WSe₂ channel by incorporation of a thicker (20-30nm) multilayer WSe₂ film under the metal source contact only. By fabrication and analysis of FETs comprised of single layer, bi-layer, and tri-layer WSe₂ channel regions, we correlate the increase in injected hole current to a decrease in the hole Schottky barrier height at the source contact due to incorporation of the multilayer WSe₂ film.

Index Terms— WSe₂, field-effect transistor, hole injection, Schottky barrier, single layer

I. INTRODUCTION

Electroluminescence (EL) from single layer TMDs, e.g., MoS₂, WS₂, WSe₂, and MoS₂/WSe₂ heterostructures is an active area of research [1]-[6]. The interest in single layer (1L) TMDs is due to the formation of a direct bandgap at the single layer limit [7]. Increased EL can be obtained by increasing the electron and hole current injection into the 1L direct bandgap TMDs. A previous report demonstrates the ability to increase electron current into 1L MoS₂ by thickness modulation [8]. In this work, we focus on WSe₂ because of its superior optical quality compared to MoS₂, air-stability, and its ambipolar characteristics allowing for the simultaneous study of both electron and hole injection as opposed to only electron injection in n-type MoS₂ [6], [9], [10]. Utilizing back-gated FET structures, we investigate increased hole injection by thickness modulation into thin WSe₂ channel regions as an analogue to the increased electron injection in MoS₂ by the same method. The ability to increase both hole (electron) current into 1L WSe₂ (1L MoS₂) allows for the ability to form improved p-n junction heterostructures made of thickness modulated WSe₂ and MoS₂ for increased EL.

Carrier injection into WSe₂ is poor due to the Schottky barrier (SB) that forms between metal (source/drain (S/D)) contacts and intrinsically low-doped WSe₂. In addition to low doping, the electronic bandgap of WSe₂, and thus the SB at the source contact, increases with decreasing thickness, further worsening the injection of hole current into a channel region comprised of single layer WSe₂ [11]. In order to achieve efficient EL in an electronic device with a 1L WSe₂, electrons and holes must be readily injected into the 1L channel, by achievement of a S/D contact with low SB height and thus low contact resistance (R_C).

Fig. 1. (a) Optical image showing contrast between thin, e.g. single layer (1L), and multilayer (ML) WSe₂ flakes. (b) AFM scan of a thin-ML WSe₂ FET; scale bar is 5um. (c) Schematic cross section of thin-ML WSe₂ FET showing the four different 2-point probe conducting paths A, B, C, and D.
In this letter, we first demonstrate a 1000x increase in injected hole current into a single layer WSe$_2$ channel region by incorporation of a thicker (20-30nm) multilayer (ML) WSe$_2$ film between the metal source contact and single layer WSe$_2$ channel region. Second, by fabrication and analysis of FETs comprised of single layer (1L), bi-layer (2L), and tri-layer (3L) WSe$_2$ channel regions, we correlate the increase in injected hole current to a decrease in the hole SB height at the source contact due to incorporation of the multilayer WSe$_2$ film. Third, we correlate the decrease in hole SB height to a decrease in $R_C$.

II. DEVICE FABRICATION AND MEASUREMENTS

Devices were fabricated on a heavily doped n-type silicon substrate (0.001–0.005 Ω-cm) serving as the back gate. 285 nm of SiO$_2$ was thermally grown on the wafer to form the gate dielectric, followed by exfoliation of WSe$_2$ flakes (from 2D Semiconductors) on the SiO$_2$. Single (1L), bi (2L), and tri-layer (3L) WSe$_2$ flakes, attached to ML flakes, were then selected on the wafer via optical contrast and verified by measuring the photoluminescence (PL) spectrum. An optical image of a 1L WSe$_2$ flake attached to a ML WSe$_2$ flake is shown in Fig. 1(a). Contact regions were formed by e-beam lithography of the contact patterns, deposition of 8 nm / 50 nm of Ni / Au metal (or 4nm / 50nm Ti / Au metal) using a thermal evaporator, and lift-off. Fig. 1(b) shows an AFM scan (top view) of a FET utilized in this work, with four contacts (1, 2, 3, and 4). The four contact regions enable 2-point probe measurements of different conduction paths associated with thin and ML WSe$_2$, as shown in Fig 1(c). Fig. 2(a) shows the PL spectrum (at 300K) of the 1L and ML region from a device in this work. PL is measured before metal contact patterning; thus, the flakes are unbiased during the PL measurement. The PL spectrum is consistent with Kim et al. [12].

$I_D$-$V_G$ characteristics were measured for the FET structure in Fig. 1(b), for each of the paths in Fig 1(c). Fig. 3 shows $I_D$-$V_G$ characteristics for Devices 1, 2, 3 with Ni / Au contacts, for paths B and C ($I_D$-$V_G$ characteristics for Device 1 are also shown for paths A and D). The thin WSe$_2$ layers for Device 1, 2, and 3 are 1L, 2L, and 3L, respectively. A 4-point probe (4PP) measurement [13], [14] was performed on WSe$_2$ flakes of varying thickness to extract $R_C$. A schematic of the measurement technique and cross section of the 4PP device is shown in Fig 2(b). In the 4PP measurement, a fixed current is forced through the outer two probes and a voltage is measured across the inner two probes. $R_C$ is extracted from the measured voltage associated with the forced current as in [14]. The extracted $R_C$ for varying WSe$_2$ thicknesses is shown in Fig. 4(a). $I_D$-$V_D$ characteristics were measured to evaluate injection at $V_G > 0$V, and rectification at $V_G < 0$V, as shown in Figs. 4(b) and (c), with $V_D$ applied to contact 2 while contact 3 is grounded.

Fig. 5 shows the temperature dependence of the $I_D$-$V_G$ characteristics for paths B and C, for a thin-ML device with Ni / Au contacts, to identify the current injection mechanisms. Fig 6(a) shows $I_D$-$V_G$ characteristics for a thin-ML device with Ti / Au contacts (for comparison to devices with Ni / Au contacts); Fig 6(b) shows the corresponding temperature dependence of the $I_{DP}$-$V_{DP}$ characteristics for paths B and C, for the same device in Fig. 6(a).

III. RESULTS AND DISCUSSION

In this section, we first focus on devices fabricated with Ni / Au contacts. From $I_D$-$V_G$ characteristics for paths A and D of Device 1 (Fig. 3), it is noted that both the hole ($V_G < 0$V) and electron ($V_G > 0$V) currents for ML WSe$_2$ are larger than for 1L WSe$_2$. This result is as expected because ML and 1L WSe$_2$ have a type-I band alignment (with 1L WSe$_2$ having the larger bandgap) [15], leading to larger electron and hole SBs for 1L, compared to ML, WSe$_2$. From Fig. 3, thin (1L, 2L, or 3L)-ML devices 1, 2, 3 show ambipolar characteristics enabling analysis of both electron and hole Schottky barriers.

Electron current ($V_G > 0$V) is the same for conduction paths B and C, independent of WSe$_2$ channel layer thickness, as shown in Fig. 3. Symmetrical (equal) electron injection is also observed, e.g. for Device 1, from its $I_D$-$V_D$ characteristics (with $V_G > 0$V), as shown in Fig. 4(b). Injected electron current also has negligible temperature dependence as shown in Fig. 5; this indicates that electron current primarily occurs by tunneling through a SB, rather than by thermionic emission over a SB. We note that the tunneling electron current in paths B and C is limited by the SB on the thin WSe$_2$ side, for the Ni / Au contacts, independent of whether or not the SB on the thin WSe$_2$ is forward or reverse biased.

In contrast, hole current ($V_G < 0$V) is significantly different for paths B and C, with the hole current for path C increasing with WSe$_2$ layer thickness, 1L, 2L, to 3L, as shown in Fig 3. Asymmetrical hole injection is observed, e.g. for Device 1, from its $I_D$-$V_D$ characteristics (with $V_G < 0$V), as shown in Fig. 4(c). Furthermore, unlike the injected electron current, the injected hole current has a strong temperature dependence as
shown in Fig. 5; the decreasing hole current with decreasing temperature indicates that hole current primarily occurs by thermionic emission over a SB, rather than by tunneling through a SB.

Injected hole current could increase with increasing WSe$_2$ thickness for two reasons: (1) hole SB decreases with increasing WSe$_2$ thickness, or (2) lateral access resistance associated with hole flow decreases with increasing WSe$_2$ thickness. We conclude that mechanism (1) is correct from the following argument. It is recognized that the source and drain resistances (including contact resistance associated with the SBs, and lateral access resistance) are in series; however, the drain (non-injecting hole contact) SB is forward biased, and the other reverse biased. With decreasing WSe$_2$ thickness, we find that the increasing magnitude of the reverse biased “hole injection SB” is reduced. It is noted that the reverse biased source contact is due to incorporation of the ML WSe$_2$ film. A large change in the hole Schottky barrier with decreasing WSe$_2$ thickness is consistent with Prakash et al. [16].

From our analysis of FETs comprised of 1L, 2L, and 3L WSe$_2$ channel regions, we correlate the increase in injected hole current to a decrease in the hole Schottky barrier height at the source contact due to incorporation of the ML WSe$_2$ film. A large change in the hole Schottky barrier with decreasing WSe$_2$ thickness is consistent with Prakash et al. [16].

A Schottky barrier FET (SB-FET), as in this study, consists of two Schottky barriers (at S and D). With an applied $V_{DS}$, one of the hole SBs is forward biased, and the other reverse biased. A large $V_{D}$ of 1V is applied during $I_{D}-V_{G}$ measurements so that the value of $R_C$ from the forward biased hole SB is negligible. With decreasing WSe$_2$ thickness, it is the increasing magnitude of the reverse biased “hole injection SB” that limits the hole current into the thin WSe$_2$ channel without the use of ML WSe$_2$ at the hole injecting contact. By first injecting holes into the ML WSe$_2$, and then from the ML WSe$_2$ into the thin WSe$_2$ channel, the metal-WSe$_2$ “hole injection SB” is reduced. It is noted that the hole current of path D is similar to the hole current of path B (e.g. see $I_{D}-V_{G}$ characteristics for Device 1 in Fig. 3). Therefore, even with the valence band offset (due to the different bandgaps) between thin and ML WSe$_2$, this reduction in metal-WSe$_2$ SB allows for much larger hole injection current.

It is expected that the extracted $R_C$ from 4PP measurements...
should be consistent with the results in Fig. 3. Fig. 4(a) shows

![Graph showing temperature dependence of I_DRAIN vs. V_GATE for Ni/Au contacts.]

referring to Fig. 1(c), we denote \( \Phi_{\text{eff}, B} \) (or \( \Phi_{\text{eff}, \text{thin}} \)) as the effective Schottky barrier height associated with the metal/thin WSe\(_2\) layer (either 1L, 2L, or 3L), and \( \Phi_{\text{eff}, C} \) (or \( \Phi_{\text{eff}, \text{ML}} \)) as the effective Schottky barrier height associated with the metal/ML WSe\(_2\). We define \( \Delta \Phi_{\text{eff}} \) as \( (\Phi_{\text{eff}, \text{ML}} - \Phi_{\text{eff}, \text{thin}}) \) (or similarly, \( (\Phi_{\text{eff}, C} - \Phi_{\text{eff}, B}) \)) such that \( \Delta \Phi_{\text{eff}} = kT \ln(I_B/I_C) \), where \( I_B (I_C) \) is the hole current for path B (C) at the same back-gate bias \( V_G \) (\( V_G - V_{T, \text{holes}} = -15V \)) as was used when plotting \( R_C \). Fig. 4(a) shows that \( \Delta \Phi_{\text{eff}} \) is a maximum for 1L-ML thickness modulated WSe\(_2\) and decreases for 2L-ML and 3L-ML cases. This is consistent with the decrease in hole SB \( R_C \) and decrease in bandgap with increasing thickness, thus decreasing the difference in hole SB height between metal/thin WSe\(_2\) and metal/ML WSe\(_2\) for increasing thickness of the thin WSe\(_2\). Finally, we investigate devices with Ti / Au contacts, for which Ti has a lower work function versus Ni. From Fig. 6(a), we observe that for Ti / Au contacts, hole current is increased for path B versus path C (similar to the case of Ni / Au contacts, as in Fig. 3). In contrast, for Ti / Au contacts, electron current is increased for path C versus path B (unlike the case of Ni / Au contacts, as in Fig. 3). This result demonstrates that for Ti / Au contacts, electron injection through the thin WSe\(_2\) channel is increased when first injecting electrons from the Ti / Au metal into the ML WSe\(_2\) and then into the thin channel layer. The increase of both electron and hole injection due to the ML WSe\(_2\) is in agreement with the type-I band alignment of 1L-ML (with 1L WSe\(_2\) having the larger bandgap). Fig 6(b) shows both decreasing electron and hole current with decreasing temperature, for the case of Ti / Au contacts. This result, along with temperature dependent hole current (associated with thermionic emission) for the case of Ni / Au contacts in Fig. 5, further corroborates our explanation that that increased current, either hole or electron, due to the use of ML WSe\(_2\), is a result of a lower SB for ML WSe\(_2\) compared to the SB for thin (i.e. 1L, 2L and 3L) WSe\(_2\).

**IV. CONCLUSION**

In conclusion, this work presents a method to increase hole injection into thin WSe\(_2\), most importantly 1L WSe\(_2\), by using multilayer WSe\(_2\) underneath the source (hole injecting) contact, while keeping the channel as a single WSe\(_2\) layer. We demonstrate a 1000x increase in injected hole current into the channel region of a FET comprised of a single layer WSe\(_2\) channel by incorporation of a thicker (20-30nm) multilayer WSe\(_2\) film under the metal source contact only. We conclude that the increase in injected hole current is due to the multilayer WSe\(_2\) reducing the reverse biased “hole injection Schottky barrier”. The 4PP contact resistance measurements support this by showing that \( R_C \) associated with a FET having...
multilayer WSe$_2$ under the metal contacts can be on the order of 1000x smaller versus only having a single layer WSe$_2$ under the metal contacts. An increase in hole injection into single layer WSe$_2$ can help enhance the electroluminescence and improve light emitting devices made from WSe$_2$ or p-n junctions made from WSe$_2$/MoS$_2$ heterostructures. For future work, it is suggested to construct a thickness modulated WSe$_2$/MoS$_2$ p-n junction heterostructure for increased light emission utilizing the improved electron injection in thickness modulated MoS$_2$ as reported by Sun et al. [8] and the increased hole injection into WSe$_2$ as reported in this work.

REFERENCES