High-mobility and H₂-anneal Tolerant InGaSiO/InGaZnO/InGaSiO Double Hetero Channel Thin Film Transistor for Si-LSI Compatible Process

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Abstract—We demonstrate a high-mobility and H₂-anneal tolerant InGaSiO/InGaZnO/InGaSiO double heterochannel (DH) thin film transistor (TFT) for 3D integration with Si CMOS-LSI applications. A novel oxide semiconductor (OS) material, InGaSiO (Si/In ratio > 0.47) was found to exhibit semiconductor property even after H₂ annealing at 380°C, whereas a conventional InGaZnO layer changed into a metallic one. Moreover, the DH channel TFT was operated in an enhancement mode and achieved a high mobility of 30 cm²/Vs after the H₂ annealing. The proposed DH channel TFT has a potential as a high-performance Back end of line (BEOL) transistor with Si-CMOS process compatibility.

Index Terms—oxide semiconductor, thermal stability, mobility, and BEOL transistor, double heterochannel.

I. INTRODUCTION

RECENTLY, wide-bandgap oxide semiconductor (OS) TFTs have attracted attention as BEOL transistors for 3D integration with Si-CMOS LSI applications because of their unique characteristics i.e., extremely low off-state current (<10⁻²²A/µm), high breakdown voltage (V BD > 40V) and low-temperature process (<400°C). Consequently, the various applications, such as high voltage I/O switches and embedded memory, have been intensively investigated [1-5]. However, the thermal instability of OS materials caused by oxygen vacancy (V o) formation during H₂ annealing [6, 7] is an obstacle to integration with Si-CMOS LSIs. Moreover, typical OS channel InGaZnO shows low mobility (~10 cm²/Vs), which limits the applications of OS TFTs by its relatively low current drive. Although higher mobility values have been reported for other OS materials [8, 9], the stability against the H₂ annealing is still not clear.

In this paper, a newly developed OS material, InGaSiO (Si/In ratio > 0.47) was found to show stable high resistivity (>1x10¹⁰ Ω/sq.) against H₂ annealing, and the InGaSiO TFTs showed an enhancement mode operation after the H₂ annealing at 380°C. Furthermore, for the first time, we demonstrate the improvement of mobility up to 30 cm²/Vs and thermal stability.

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Fig.1 (a) Concept of the improvement of H₂-anneal tolerance and (b) list of metal-oxygen bond dissociation energy of InGaZnO related metals and Si [7]. Since the Si-O bond exhibits much larger dissociation energy than that of the Zn-O bond, replacing Zn atoms to Si atoms are expected to suppress oxygen vacancy formation during H₂ annealing.

III. OPTIMIZATION OF SI COMPOSITION & EVALUATION OF H₂-ANNEAL TOLERANCE

In order to proof our concept, we fabricated InGaSiO films having various Si fractions by co-sputtering with a polycrystalline InGaSiO target and a polycrystalline In₂O₃ target at room temperature in the mixed atmosphere of Ar and O₂. The InGaSiO target is conventional ceramic target and its composition is In:Ga:Si:O = 1:1:1:5. Figure 2 (a) and (b) show an In₂O₃ input RF power dependence of deposited InGaSiO film composition and film density, respectively, where the input RF power to the InGaSiO target was fixed at 400W. The deposited film was amorphous and the composition of deposited film was determined by RBS and ICP-mass spectroscopy measurements. The thickness of each deposited film was 100 nm. As shown in Fig.2(a), the Si/In ratio of the InGaSiO films was successfully controlled by changing the input RF power to the In₂O₃ target with a constant RF power to the InGaSiO target. Fig. 2(b) shows the density of deposited...
InGaSiO films increased with the increase of the input RF power to the In$_2$O$_3$ target.

The band structure of InGaSiO and its composition dependence were evaluated through the conduction energy minimum ($E_c$) and valence energy maximum ($E_v$) evaluation by X-ray photoemission spectroscopy (XPS) and ultra-violet photoemission spectroscopy (UPS), respectively. Figure 3 shows a obtained Si/In ratio dependence of $E_c$ and $E_v$. Although the $E_c$ and $E_v$ of InGaSiO with low Si fraction are comparable to that of InGaZnO, the bandgap energy of InGaSiO tends to increase with the increase of the Si/In ratio.

![Fig.2 In$_2$O$_3$ input power dependence of (a) InGaSiO film composition and (b) film density. The input RF power to the InGaSiO target was fixed at 400W. The Si/In ratio of the InGaSiO films was successfully controlled by changing the input RF power to the In$_2$O$_3$ target. O concentration was almost constant (61%).](image)

In order to evaluate H$_2$-anneal tolerance, the deposited OS films on high impedance glass substrate were annealed for 1 hour at various temperatures in N$_2$ and mixed atmosphere of N$_2$ and H$_2$ (2%), then the sheet resistance values were evaluated by resistance meter. Fig.4(a) and (b) shows the Annealing temperature dependence of sheet resistance of InGaSiO and InGaZnO film after annealing at (a) N$_2$ and (b) H$_2$ annealing for 1 hour. The sheet resistance of OS films decreased at lower temperature in H$_2$ annealing than in N$_2$ annealing. Although the sheet resistance of InGaZnO film decreases severely after annealing at 320°C in H$_2$, that of InGaSiO (Si/In ratio >0.47) keeps higher resistivity (>1x10$^8$Ω/sq.) even after H$_2$ annealing at 370°C, which suggests that InGaSiO maintains semiconductor properties.

![Fig.4 Annealing temperature dependence of sheet resistance of InGaSiO and InGaZnO film after annealing in (a) N$_2$ and (b) H$_2$ +N$_2$ annealing for 1 hour. The sheet resistance of OS films decreased at lower temperature in H$_2$ annealing than in N$_2$ annealing. Although the sheet resistance of InGaZnO film decreases severely after annealing at 320°C in H$_2$, that of InGaSiO (Si/In ratio >0.47) keeps higher resistivity (>1x10$^8$Ω/sq.) even after H$_2$ annealing at 370°C, which suggests that InGaSiO maintains semiconductor properties.](image)

InGaSiO films with high Si/In ratio (>0.32) are expected to maintain semiconductor properties and show higher H$_2$-anneal tolerance than that of conventional InGaZnO.

![Fig.5 Si/In ratio dependence of sheet resistance of InGaSiO film after H$_2$ annealing at 370°C. InGaSiO films with higher Si/In ratio (>0.32) are expected to maintain semiconductor properties and show higher H$_2$-anneal tolerance than that of conventional InGaZnO.](image)

IV. TFT FABRICATION & EVALUATION OF H$_2$-ANNEAL TOLERANCE

Figure 6 (a) and (b) shows TFT fabrication process and a TEM image of the fabricated OS TFT, respectively. A bottom-gated TFT is formed on a Si substrate. The gate electrode was MoTa. The thickness of the OS channel and the gate insulator was 25 nm and 40 nm, respectively. PE-CVD SiO$_2$ film was used for a gate insulator and an interlayer.
channel were fabricated by sputtering at room temperature. The maximum temperature throughout a TFT fabrication process was 350°C.

![TFT fabrication process](image)

Figure 6 shows the (a) TFT fabrication process and (b) cross-sectional TEM image of the fabricated TFT.

Figure 7 shows a comparison of $I_d$-$V_g$ characteristics between (a) InGaZnO TFT and (b) InGaSiO TFT (Si/In ratio =0.47) after the H$_2$ annealing. The channel length ($L$) and the channel width ($W$) are 2 μm and 2 μm, respectively. Although InGaZnO film changed into metallic property after H$_2$ annealing at 320°C as shown in Fig.4(b), InGaZnO TFT kept an enhancement mode operation up to 360°C. This indicates that an interlayer of SiO$_2$ in the TFT structure may suppress $V_o$ formation in InGaZnO channel by blocking oxygen outdiffusion from InGaZnO channel and improves the H$_2$-anneal tolerance in some degree. However, as shown in Fig. 7, only the InGaSiO TFT remained as enhancement mode while the InGaZnO TFT changed to depletion mode after the annealing at 380°C. The better stability against the H$_2$ annealing of the InGaSiO TFT is consistent with the results in Fig.4.

![Comparison of Id-Vg characteristics](image)

Figure 8 shows a Si/In ratio dependence of (a) threshold voltage, $V_{th}$ and (b) $I_{on}$ after H$_2$ annealing at 380°C. Here $V_{th}$ is $V_g$ at $I_d=1nA/μm$ and $I_{on}$ is $I_d$ at $V_g=20V$ and $V_d=1V$. There are a clear trade-off between the $V_{th}$ stability and high $I_{on}$ as a function of Si/In ratio. It is shown that higher Si fraction is effective to improve the thermal stability of InGaSiO, however, there is a trade-off between $I_{on}$ and thermal stability.

V. BREAKING THE TRADE-OFF BY INGaSiO/InGaZnO/InGaSiO DH TFTs

In order to improve both thermal stability and mobility, we examined a DH TFT composed of an InGaZnO core layer and thermally stable InGaSiO top/bottom barrier layers as shown in Fig.9. High H$_2$-anneal tolerant InGaSiO encapsulates high-mobility OS layer and can suppress $V_o$ formation in high-mobility core layer by blocking oxygen diffusion. Additionally, the conduction band offset of the proposed DH structure was 0.7eV as shown in Fig.3 and the band structure of the DH structure could be type-I quantum well. Since electrons are confined in the InGaZnO layer with higher mobility than the other, mobility improvement is expected by carrier separation from the SiO$_2$ interface via the InGaSiO barrier layers.

![Concept of improvement](image)

Figure 10 shows $I_d$-$V_g$ characteristics of the InGaSiO/InGaZnO/InGaSiO (5nm/10nm/2nm) DH TFT after...
H₂ annealing at 380°C. About two orders of magnitude higher $I_{on}$ was observed as expected than that of the InGaSiO TFT. Furthermore, the enhancement mode operation was maintained, suggesting that the InGaSiO barrier layers suppress dissociation of Zn-O bonds in the InGaZnO core layer via blocking oxygen diffusion out from the core layer.

Figure 11 shows effective electron mobility in the InGaZnO TFT and the DH TFT extracted by split CV method ($L/W=50 \mu m/50 \mu m$). Almost 3 times higher mobility ($\sim 30 \text{ cm}^2/\text{Vs}$) than that of the InGaZnO TFT, was realized at $N_s=2 \times 10^{12} \text{ cm}^{-2}$ in the DH TFT.

![Fig.11 Comparison of mobility between characteristics between InGaZnO and InGaSiO/InGaZnO/InGaSiO DH TFT extracted by split CV method. Almost 3 times higher mobility was realized in the proposed DH TFT.](image)

To further understand the mechanism of mobility improvement, we compared the mobility characteristics of hetero channel TFTs. Figure 12 shows the comparison of the mobility characteristics among InGaSiO/InGaZnO/InGaSiO (5nm/10nm/2nm), InGaSiO/InGaZnO (10nm/10nm) and InGaZnO/InGaSiO (10nm/10nm) TFTs. The peak mobility of InGaZnO/InGaSiO TFT (top InGaSiO case) was about 2.5 cm²/Vs and comparable with that of the InGaZnO single layer TFT, which means that carrier transports mainly in InGaZnO layer. However, the InGaSiO/InGaZnO TFT (bottom InGaSiO case) exhibits low mobility ($<0.8 \text{ cm}^2/\text{Vs}$) characteristics. These results indicates that when the bottom InGaSiO is relatively thick (10nm), carrier might transport both in InGaSiO (low mobility layer) and InGaZnO layer, which caused a mobility degradation as illustrated in Fig. 13(b). On the other hand, in the DH TFT with the thin bottom InGaSiO layer (5nm), the carrier confinement in InGaZnO layer and the carrier separation from the SiO₂ interface were successfully realized as we expected, which resulted in the mobility improvement (Fig. 13(c)).

![Fig.12 Comparison of the mobility characteristics among InGaSiO/InGaZnO/InGaSiO (5nm/10nm/2nm), InGaSiO/InGaZnO (10nm/10nm) and InGaZnO/InGaSiO (10nm/10nm) TFTs.](image)

Figure 13 shows a relationship between mobility (at $N_s=2 \times 10^{12} \text{ cm}^{-2}$) and H₂-anneal tolerance ($V_{th}$ after H₂ annealing at 380°C, $L/W=2 \mu m/2 \mu m$). It is shown that the proposed InGaSiO/InGaZnO DH TFT achieved both of better tolerance (stable enhancement mode operation) and higher mobility than those of InGaZnO and InGaSiO single-layer TFTs.

![Fig.13 Mechanism of mobility improvement in DH channel TFT. The insertion of thin bottom InGaSiO layer could confine the carrier in InGaZnO layer effectively and suppress the carrier scattering at SiO₂ interface, which results in mobility improvement.](image)
VI. CONCLUSION

We have developed a high-performance OS TFT with excellent H₂-anneal tolerance and high mobility for the first time. A newly developed OS material, InGaSiO (Si/In ratio > 0.47) was found to show high resistivity (>1×10¹⁰ Ω/sq.) after H₂ annealing at 380°C. Enhancement mode operation was confirmed for the InGaSiO TFTs after the annealing. Novel DH TFTs composed of InGaSiO and InGaZnO layers were also examined and achieved both of enhancement mode operation and high mobility of 30 cm²/Vs even after H₂ annealing. These results indicate that the proposed DH TFTs have great potential to serve high-performance BEOL transistors for 3D-LSI applications.

REFERENCES


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