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Abstract: A 1 × 4 loop-mirror-integrated folded silicon-photonics arrayed waveguide grating (AWG) is designed and fabricated on an SOI wafer with two kinds of thickness of silicon areas. The introducing of two silicon thicknesses benefits the design of de/multiplexing devices with an optimal performance and large fabrication tolerances. Transition structures are used to connect 220-nm-thick sections with 340-nm-thick areas. The folded AWG consists of a half normal AWG structure, transition structures array, and loop-mirror reflector array. Each loop-mirror reflector is composed of a 1 × 2 multimode interferometers splitter/combiner and a bend nanowire silicon waveguide, which is designed on a 220-nm-thick silicon region. The half AWG structure with arrayed waveguides is designed on the 340-nm-thick section. The measured on-chip loss and crosstalk are ∼−3.5 and ∼−20 dB, respectively. This integration of devices on an SOI wafer with different thickness of silicon sections is a potential scheme to integrate silicon-based passive and active devices with the best performances of each device.

Index Terms: Folded arrayed waveguide grating, silicon-photonics, loop-mirror reflectors, transition structure.

1. Introduction

Due to the capability of large transmission bandwidth and flexible architecture, optical fiber communications technology continues to grow explosively in the large-scale and long-distance commercial telecommunication networks. Wavelength division multiplexing (WDM) is a critical technology and it is widely used in the commercial optical fiber communications networks. Currently, the commercial optical components are from different material platforms. For example, most of passive optical parts are based on silica because silica waveguide has extreme low loss and its dimension greatly matches the optical fiber. Most of laser sources and photo-detectors are from the III-V material and most of high-speed modulators are made of lithium niobate. With the rapid development of communications for higher transmission capability and lower power consumption, the above...
discrete devices are almost difficult to meet the demand because it is impossible to monolithically integrate them on the same wafer or chip. SOI is a very promising material platform to monolithically integrate full optical passive and active components, except the laser source. SOI-based Silicon photonics has attracted tremendous interest because it has many advantages of compactness, low cost, full integration and its compatibility with complementary metal oxide semiconductor (CMOS) technology for mass production. In the past more than 10 years, lots of silicon-photonics devices with good performances are achieved [1]–[6].

AWG is a key component in WDM system, which is usually used as a multiplexer/de-multiplexer device [7], [8]. Many silicon-photonics AWG results were reported in the past decade on SOI wafers with several-microns-thick or several hundred-nanometers-thick top silicon layers [9]–[18]. The sizes of devices are much compact with insertion losses as low as −2.2 dB [15]. For the crosstalk, silicon AWGs fabricated on several-microns-thick top silicon layer have crosstalk as low as −25 dB [10], instead of −17 −−20 dB for those on a 220 nm-thick silicon layer [15], [17], [18]. The main reason of higher crosstalk for AWGs on a thin silicon layer is that the nanowire waveguide-based AWG is more sensitive to the phase errors brought by fabrication errors and top silicon layer variations [19], [20].

To obtain a low crosstalk, AWG on a SOI wafer with two kinds of silicon thicknesses is proposed in this paper. SOI wafers with a 340 nm-thick top silicon layer are used for the main parts of the AWG such as the planar waveguide and phase arrays to relieve the sensitivity on top silicon thickness variations. By introducing a transition structure, the silicon thickness is reduced to 220 nm to accommodate the other part of the AWG. With this design, high-speed silicon-photonics devices having good performances can be formed on a thinner silicon layer, especially in 220 nm-thick silicon layer. To further reduce the device size, folded silicon-photonics AWG is designed. The terminal reflector consists of a MMI splitter/combiner and a bend waveguide, which is fabricated on the section of 220 nm-thick silicon. The characterized results show that the crosstalk is about −20 dB and the on-chip loss is about −3.5 dB. Compared with other folded AWGs on 220 nm-think silicon layer [21]–[24], this device has a high performance both on loss and crosstalk. The result proves that different silicon-photonics components can be designed and fabricated in different thickness silicon sections on the same SOI wafer. This is a promising scheme to fully integrate different functional silicon-photonics devices with each best performance.

2. Design and Fabrication

The schematic of the folded silicon-photonics AWG with loop-mirror reflectors is depicted in Fig. 1. This structure consists of input/output waveguides, a single slab waveguide, arrayed waveguides, transition structures and loop-mirror reflectors. Its footprint size shrinks 50%, compared to the normal AWG. In this structure, one input waveguide and four output waveguides are connected.
with the input slab waveguide which is subsequently connected with arrayed waveguides, transition structures and loop-mirror reflectors in our structure. The optical signals are launched into the input waveguide and diverged in the slab waveguide, then coupled into the arrayed waveguides. At the end of arrayed waveguides, the signals are compressed from 340 nm-thick silicon into 220 nm-thick silicon by the transition structures, and then coupled into loop-mirror reflector. The reflected signals go back to the arrayed waveguides and the input slab waveguide in sequence, which are further split into the four output waveguides.

The main design parameters of 1×4 folded AWG are listed in Table 1 (left). The initial silicon height was 340 nm. In order to meet the single-mode condition of waveguide, the silicon layer is etched to form the ridge arrayed waveguides with 220 nm in height and 600 nm in width. So, the effective refractive index of the ridge arrayed waveguide is 2.99 for TE mode, based on the silicon material index of 3.48. According to the grating equation of \( m\lambda_0 = N_c \Delta L \) for the centre wavelength, the grating order \( m \) of 25 is selected and the length difference \( \Delta L \) of 12.95 \( \mu \)m between two adjacent arrayed waveguides is calculated. This length difference can make the space among arrayed waveguides enough to insert the reflectors. According to the angle dispersion, we get the equation of \( \Delta \lambda = \Delta X N_s d N_g / (R m N_g) \), where \( \Delta \lambda \) is channel spacing, \( \Delta X \) is the minimum distance of input or output waveguides, \( d \) is the minimum distance of arrayed waveguides, \( R \) is the radius of Rolland circle, \( N_s \) is the effective refractive index of planar waveguide and \( N_g \) is the group index of waveguides. In order to reduce the crosstalk between the adjacent waveguides, \( \Delta X \) and \( d \) are 2.5 \( \mu \)m. When the channel spacing of 6.4 nm is selected, the radius of Rolland circle is 89.3 \( \mu \)m. To reduce the bend loss, the min. bend radius of arrayed waveguide is designed as 50 \( \mu \)m. The design parameters of transition unit and the reflector are also included in Table 1 (right). In the transition unit, two vertical overlapped nano-tapers are used and each silicon etching height is 60 nm as shown in Fig. 1(a). Its waveguide in the port connected with ridge arrayed waveguide is ridge type with a thickness of 340 nm. In another port, it is changed to channel type by the overlapped nano-taper and the channel waveguide thickness is 220 nm. The waveguide width is changed from 600 nm to 500 nm, matching the input waveguide of splitter/combiner. In principle, Y-junction is an ideal choice for this splitter/combiner because of a good wavelength-independent performance. However, the experimental transmission loss of Y-junction is high using current 248 nm deep UV (DUV) photolithography technology. Therefore, a 1×2 MMI unit is used as a splitter/combiner. The MMI width and length are 1.5 \( \mu \)m and 2.0 \( \mu \)m and its schematic is shown in Fig. 1(b).

The simulated optical field distribution of the transition structure is obtained using a 3-dimension (3D) model of RSOFT software with a launched wavelength of 1570 nm, which is shown in Fig. 2. In the simulation model, Z axis is the transmission direction of optical signal; X axis is perpendicular to transmission direction in the integrated plane of the devices; Y axis is perpendicular to the XZ plane and represents the height direction of waveguides. The top view of the simulation result, indicated as the left part of Fig. 2(a), shows that the optical signal has almost lossless propagation from the ridge waveguide to the channel waveguide. On the other hand, we can also infer that the optical signal

<table>
<thead>
<tr>
<th>Structures</th>
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<tbody>
<tr>
<td>Silicon total height</td>
<td>340 nm</td>
<td>Transition unit silicon height</td>
<td>340 nm to 220 nm</td>
</tr>
<tr>
<td>Ridge waveguide height</td>
<td>220 nm</td>
<td>Waveguide width of transition unit</td>
<td>600 nm to 500 nm</td>
</tr>
<tr>
<td>Channel spacing</td>
<td>6.4 nm</td>
<td>1st etching height of transition unit</td>
<td>60 nm</td>
</tr>
<tr>
<td>Grating order</td>
<td>25</td>
<td>2nd etching height of transition unit</td>
<td>60 nm</td>
</tr>
<tr>
<td>Radius of Rolland circle</td>
<td>89.3 ( \mu )m</td>
<td>MMI unit silicon height</td>
<td>220 nm</td>
</tr>
<tr>
<td>Arrayed waveguide width</td>
<td>600 nm</td>
<td>MMI width</td>
<td>1.5 ( \mu )m</td>
</tr>
<tr>
<td>Number of arrayed waveguide</td>
<td>20</td>
<td>MMI length</td>
<td>2.0 ( \mu )m</td>
</tr>
<tr>
<td>Min. radius of arrayed waveguide</td>
<td>50 ( \mu )m</td>
<td>Width of loop waveguide</td>
<td>500 nm</td>
</tr>
<tr>
<td>( \Delta L )</td>
<td>12.95 ( \mu )m</td>
<td>Min. radius of loop waveguide</td>
<td>3.5 ( \mu )m</td>
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is effectively compressed from the 340 nm-thick ridge waveguide into the 220 nm-thick channel waveguide through the vertical overlapped nano-tapers from the lateral view of the simulation result, shown in the Fig. 2(b). Additionally, we also observe that the radiation in the MMI unit is relatively low in the C and L bands, which can be ascribed to small index change of silicon material. Furthermore, the wavelength-dependent silicon material index, simulated transmission and MMI unit loss have also been measured and shown in the Fig. 3. Within the wavelength regime of 1530~1590 nm, the simulated transmission losses of transition structure and 1 × 2 MMI are around −0.11 dB and −0.19 dB for transverse-electric (TE) mode, respectively, and the material index change is less than 0.1%. The loss is insensitive to the change of wavelength in this regime, which is a critical performance for WDM devices. All reflectors have the same structure to conveniently reduce the phase error. For parallel performance comparison, a normal symmetrical 5-ch AWG with 2ΔL was also fabricated on the same wafer, with all other parameters remained the same as listed in the Table 1. Because the turn-round light path, the different length of arrayed waveguides of folded AWG is only half of the normal AWG. The input waveguide location of the folded AWG is the same with the 1st input (or output) waveguide location of the normal AWG. The footprint size of the core structure in the folded AWG is 200 μm × 350 μm.

The folded and normal AWGs were fabricated on a SOI wafer with a 340 nm-thick silicon layer and a BOX layer of 2.0 μm using a 248 nm-DUV lithography exposure system. The brief process flow chart is shown in Fig. 4. First, double silicon-etching processes were performed using mixed gas of hydrobromic acid (HBr) and hydrochloric acid (HCl) to form the two vertical overlapped nano-tapers each of which had an etching height of 60 nm in Fig. 4(a)–(c). Its scanning electron microscope (SEM) image is shown in Fig. 5(a). After the double silicon-etching process, the remained silicon thickness in the loop-mirror area is 220 nm and it is 340 nm thick in the arrayed waveguide area.
Then, a 600 nm-thick SiO\textsubscript{2} layer as hard mask (HM) was deposited. The 3rd lithography was processed for waveguide pattern (including the double nano-taper patterns) and the HM layer was etched using carbon tetrafluoride (CF\textsubscript{4}). After HM pattern formation, a 120 nm-high silicon layer was etched to form the ridge waveguide and the channel waveguide was also partially etched, shown in Fig. 4(d). The SEM images of ridge waveguide are shown in Fig. 5(a) and (b). After clean, the 4th lithography was performed for protecting the ridge waveguide. Another 100 nm-high silicon layer of was etched to form the 220 nm-thick channel waveguide for loop-mirror reflectors, as shown in Fig. 4(e). The SEM image of channel-type reflector is shown in Fig. 5(b) and (c). In the last etching step, an over-etching process was done for a good profile of channel waveguide. For the normal symmetrical 5-ch AWG, only the last two lithography/etching processes were performed. Finally, a more than 120 \(\mu\)m-deep trench was formed for coupling with optical fiber after the deposition of the upper SiO\textsubscript{2} cladding layer of 2 \(\mu\)m, as shown in Fig. 4(f). The optical microscope image of deep trench is shown in Fig. 6(a). After fabrication, the optical microscope (OM) images of the two kinds of AWG are shown in Fig. 6. The left is the OM image of folded AWG and the right is the OM image of normal AWG. In Fig. 6, ridge waveguides are in the light-blue area and channel waveguides are in the dark-blue area. In order to efficiently coupling with lensed fibers, the input/output waveguides are channel-type, located beside the deep trench in Fig. 6(a).

### 3. Characterization and Analysis

In our measurement, a wide amplified spontaneous emission (ASE) source was used because it is hard for the tunable laser source to maintain the same polarization at the whole wavelength range.
An optical polarization controller (Agilent 8169 A), a polarizer and a rotatable input fiber holder was used to keep the input light as the TE mode. More than 99% input light can be kept in TE mode. The lensed fiber had a spot size of 2.5 $\mu$m to couple with the input/output taper waveguide. During the fiber-to-chip alignment, the output optical power was detected by a high-sensitivity optical power meter (Yokogawa AQ2200-215). After alignment, the output optical fiber was switched to a high-precision optical spectrum analyzer (Yokogawa AQ6370D) for optical spectra. Deducting the loss of a straight referenced waveguide, the measured on-chip transmission loss of $1 \times 2$ MMI was presented in Fig. 7. Its loss is $\sim-0.30 \pm 0.02$ dB in the wavelength range of 1530$\sim$1590 nm. The on-chip transmission loss of transition structure is $\sim-0.2 \pm 0.02$ dB, also shown in Fig. 7. At the same time, the propagation loss of ridge waveguide of $\sim-1.70 \pm 0.15$ dB/cm for TE mode was achieved by cut-back waveguides in this wavelength range. Deducting the loss of a straight referenced waveguide, the measured spectra of the folded AWG and the normal reference AWG are shown in Fig. 8(a) and (b), respectively. The results show that the on-chip loss of the folded AWG is $\sim-3.5$ dB and it is $\sim1.0$ dB higher than the loss of the reference AWG. The excess loss is mainly from the transition structure and the MMI splitter/combiner. The lights go through the MMI structure and the transition structure two times in the folded AWG and this excess loss is just around 1.0 dB. Compared to the normal AWG crosstalk of $\sim-25$ dB, the crosstalk of folded AWG is slightly high, $\sim-20$ dB. It may result from the optical leakage from transition structure and loop-mirror reflectors because they have slightly higher loss than the ridge waveguide. Both of AWGs have a channel spacing of $\sim6.8$ nm and the deviation from the design is mainly from the factor of measurement temperature and the excursion of waveguide cross-section. In fact, the
incoming top silicon thickness of our SOI wafer (purchased from SOITEC Company) is ~335 nm by characterization. The deviation of SOI top silicon thickness also contributes to the wavelength shift. The measured non-uniformity performance of folded AWG is 1.35 dB, which is similar to that of reference AWG, 1.10 dB. The measured loss/crosstalk performances of the integrated devices were summarized in Table 2. For a commercial silica-based AWG in the WDM system, a crosstalk of −20 dB and an on-chip loss of ~−1.5 dB are the minimum requirements. The crosstalk of our folded AWG just meets this requirement, but its on-chip loss is lightly higher. The critical issue for the application of our folded AWG is the coupling loss between the single mode fiber and the device. For a commercial silica-based AWG, the coupling loss is usually less than −0.5 dB/facet by using cleaved fibers. However, it is close to −2 dB/facet even if we use lensed fibers to couple. Although some performances are not better than those of silica-based AWG, its footprint is much smaller and it can be monolithically integrated with high-speed active devices. After resolving the coupling issue, this folded silicon-photonics AWG should have a good application prospect.

4. Conclusion
We demonstrated a 1 × 4 folded silicon-photonics AWG with loop-mirror reflectors in this paper. Its length difference of arrayed waveguide is half of the normal AWG with the same optical design. Most parts of the AWG are fabricated on the 340 nm-thick silicon and a transition structure is used to connect the 340 nm-thick arrayed waveguide and the 220 nm-thick reflector. The crosstalk of −20 dB and on-chip loss of −3.5 dB are achieved. The result proves that different silicon-photonics components can be designed and fabricated on SOI wafer with different silicon thicknesses. This is a promising scheme to fully integrate various functional silicon-photonics devices with each best performance on the same SOI wafer.
References