Dr. Ahmed Ali Embarks on an IEEE SSCS DL Tour of the Northeast U.S.

Dr. Ahmed Ali from Analog Devices made several stops during a lecture tour in April 2019.

Lehigh Valley Section of SSCS Hosts Dr. Ahmed Ali

Dr. Ali presented his seminar “Digitally Assisted Data Converters” for the Lehigh Valley Section of the IEEE Solid-State Circuits Society (SSCS) at Lehigh University, Bethlehem, Pennsylvania, on 17 April 2019. The presentation was part of his Distinguished Lecturer (DL) tour of the Northeast United States.

During his introduction, Ali discussed the need for data converters, which interface between the analog and digital worlds, where wide-ranging digital processing can be brought to bear. The converters are found in everything ranging from medical applications to Internet of Things applications and self-driving cars, as presented in one of his introductory slides. As IC technology has advanced, higher digital signal-processing speeds allow the data converter in high-speed communication systems to approach the front end, enabling simpler systems with lower power and higher speed and accuracy.

Ali then covered the essential differences between several analog-to-digital (A/D) architectures. The flash A/D converter (ADC) is at the highest end of the conversion speed scale but requires significant area and power, even for low bit resolution. It involves one comparator for each level to be digitized, so there is no re-use of any converter during the conversion.

At perhaps the other end of the conversion speed scale is the successive approximation radar (SAR) converter, along with the sigma-delta converter. The SAR ADC design includes only one comparator, which is reused for every bit to be converted.

Both the flash and SAR approaches can be modified with pipelined and interleaved methods, respectively, to increase speed and accuracy. In the pipelined approach, conversions take place on an assembly line. The first conversion is performed by the first stage, converting the first bit or first several bits. The residual of the first conversion is amplified and presented to the second stage, and so forth. Therefore, the output of the converter is delayed in time because of the pipelining, but the sample rate remains very high (high throughput). With interleaving, the sample rates can be increased. Using this approach, one pipeline per leaf converts the incoming signal at a fractional phase of the main clock cycle.

In the pipelined ADC, each stage conversion can be a small flash ADC or small SAR ADC, trading off stage delay for complexity. The interstage residual is amplified at the output of each stage. Errors in the residual gain can give rise to conversion errors, degraded linearity (integral and differential nonlinearity), and possibly missing codes. In the frequency domain, these errors appear as unwanted spurs, decreasing the spurious free dynamic range metric.

In addition to residual gain errors, each stage converter is subject to error sources, which can also produce degraded linearity, missing codes, and unwanted spurs. Errors are also introduced in each stage by sampling.

Finally, Ali presented the concept of digitally assisted A/D conversion. Analog parts of the converter are subject to numerous error sources, which may worsen with each new technology node. However, these errors in each component can be corrected using calibration and digital assistance. Large sources of error can be calibrated out digitally by adjusting the components in each stage. Other errors can be corrected by digital assistance, whereby a low-level dither signal is applied to each component and used to correct the digital result caused by each error in the stage residual gain or stage

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conversion. Because each dither signal is uncorrelated with any other, a concurrent algorithm can be used to calibrate every component. Ali showed an impressive series of slides detailing the improvements in linearity, signal-to-noise and distortion ratio versus input signal amplitude, and fast Fourier transforms for calibrated versus uncalibrated converters.

Ali’s presentation covered a broad topic in an understandable and interesting way. At the end of the talk and questions, one member reminded us that there are other varieties of ADCs, each with its own advantages and disadvantages.

—Richard Booth
Webmaster, SSCS Lehigh Valley Section

IEEE SSCS Princeton Chapter Hosts DL Dr. Ahmed Ali

The IEEE SSCS Princeton Chapter organized an SSCS DL presentation, “Digitally Assisted Data Converters,” by Dr. Ali. Data converters play a central role in any electronic system and continue to grow in importance for Internet of Things ubiquitous sensing as well as high-speed converters for 5G applications. Ali’s talk focused on signal processing techniques and algorithms for converting A/D nonidealities. The lecture attracted more than 25 attendees, including students, postdoctoral scholars, local engineers, and IEEE Members, and generated much enthusiasm from those in attendance.

—Kaushik Sengupta

Dr. Ahmed Ali Visits IEEE SSCS New York Chapter

The IEEE SSCS New York Chapter organized a DL presentation by Dr. Ali on 19 April 2019. His lecture, “Digitally Assisted Data Converters,” was well received by all attendees. Ali discussed how data converters are the interface between the analog world and the digital realm. They are so ubiquitous that, on any given day, every person in the developed world will likely utilize a data converter in one form or another. The unyielding demand for higher-resolution ADCs at higher sample rates has made digital assistance a necessity.

During his talk, Ali presented some common architectures and advanced calibration techniques for high-speed, high-resolution ADCs. Included were techniques for correcting nonlinearity, settling, kickback, and memory errors. The talk covered the advantages and limitations of the different approaches as well as practical considerations, design tradeoffs, challenges, and numerous state-of-the-art examples.

—Abira Altvater