Effective Concentration Profile: Mechanism of Gate Field-Plate Assistant Effect in SOI Lateral Power Devices

Jun Zhang, Member, IEEE, Yu-Feng Guo, Member, IEEE, and David Z. Pan, Fellow, IEEE

Abstract—The field-plate (FP) technique suppresses the electric field crowding at the p-n junction by inducing the interface charges in the drift region. However, due to the modeling difficulty, the physical meaning cannot be elaborated via the conventional 2-D methods, not to mention the designing optimization. Therefore, the FP assistant reduced surface field effective concentration profile (ECP) is proposed in this paper to explore the physical insight of the FP assistant 2-D coupling. The ECP simplifies the sophisticated 2-D coupling by equating the FP assistant effect to the variation of the ECP. As a result, a simple and effective 1-D analytical model is presented to qualitatively and quantitatively explore the FP-induced surface field reshaping and its distinctive breakdown mechanism. The analytical solutions are found out to be consistent with the simulation results obtained from MEDICI, a commercial TCAD tool.

Index Terms—1-D model, breakdown voltage (BV), effective doping, field plate (FP).

I. INTRODUCTION

THE unceasing demand for lateral power devices to improve the breakdown voltage (BV), specific ON-resistance ($R_{ON}$), and area utilization simultaneously has led to the introduction of many revolutionary techniques[1]–[4]. Among them, reduced surface field (RESURF) technique has been widely used for its CMOS compatibility [4]–[10]. However, due to its inherent U-shaped surface electric field profile, the lateral breakdown easily happens at both ends of the drift region. Thus, the field-plate (FP) technique has been presented to curb the field crowding at p-n junction. Owing to the FP, a layer of interface charge has been induced on the top of the drift region, which reshapes the surface electric field and, therefore, allows designers to obtain a better tradeoff between BV and $R_{ON}$ [6]–[8]. In early 1990s, the simple 1-D models have been proposed to qualitatively explore the field reshaping effect of FPs [7], [8]. Yet, those 1-D models neglect the coupling effect between the x- and y-dimensions. Subsequently, the 2-D models are used to quantitatively explore the abnormal electric field profile induced by FPs [5], [11]. Conventional 2-D approaches depict such effect via directly solving of 2-D Poisson equation. As a result, these 2-D models can effectively analyze 2-D electric field distribution. Nevertheless, the mathematical expressions of these 2-D models are very complicated and lack of clear physical meaning [5]–[13]. Since the proper shaping of the surface electric field plays a key role in improving the $R_{ON}$ versus BV tradeoff, one of the most vital functions of the analytical model is to provide a theoretical guidance on optimizing the structure. Unfortunately, the conventional 2-D models are incapable of doing so for its complexity [5], [6], [11]–[14].

In this paper, in order to elaborate the physical meaning of the FP technique, we propose the FP assistant RESURF (FP-RESURF) effective concentration profile (ECP) to simplify the sophisticated 2-D coupling effect and equivalent the drift region to a simply 1-D planer junction. The proposed ECP indicates that the FP significantly promotes the drift region depletion in reversed-biased case. Moreover, the further depletion results in an equivalent p-n or p-n-p-n structure of the drift region, which forms a distinctive electric field peak in the drift region. The proposed ECP provides an effective way to reveal the influence of FP-RESURF effect on the performance of silicon on insulator (SOI) lateral double diffusion MOS (LDMOS). Furthermore, a simple but the effective analytical model is presented using the ECP to explore the sensitivity of surface electric field and BV. To our knowledge, the proposed FP assistant ECP and corresponding 1-D model is the first methodology that can provide a simple and clear explanation of the FP-RESURF effects. Finally, an optimization criterion is proposed to provide an efficient and reasonable designing guidance. The analytical solutions are found out to be consistent with the simulation results obtained from MEDICI, a commercial TCAD tool. The simulation models used in MEDICI are CONSRH, AUGER, BGN, FLDMOB, IMPACT I, and CCSMOB [1], [6], [7].
II. EFFECTIVE CONCENTRATION PROFILE

The ECP under the effect of FPs is determined by 2-D Poisson’s equation. To obtain the ECP, a 2-D cross section of SOI LDMOS with gate FP shown in Fig. 1(a) is used for modeling. In this paper, $x$ measures the lateral position relative to the left edge of the drift region and $y$ measures the vertical position relative to the surface of the drift region. Due to the existence of the FP, the drift region can be divided into two parts, region I and II. Furthermore, the drift region under the FP contains two subregions (represented by region I.a and I.b) and the boundary positions of them are given by $L_1$ and $L_2$, respectively. The $t_{ox1}$ is the thickness of the gate oxide layer. Meanwhile, the $t_{ox2}$ being the oxide layer thickness under the gate FP. Under the reverse-bias condition, the potential function within the silicon layer is determined by 2-D Poisson’s equation, which yields

$$\frac{\partial^2 \phi_i(x, y)}{\partial x^2} + \frac{\partial^2 \phi_i(x, y)}{\partial y^2} = -\frac{q N_i}{\varepsilon_s}, \quad i = I \quad (1)$$

$$\frac{\partial^2 \phi_i(x - L_2, y)}{\partial x^2} + \frac{\partial^2 \phi_i(x - L_2, y)}{\partial y^2} = -\frac{q N_i}{\varepsilon_s}, \quad i = II \quad (2)$$

where $q$ is the electronic charge, $N_i$ is the doping concentration of drift region, and $\varepsilon_s$ being the dielectric constant of silicon. The second-order Taylor series expansion along the $y$-dimension is employed to approximate the electric potential [9]–[11]

$$\varphi_i(x, y) = \varphi_i(x, 0) + \left. \frac{\partial \varphi_i(x, y)}{\partial y} \right|_{y=0} y + \left. \frac{\partial^2 \varphi_i(x, y)}{\partial y^2} \right|_{y=0} \frac{y^2}{2} \quad (3)$$

The corresponding boundary condition can be given by [6], [7], [11]

$$\frac{\partial \varphi_i(x, 0)}{\partial y} \bigg|_{y=0} = \frac{[\varphi_i(x, 0) - V_{fox1,2}]}{K_{fox1,2}}, \quad i = I \quad (4)$$

$$\frac{\partial \varphi_i(x, y)}{\partial y} \bigg|_{y=0} = 0, \quad i = II \quad (5)$$

$$\frac{\partial \varphi_i(x, y)}{\partial y} \bigg|_{y=t_s} = -\frac{\varphi_i(x, t_s)}{K_{fox}}, \quad i = I, II \quad (6)$$

where $V_{fox1,2} = V_{gs} - V_{FB1,2}$, $V_g$ being the applied gate voltage and $V_{FB1,2}$ is the flat band voltage of the region I.a and I.b, respectively. $K = \varepsilon_s/\varepsilon_{ox} \approx 3$ is the dielectric constant ratio of silicon and silicon dioxide material. By substituting the (3) and boundary conditions into (1), a general differential equation for the surface potential distribution can be obtained, which yields

$$\frac{\partial^2 \phi_i(x, 0)}{\partial x^2} - \frac{\phi_i(x, 0)}{t_{ox1}^2} = -\frac{q N_{e1,2}}{\varepsilon_s}, \quad i = I \quad (7)$$

$$\frac{\partial^2 \phi_i(x, 0)}{\partial x^2} - \frac{\phi_i(x, 0)}{t^2} = -\frac{q N_d}{\varepsilon_s}, \quad i = II \quad (8)$$

where $a_{1,2} = [(K_{fs} + K_{fox}^2)t_{fox1,2} + 1]$ indicates the influence of gate FP on region I. $N_{e1,2} = (N_d + N_{fox1,2})$ being the ECPs under the FP. $N_{fox1,2} = [(a_{1,2} - 1)\varepsilon_s V_{fox1,2}(q^2)]$ being the effective increment of ECP induced by the FP. $t = (0.5t_{ox}^2 + K_{fs}t_{fox})^{0.5}$ is the characteristic thickness, $t_{a1,2} = t/(a_{1,2})^{0.5}$ is the effective characteristic thicknesses (ECTs) of subregion I.a and I.b, and $t_s$ and $t_{ox}$ are epitaxial and buried oxide (BOX) layer thickness, respectively. Equation (7) indicates, the FP equivalently affects the ECP and the ECT at the same time.

So far, by solving (7) and (8) directly with 2-D methods, the conventional 2-D models are capable of providing accurate surface potential and electric field distribution distributions. Nevertheless, the mathematics expressions for those are too complicated to provide a clear and simple physical insight, and thus failing to elaborate the FP effect and give an efficient optimization tool for the device designing. In order to obtain the simplicity and accuracy simultaneously, the dimension-reduction method proposed in [9] is employed to simplify the 2-D expressions. Such method assumes that the charging charge region (SCR) can be divided into two parts by charge appointment line and only the upper part contributes to the lateral junction. Since the SCR is determined by the lateral and vertical depletions length $x_{int}$ and $x_{ver}$, the ratio of vertical depletions length and SOI layer thickness $\eta = x_{ver}(V_{app})/t_s$ is applied to describe the 2-D coupling between vertical and lateral structure. By using such dimension reduction, the 2-D RESURF effect can be demonstrated by the variation of ECP.

In light of that for the full-depletion case, (7) and (8) can be simplified to 1-D Poisson equations, which yields [9]

$$\frac{\partial^2 \phi_i(x, 0)}{\partial x^2} - \frac{q N_{e1,2}}{\varepsilon_s} \left(1 - \frac{\eta_{1,2}}{L_d} x\right), \quad i = I \quad (9)$$

$$\frac{\partial^2 \phi_i(x, 0)}{\partial x^2} - \frac{q N_d}{\varepsilon_s} \left(1 - \frac{\eta}{L_d - L_2} (x - L_2)\right), \quad i = II \quad (10)$$
where \( \eta_{1,2} = \eta_{1,2}^{0.5} \) reflect the influence of vertical MIS structure on ECTs. Therefore, as shown in Fig. 1(b), the ECP can be given accordingly

\[
N(x) = \begin{cases} 
N_{1} \left( 1 - \eta_{1} \frac{x}{L_{1}} \right) & 0 \leq x \leq L_{1} \\
N_{2} \left( 1 - \eta_{2} \frac{x}{L_{2}} \right) & L_{1} \leq x \leq L_{2} \\
N_{d} \left( 1 - \eta_{d} \frac{x - L_{2}}{L_{d} - L_{2}} \right) & L_{2} \leq x \leq L_{d}
\end{cases}
\]

(11)

It is worth noting that the proposed methodology is still valid when the drift region only partially depleted. In that case, \( L_{d} \) used in (9) and (10) should be replaced by \( \chi_{\text{lat}} \) which is given by \( \int E(x)dx = V_{\text{app}} \) and \( E(\chi_{\text{lat}}) = 0 \). However, since a partially depleted drift region can only sustain a considerable low voltage and thus lack of application lack of practical value, we will not discuss such case in detail within the consideration of this paper [9], [10].

Fig. 2 intuitively illustrates the variation of the ECP under the varied \( V_{\text{app}} \) and structure parameters. With the help of FP assistant depletion effect, as shown in Fig. 2(a) and (b), the drift region rapidly depleted and thus forming an equivalent p-type region. In other words, the gate FPs result in the reduction of equivalent charges in regions that under. It is worth noting that this conclusion also consistent with qualitative analysis from other papers [15], [16]. However, (11) indicates, the FPs not only reduce the equivalent lateral charges, but also alter the characteristic thickness in region I.

Moreover, since the FP only has effects on region I, the ECP in region II still has the same profile as single RESURF case. Thereby, an equivalent reversed-biased p-n junction may form at \( x = L_{2} \). Apparently, the ECP itself is a strong function of the drift region doping concentration. A higher \( N_{d} \) not only enhances the 2-D coupling effect in region II but also strengthens the FP assistant effects in region I. Therefore, with the increase of \( N_{d} \), a higher electric peak at the \( x = L_{2} \) is expected. Fig. 2(d) indicates that the applied \( V_{\text{app}} \) also has an effect on ECP in region I. With the increase of \( V_{\text{app}} \), both the regions I and II will have a higher degree of 2-D coupling effect. Moreover, the ECP in region I is more sensitive to the variation of \( V_{\text{app}} \) than that in region II.

According to the discussion above, as shown in Fig. 3, there are two possible types of equivalent drift region: n-p-n and n-p-n-p types. In n-p-n case, as Fig. 3(a) shows, there ought to be two reversed-biased and one forward-biased equivalent p-n junction. However, since the gate is grounded when at OFF-state, the ECP in region I.a is relatively low. Therefore, the electric field peak at PN(x) is hard to be observed. For the same reason, as shown in Fig. 3(b), there are only two electric field peaks appear in n-p-n-p case.

### III. Surface Electric Field

For an SOI lateral power device, the lateral and vertical structure sustains the reversed-biased applied voltage simultaneously. Therefore, the BV is limited by the weakest point among surface and vertical electric field. For the vertical structure, the weak point occurs at the interface of SOI and BOX layers. Meanwhile, as shown in Fig. 3(b), \( P(x)N(x) \) and \( P(x)n^{+} \) junctions formed two electric fields as the weak points of the lateral junction. In practice, the vertical BV varies insignificantly for a specified processing. In order to explore the breakdown mechanism of FP assistant LDMOS, and thus
The electric field profile of the drift region can be obtained by substituting the ECP profile into 1-D Poisson equation. For a commercial lateral power device, in order to meet the requirements of a high breakdown voltage, the design need to even the surface electric field profile so that a higher BV can be reached. In this case, one needs to even the surface electric field profile so that a higher BV can be reached. In this case, the best scenario is to make the electric field peaks at the surface electric field profile at the region Ia slightly, while $L_2$ affects the location of electric field peak, and thus, reshaping the surface electric profile. As one of the most commonly seen edge termination techniques, the FP can be used around device periphery to minimize crowding of electric field lines at the device edge. Nevertheless, as Fig. 4(b) shows, the designing optimization of the FP plays an essential role in optimizing the device BV characteristics. Furthermore, the $L_1$ is usually very small in the commercial scenario. Since the influence of $L_1$ on the surface electric field is very insignificant in practical, (12) can be further simplified as

\[
E(x, 0) = \begin{cases} 
E_1 - \frac{qN_e}{\varepsilon_s} \left( x - \frac{\eta_1}{2L_d} \right)^2, & 0 \leq x < L_1 \\
E_2 - \frac{qN_e}{\varepsilon_s} \left( x - \frac{\eta_2}{2L_d} \right)^2, & L_1 \leq x < L_2 \\
E_3 - \frac{qN_d}{\varepsilon_s} \left( (x - L_2) - \frac{\eta(x - L_2)^2}{2(L_d - L_2)} \right), & L_2 \leq x < L_d
\end{cases}
\]

where $E_1 = E(0)$ is the surface electric field at the p-n junction, $E_2 = E(L_1) = E_1 + qL_1E_s(\eta_1N_e - N_1) + (\eta_1N_e - \eta_2N_c)\eta_1(2L_d)$ is the electric field peak at $x = L_1$, $E_3 = E(L_2) = E_2 - \frac{qN_e}{\varepsilon_s}L_2$ being the electric field peak at the surface electric field profile. The existence of the FP significantly complicates the designing and optimizing of the SOI lateral power device as well.

IV. BREAKDOWN VOLTAGE

For a lateral power device, the BV is limited by the most vulnerable electric field peak. For the surface breakdown of the LDMOS with FP, there are two possible breakdown points at $x = L_2$ and $x = L_d$. As shown in Fig. 4(c) and (d), the variation of field oxide layer thickness and applied voltage would change the 2-D coupling degree both in regions I and II. The decrease of $t_{fox2}$ or increase of $V_{app}$ would both lift the electric field peak at $x = L_2$. Since the lateral approach consumes a great deal of surface area to support a high-applied voltage, in order to make the lateral power device more commercial competitive and robust, it is vital to even the surface electric field profile so that a higher BV can be reached. In this case, the best scenario is to make the electric field peaks at $x = L_2$ and $x = L_d$ reach the critical electric field ($E_C$) simultaneously. As shown in (12) and (13), to achieve $E(L_d, 0) = E(L_2, 0)$ when a breakdown occurs, the $\eta$ is ought to equal to 2.

In conclusion, the FP substantially assists the depletion of the drift region, and thus inducing an equivalent p-region which results in an electric field peak at the boundary between regions I and II. Such a surface electric field reshaping process is highly dependent on the designing of the structure parameters. Although, the FP can suppress the electric field crowding at the cylindrical region and reshaping the surface electric field profile, the existence of the FP significantly complicates the designing and optimizing of the SOI lateral power device as well.
and, therefore, (13) is applied in this section to derive a simple and clear the breakdown model. By substituting (13) into 1-D Poisson equation, the lateral BV can be obtained, which yields

\[
BV_{\text{lat}} = E_3 L_d - \frac{q N_d \times (L_d - L_2)^2}{2 \varepsilon_s} \left( 1 - \frac{\eta}{3} \right) + \frac{q N_d L_2^2}{2 \varepsilon_s} \left( 1 - \frac{2L_2}{3L_d} \eta_s \right).
\]

For the lateral \( P(x)N(x) \) breakdown case, the breakdown occurs at \( x = L_2 \), and, therefore, \( E_3 = E(L_2) = E_C \). Whereas, for the lateral NN\( + \) breakdown, \( E(L_d) = E_C \) and \( E_3 \) can be obtained accordingly, which yields

\[
E_3 = E_C - \frac{q N_d (L_d - L_2)}{\varepsilon_s} \left( \frac{\eta}{3} - 1 \right).
\]

In this paper, the critical electric field \( (E_C) \) is determined by

\[
E_C = 3 \times 10^5 \left( 1 - 0.33 \log_{10}(N_d/10^{16}) \right) \text{[V/cm]} [10], [13].
\]

Meanwhile, in light of the high BV requirement, the drift region usually fulfills the full-depletion condition. Therefore, the vertical breakdown is determined by the full-depletion BV, which yields \([9], [10], [12]\)

\[
BV_{\text{ver}} = \frac{q N_d L_1}{\varepsilon_s} \left( K \eta_{\text{fox}} + \frac{2\eta - 1}{2} L_1 \right).
\]

Therefore, as mentioned above, the BV of the LDMOS with FP is limited by the lowest BV which can be given by

\[
BV = \min[BV_{\text{lat}}, BV_{\text{ver}}].
\]

Fig. 5 gives the BV as a function of drift region doping concentration. As shown in Fig. 5(a) and (b), the same as a typical RESURF LDMOS, the LDMOS with the FP successively undergoes \( n_n^+ \) junction full depletion, vertical breakdown, \( p-n_d \) junction full depletion, and \( p-n_d \) junction partial depletion with the increase of \( N_d \). However, the p-type region that forms p-n\( _d \) junction is created by extended depletion region due to the FP assistant effect. As shown in Fig. 5(a), since the p-n\( _d \) junction moved from \( x = 0 \) to \( x = L_2 \), the length between the two peaks is reduced to \( L_{\text{eff}} = L_d - L_2 \). Namely, the maximum lateral BV has been shrunk which may further curb the vertical breakdown from happening. Therefore, the \( L_d - L_2 \) has to be large enough to allow the vertical breakdown. As shown in Fig. 5(c), the \( t_{\text{fox}} \) plays an essential role in affecting the device’s BV characteristics. A poorly designed FP could deteriorate the electric field crowding and degrades the BV.

To summarize, the FP induces a further drift region depletion and thus resulting in an n-p-n or n-p-n-p structure in drift region which curbs the electric field peak at \( x = 0 \). As the FP not only reshapes the surface electric field profile but also affects the breakdown characteristic by interfering the inherent 2-D coupling effect, the design difficulty in optimizing the structure parameters along with the FP is increased largely.

V. STRUCTURE OPTIMIZATION

In order to achieve a good tradeoff between breakdown characteristic and process tolerance, a structure optimization criterion (SOC) is essential in designing the structure parameters. Especially, since the existence of the FP results in a complicated surface electric field profile and a sophisticated breakdown characteristic, the optimization of the structure parameters needs to consider the FP assistant effect. However, as a result of its complicated mathematic expressions, the conventional 2-D models are not applicable to provide such a SOC [5], [6], [11]–[14].

For the FP-RESURF lateral power device, we propose an FD SOC to provide a theoretical window for optimizing the drift region doping dose \((Q = N_d \times t_1)\). To obtain a high BV, the device ought to fulfill the vertical breakdown condition. Therefore, the limits of the optimized doping dose (ODD) are determined by the lateral and vertical BVs. The upper limit of ODD \((Q_{\text{up}})\) is limited by the point that vertical structure and lateral p-n\( _d \) junction reaches breakdown simultaneously. Meanwhile, the lower limit \((Q_{\text{down}})\) is obtained when the vertical structure and lateral n\( _n^+ \) junction breakdown happen at the same time. Hence, by substituting (14) into (16), the upper and lower limits of the ODD can be given by

\[
Q_{\text{up}} = Q_s - Q_{G}\cdot F (19)
\]

\[
Q_{\text{down}} = Q_s - Q_{G}\cdot F (19)
\]

where \( Q_s \) and \( Q_{G}\cdot F \) are the upper and lower limits of the single RESURF criterion obtained in [9]. Whereas, the \( Q_{G}\cdot F \) is the effective doping dose increment, which yields

\[
Q_{G}\cdot F = \frac{e_s E_C}{q} \left[ \frac{2a_1^2}{3(a_1^2 - 1)} \left( 1 + a_2 \right) \left( 1 + \frac{a_2^5 N_e}{a_2^2 N_d} \right) \right],
\]

Meanwhile, \( a = t_1/L_{\text{eff}} \) and \( \beta = t_{\text{fox}}/L_{\text{eff}} \), are the shape factors of SOI layer and BOX layer, respectively. \( a_2 = L_2/L_{\text{eff}} \) is the shape factors of the FP. \( L_{\text{eff}} = L_d - L_2 \) represents the effective drift region length.

For the simplicity, the \( E_C \) used in (18)–(20) is \( E_C = 3 \times 10^5 \text{[V/cm]} [9], [10], [13]. It is worth noting that the ODD of FP-RESURF can easily degenerate to ODD of S-RESURF.
FP-RESURF lateral power device can be given as

$$Q_{\text{down}} \leq Q \leq Q_{\text{up}}.$$  \hspace{1cm} (21)

For an FP-RESURF lateral power device, the FP enhances the 2-D coupling effect and thus allowing a higher doping dose in the drift region. Namely, it allows the FP-RESURF a higher doping concentration in drift region to reduce $R_{\text{ON}}$ while maintaining a high $BV$ compared with an S-RESURF LDMOS. However, this effect also comes with a price. As shown in Fig. 6(a) and (b), a higher $L_2/L_d$ not only results in a higher ODD but also brings a smaller process tolerance ($\Delta Q = Q_{\text{up}} - Q_{\text{down}}$).

**VI. CONCLUSION**

For the purpose of providing a simple and clear physical insight for the FP-RESURF lateral power device, we propose the FP assistant ECP to describe the FP assistant effect on 2-D RESURF LDMOS using the variation of the ECP and ECT. The FP ECP indicates that the FP enhances the 2-D coupling and thus causing an equivalent p-region appears in region I. Hence, the sophisticated 2-D drift region can be equivalent to an equivalent n-p-n or n-p-n-p structure which explains the surface electric field reshaping process and an abnormal electric field peak at $x = L_2$. By applying the proposed ECP, a novel 1-D analytical model is presented to qualitatively and quantitatively explore the FP assistant effect on the surface electric field and breakdown mechanism for the first time. Since such an electric field reshaping process changes the 2-D coupling effect which leads to a higher degree of optimization complexity, a simple and effective tool for optimizing the structure parameters of SOI lateral power device with FP is proposed. The proposed methodology is validated by the good agreement between the modeling results and simulation results by MEDICI, a commercial TCAD tool.

**REFERENCES**


Yu-Feng Guo (M’05) received the B.Eng. and M.Eng. degrees from Sichuan University, Chengdu, China, in 1996 and 2001, respectively, and the Ph.D. degree in microelectronics and solid-state electronics from the University of Electronic Science and Technology of China, Chengdu, China, in 2005.

He is currently the Dean of the College of Electronic and Optical Engineering, and the Vice-Director of the National and Local Joint Engineering Laboratory of RF Integration and Micro-Assembly Technology, Nanjing University of Posts and Telecommunications.

David Z. Pan (S’97–M’00–SM’06–F’14) is currently the Engineering Foundation Professor with The University of Texas at Austin, Austin, TX, USA. He has published over 280 refereed technical papers and holds 8 U.S. patents. He has graduated over 20 Ph.D. students. His current research interests include cross-layer IC design for manufacturability, reliability, security, physical design, analog design automation, and CAD for emerging technologies.