

Material Limit of Power Devices—Applied to Asymmetric 2-D Superjunction MOSFET

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Abstract—In spite of the reporting of several mathematical approaches dealing with the behavior of the superjunction MOSFET's specific resistance, a study for the asymmetrical pillar (when the width of the n-pillar and the p-pillar are not the same at a given cellpitch) has not been carried out yet. When the width of one of the pillar (say n-pillar) is modified, the doping concentration (say donor) should be changed to maintain a charge balance condition. This in turn, changes the width of the depletion region, due to the parasitic JFET effect and as a result the effective on-state conduction path. This raises the question whether the best tradeoff between the specific on-state resistance and the breakdown voltage could be achieved by employing the conventional assumption of the same width of the n and p pillars. This paper clarifies the best option for the width of each pillar when designing a superjunction MOSFET and adapts the figures of merit to take into account the asymmetrical superjunction cell.

Index Terms—JFET, power MOSFET, superjunction.

I. INTRODUCTION

THE superjunction field started in the 1980s with the invention of a V-groove MOSFET with multiple p-n layers using the charge balance concept [1]. The first analytical theory was proposed by Fujihira [2], and the first experimental demonstration of a superjunction device, the Cool MOS, was reported in 1998 by Deboy *et al.* [3]. A review of the superjunction field from its invention to present has been recently published by Udrea *et al.* [4]. Since the introduction of the ideal relationship between the superjunction MOSFET specific ON-state resistance R_{sp} and breakdown voltage V_B [2], there have been several attempts of mathematically modeling the superjunction in different modes of operation. For example, Strollo and Napoli [5] first solved Poisson's equation for a 2-D superjunction structure to obtain a potential distribution at a reverse-biased condition, and expanded the solution to a charge-imbalance condition by devising a charge

superposition principle [6], [7]. Disney and Dolny [8] tried to find a limit of specific resistance of a superjunction by inserting a parasitic JFET in the superjunction with simulation study. Saito [9] found the variation of the breakdown voltage when a superjunction has a graded doping profile. Recently, Kang and Udrea [10] devised a systematic JFET model for a superjunction to show the material limit and proved that R_{sp} for a superjunction MOSFET cannot be cut indefinitely. In addition to this, a new figure of merit (FOM), $\mu_n \epsilon_S E_C^{2.5}$, for a superjunction MOSFET was derived and compared with the conventionally accepted Baliga's FOM $\mu_n \epsilon_S E_C^3$ and Fujihira's FOM $\mu_n \epsilon_S E_C^2$ [4] (where μ_n , ϵ_S , and E_C are electron mobility, permittivity of a semiconductor material, and critical electric field, respectively). The studies mentioned above assumed that the width of the p- and n-pillars were the same. This assumption is sensible as a first-order approximation, due to the charge balance condition for the relatively large dimensions.

However, as the technology evolves and the dimensions of the cellpitch are continually reduced, the effect of the asymmetrical design can no longer be ignored. For example, when the width of the n-pillar is relatively wider than that of the p-pillar, the doping concentration of the n-pillar should be lower than that of the p-pillar to maintain the charge balance condition. In this case, the depletion region created by the parasitic JFET extends more toward the n-pillar than that of the p-pillar, reducing its effective conducting doping region. This leads to the idea that the best tradeoff between R_{sp} and V_B may not result from a superjunction structure with equal widths of the pillars.

This paper analytically calculates the ON-state specific resistance R_{sp} with respect to the width of the conducting doping region, βd ($0 < \beta < 1$), when a cellpitch d is given as shown in Fig. 1. For this, the resistances of the channel, the source, and the drain contact are ignored, to concentrate our study on the drift region alone. This paper adopts a previously reported 1M1J (1 MOSFET + 1 JFET) approach to include a parasitic JFET effect in the n-pillar introduced by the built-in potential and the applied drain bias [10].

II. IDEAL APPROACH

The calculation process of an ideal tradeoff between R_{sp} and V_B follows Fujihira's approach [2]. It should be noted that the model of the ideal R_{sp} does not take into account the parasitic JFET in a superjunction. For a charge balance in the

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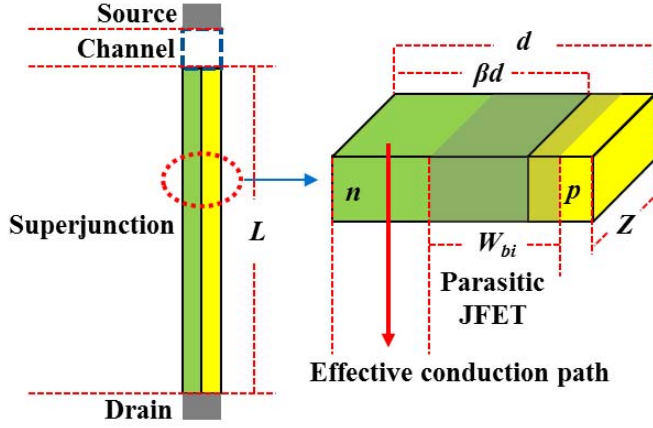


Fig. 1. Illustration of the zero-bias parasitic JFET or depletion width on the pillars. d is the cellpitch, βd is the width of the n-pillar ($0 < \beta < 1$), W_{bt} is the depletion width, L is the length of the pillar, and Z is the depth of the pillar.

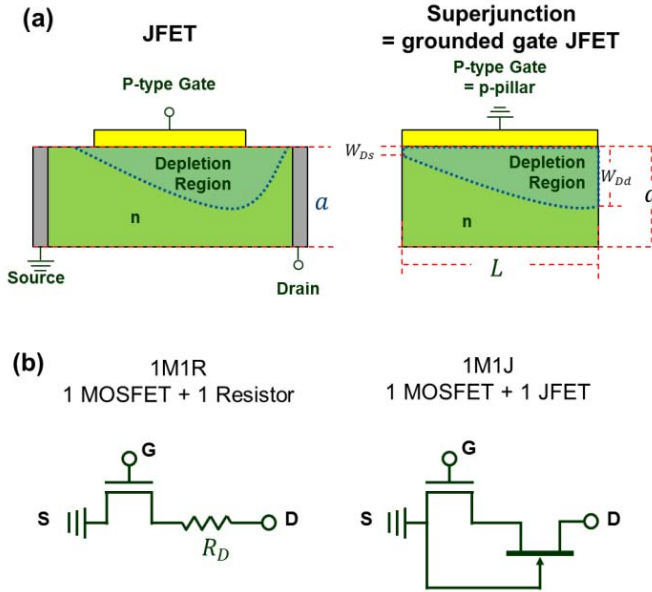


Fig. 2. (a) Illustration of a superjunction as a JFET: p-pillar is a gate of the JFET. (b) Changed inner circuit model: the drift region is regarded as a JFET rather than the resistor [10].

pillars, the concentration of the n-pillar N_D and the p-pillar N_A should have the following relationship:

$$N_D \beta d = N_A (1 - \beta) d \quad (\text{cm}^{-2}), \quad (0 < \beta < 1). \quad (1)$$

The maximum value of the lateral electric field across the n-pillar and the p-pillar, E_x , should be less than the critical electric field E_C by applying Poisson equation:

$$E_x = \alpha E_C = \frac{q N_D}{\epsilon_S} \beta d \quad (\text{V/cm}), \quad (0 < \alpha \leq 1). \quad (2)$$

where, q and ϵ_S are unit charge and the permittivity of a semiconductor material, respectively. Since, the total electric field E_C is the square root of the sum of square of the lateral and vertical electric fields E_x^2 and E_y^2 , the vertical electric field

E_y is derived as

$$E_y = E_C \sqrt{1 - \alpha^2} \quad (\text{V/cm}). \quad (3)$$

As the length of the superjunction L is relatively long enough compared to the cellpitch d by ignoring lateral voltage, the breakdown voltage V_B of a superjunction is assumed to be given only the vertical term

$$V_B = \frac{1}{2} \alpha d E_C + E_C L \sqrt{1 - \alpha^2} \approx E_C L \sqrt{1 - \alpha^2} \quad (\text{V}). \quad (4)$$

The ideal R_{sp} is a multiplication form of the resistance, $(1/qN_D\mu_n)(L/\beta dZ)$, with the area dZ

$$R_{sp} = \frac{1}{qN_D\mu_n} \frac{L}{\beta dZ} dZ = \frac{L}{qN_D\mu_n} \frac{1}{\beta} \quad (\Omega \cdot \text{cm}^2) \quad (5)$$

where μ_n is an impurity-dependent electron mobility and the relationship is modeled in Baliga's research [11] for both Si and 4H-SiC

$$\mu_n(\text{Si}) = \frac{5.10 \times 10^{18} + 92N_D^{0.91}}{3.75 \times 10^{15} + N_D^{0.91}} \quad (\text{cm}^2/\text{Vs}) \quad (6-1)$$

$$\mu_n(\text{SiC}) = \frac{4.05 \times 10^{13} + 20N_D^{0.61}}{3.55 \times 10^{10} + N_D^{0.61}} \quad (\text{cm}^2/\text{Vs}). \quad (6-2)$$

Inserting (2) and (4) into (5), R_{sp} leads to the following relationship:

$$R_{sp} = \frac{V_B}{\alpha \sqrt{1 - \alpha^2} \mu_n \epsilon_S E_C^2} d = \frac{2V_B}{\mu_n \epsilon_S E_C^2} d, \quad \alpha = \frac{1}{\sqrt{2}} \quad (7)$$

Equation (7) has the lowest value at $\alpha = 1/\sqrt{2}$, and the ideal R_{sp} is not related to β . The ideal R_{sp} is linearly proportional to the breakdown voltage V_B . The ideal R_{sp} model does not contain a theoretical limit because the R_{sp} can be reduced indefinitely by decreasing the cellpitch d . Therefore, to understand a realistic performance of the superjunction MOSFET, the JFET effect in the pillars must be considered.

III. JFET APPROACH

As reported in [10], a superjunction MOSFET is a series of one intrinsic MOSFET and one JFET, where the p-pillar acts as a gate of the JFET and the n-pillar is a channel of the JFET, as shown in Fig. 1(a). The drain current can be obtained by integrating the sheet charge density $Q_n(x)$ in the conduction path and the velocity of the electron $v(x)$ [12]

$$I_D = \frac{Z}{L} \int_0^L Q_n(x) v(x) dx (A). \quad (8)$$

The sheet charge density $Q_n(x)$ is expressed as

$$Q_n(x) = q N_D (\beta d - W_D) \quad (\text{cm}^{-2}). \quad (9)$$

By combining the charge balance relationship given by (1), the depletion width W_D in the n-pillar becomes a function of the applied potential ψ and the factor of the conduction path, β

$$W_D = \sqrt{\frac{2\epsilon_S N_A \psi}{q N_D (N_A + N_D)}} = \sqrt{\frac{2\epsilon_S \beta \psi}{q N_D}} \quad (\text{cm}^{-2}). \quad (10)$$

The derivative of (10) leads to

$$\frac{dW_D}{d\psi} = \frac{\varepsilon_S \beta}{q N_D W_D} \text{ (cm/V)} \quad (11)$$

and the velocity also can be expressed as a function of the applied potential

$$v(x) = \mu_n \frac{d\psi(x)}{dx} \text{ (cm/s)}. \quad (12)$$

By inserting (9), (11), and (12) into (8), the equation for the drain current leads to the following integral form:

$$I_D = \frac{Z \mu_n q^2 N_D^2}{\varepsilon_S L \beta} \int_{W_{D_s}}^{W_{D_d}} (\beta d - W_D) W_D d W_D \quad (13)$$

where the depletion width on the bottom of n-pillar W_{D_d} and the depletion width on the top of the n-pillar W_{D_s} can be expressed as a function of the pinch-off potential ψ_p and the built-in potential ψ_{bi} of the pillars

$$W_{D_d} = \sqrt{\frac{2\varepsilon_S \beta (\psi_{bi} + V_{DS})}{q N_D}} = \beta d \sqrt{\frac{\psi_{bi} + V_{DS}}{\psi_p}} = \beta d \cdot u_d \quad (14-1)$$

$$W_{D_s} = \sqrt{\frac{2\varepsilon_S \beta \psi_{bi}}{q N_D}} = \beta d \sqrt{\frac{\psi_{bi}}{\psi_p}} = \beta d \cdot u_s. \quad (14-2)$$

The pinch-off potential is the required voltage to deplete both the p- and n-pillars

$$\psi_p = \frac{q N_D}{2\varepsilon_S} (\beta d)^2 + \frac{q N_A}{2\varepsilon_S} (d - \beta d)^2 = \frac{q N_D}{2\varepsilon_S} \beta d^2 \text{ (V)}. \quad (15)$$

The built-in potential has the following relationship [12]:

$$\psi_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right) = \frac{kT}{q} \ln \left(\frac{N_D^2}{n_i^2} \frac{\beta}{1 - \beta} \right) \quad (16)$$

where k and T are Boltzman constant and absolute temperature ($T = 300$ K), respectively. Finally, the integral for (13) leads to

$$I_D = \frac{Z \mu_n q^2 N_D^2 \beta^2 d^3}{6\varepsilon_S L} \cdot U(V_{DS}) \text{ (A)}. \quad (17)$$

where $U(V_{DS})$ is a JFET function which describes the depletion of the pillars with respect to the applied drain voltage V_{DS} . The JFET function consists of u_d and u_s given by (14)

$$U(V_{DS}) = 3(u_d^2 - u_s^2) - 2(u_d^3 - u_s^3). \quad (18)$$

By multiplying the area dZ by the resistance, V_{DS}/I_D , the specific resistance including the parasitic JFET can be derived as

$$R_{sp} = \frac{V_{DS}}{I_D} \times dZ = \frac{6\varepsilon_S L}{\mu_n q^2 N_D^2 \beta^2 d^2} \cdot \frac{V_{DS}}{U(V_{DS})} \text{ (}\Omega \cdot \text{cm}^2\text{)}. \quad (19)$$

The R_{sp} has a minimum value when the V_{DS} approaches zero, i.e., the width of the parasitic JFET can be minimized. By applying the well-known *L'Hospital's* rule [13] to the second term of (19), a simple form of $V_{DS}/U(V_{DS})$ can be obtained

$$\lim_{V_{DS} \rightarrow 0} \frac{V_{DS}}{U(V_{DS})} = \frac{1}{3} \frac{\psi_p \sqrt{\psi_p}}{\sqrt{\psi_p} - \sqrt{\psi_{bi}}} \text{ (V)}. \quad (20)$$

By inserting (15) and (20) into (19), the R_{sp} at $V_{DS} = 0$ V has the following form:

$$R_{sp} = \frac{L}{q \mu_n N_D \beta} \left(\frac{\sqrt{\psi_p}}{\sqrt{\psi_p} - \sqrt{\psi_{bi}}} \right) \text{ (}\Omega \cdot \text{cm}^2\text{)}. \quad (21)$$

Equation (21) accounts for: 1) an ideal R_{sp} for a superjunction MOSFET given by (5), and 2) the parasitic JFET in a superjunction. Since the depletion width of the pillars is proportional to the square root of the applied bias, the R_{sp} in (21) can be expressed using dimensional terms, βd (width of the n-pillar) and W_{D_s} (depletion width of the n-pillar).

$$R_{sp} = \frac{L}{q \mu_n N_D \beta} \left(\frac{\beta d}{\beta d - W_{D_s}} \right) \text{ (}\Omega \cdot \text{cm}^2\text{)}. \quad (22)$$

From (22), the real R_{sp} can be intuitively understood that R_{sp} including the pillar's JFET is the ratio of the conduction path βd and the effective conduction path $(\beta d - W_{D_s})$. As the cellpitch d decreases, the effective conduction path $(\beta d - W_{D_s})$ will be decreased significantly reaching a minimum R_{sp} , and then, R_{sp} will increase again. Furthermore, the R_{sp} given by (22) can be expressed in the following form using the material terms given by (7):

$$R_{sp} = \frac{2V_B}{\mu_n \varepsilon_S E_C^2} d \left(\frac{\sqrt{\psi_p}}{\sqrt{\psi_p} - \sqrt{\psi_{bi}}} \right) \text{ (}\Omega \cdot \text{cm}^2\text{)}. \quad (23)$$

To obtain a value of R_{sp} , the optimum concentration with respect to each cellpitch should be defined first. By inserting the value of α given by (7) into (2), and combining the optimum concentration relationship given by (2) and Baliga's critical electric field, E_C , given by (24) [11], the optimum concentration becomes a function of βd

$$E_C(\text{Si}) = 4.0 \times 10^3 \cdot N_D^{\frac{1}{8}} \text{ (V/cm)} \quad (24-1)$$

$$E_C(\text{SiC}) = 3.3 \times 10^4 \cdot N_D^{\frac{1}{8}} \text{ (V/cm)} \quad (24-2)$$

$$N_D(\text{Si}) = \frac{1}{\sqrt{2}} \frac{\varepsilon_{Si} E_{C,Si}}{q \beta d} = 5.30 \times 10^{11} \cdot (\beta d)^{-8/7} \text{ (cm}^{-3}\text{)} \quad (25-1)$$

$$N_D(\text{SiC}) = \frac{1}{\sqrt{2}} \frac{\varepsilon_{SiC} E_{C,SiC}}{q \beta d} = 4.80 \times 10^{12} \cdot (\beta d)^{-8/7} \text{ (cm}^{-3}\text{)}. \quad (25-2)$$

where ε_S for Si, SiC, and q are $\varepsilon_{Si} = 1.03 \times 10^{-12}$ (F/cm), $\varepsilon_{SiC} = 8.55 \times 10^{-13}$ (F/cm) [14], and 1.60×10^{-19} (C), respectively. The graphs for N_D at each cellpitch in (25) are shown in Fig. 3(a) and (c). As the conduction path βd decreases, the required N_D becomes higher. It should be noted that the total amount of sheet charge, $N_D \beta d$ (cm⁻²), is maintained as $\varepsilon_S E_C / \sqrt{2} q$. The impurity-dependent mobility relationship for Si [11] given by (6) is shown in Fig. 3(b) and (d) (black lines). Since a narrow conduction path, a small β , has a higher N_D , the impurity-dependent mobility has a lower value. Finally, by inserting the optimum concentration, N_D , given by (25), mobility μ_n from (6), pinch-off potential ψ_p from (15), and built in potential ψ_{bi} from (16) into (21), R_{sp} with respect to cellpitch d can be calculated as shown in Fig. 4. The length of pillar L is 30 μm and β is varied from 0.1 to 0.9. R_{sp} for both Si and SiC devices decrease until they reach

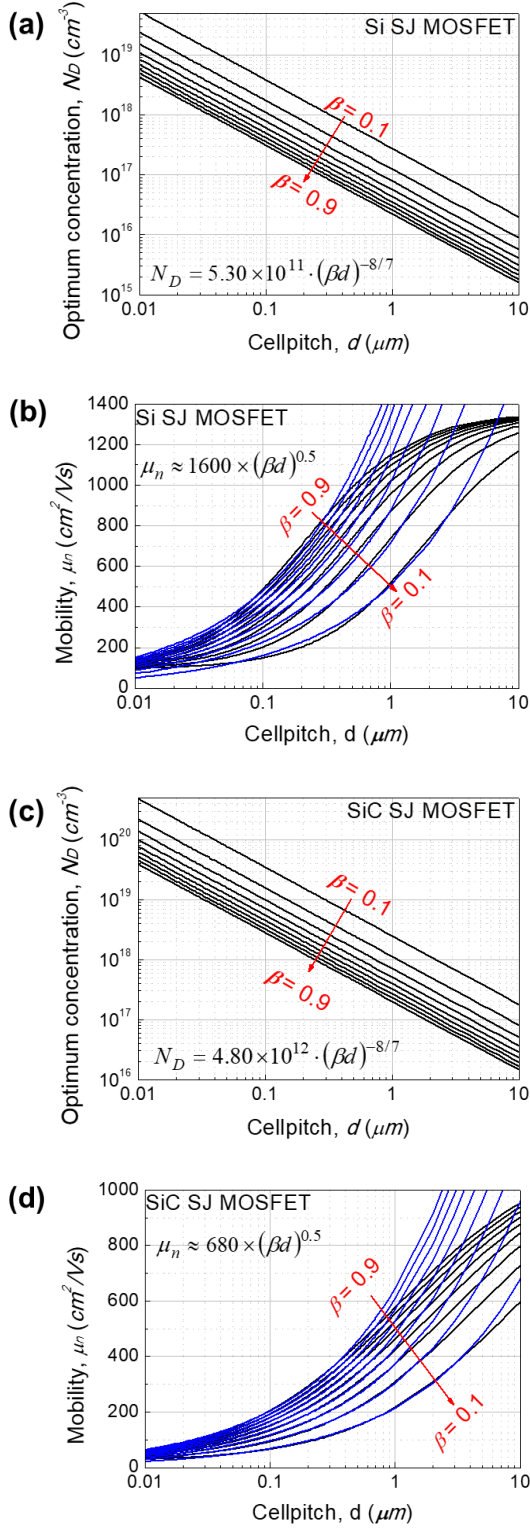


Fig. 3. (a) and (c) Optimum concentration for Si and SiC, respectively. (b) and (d) Concentration-dependent mobility for Si and SiC, respectively, (black lines). (b) and (d) Approximated mobility for Si, $\mu_n(\text{Si}) = 1600 \times (\beta d)^{0.5}$ and SiC, $\mu_n(\text{SiC}) = 680 \times (\beta d)^{0.5}$, respectively, (blue lines). β is increased from 0.1 to 0.9 by 0.1.

a minimum point, and rapidly increase again. The overall decrease in R_{sp} with scaling down is owing to the increased impurity concentration N_D . The sharp increase in R_{sp} beyond

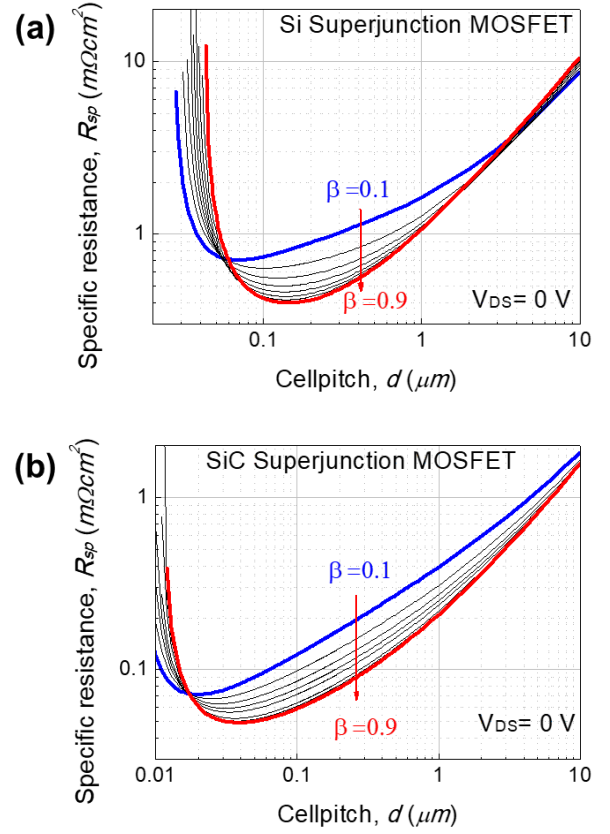


Fig. 4. Specific resistance R_{sp} with respect to cellpitch d , when the parasitic JFET in the n-pillar is included for (a) Si and (b) SiC. β is increased from 0.1 to 0.9 by 0.1.

its minimum is due to the fact that the parasitic JFET width becomes comparable to that of the n-pillar, thus, narrowing the conduction path significantly.

For more detailed information, R_{sp} values in practical cellpitches are provided in Fig. 5. For a silicon superjunction MOSFET, when cellpitch d is higher than $3 \mu\text{m}$, lower β results in a lower R_{sp} owing to the narrow depletion width toward the n-pillar. In a real case, both the concentration-dependent mobility μ_n and the effective conduction path ($\beta d - W_{\text{Ds}}$) contribute to R_{sp} . Therefore, lower β with a narrow built-in depletion width should have lower R_{sp} when the value of the mobility is similar (not a large difference) to that of a high β . Below $3\text{-}\mu\text{m}$ cellpitch, lower β results in higher R_{sp} . As can be seen from Fig. 3(b), the electron mobility shows an exponential decrease from a specific cellpitch. Therefore, R_{sp} of lower β device having a substantially lower mobility decreases slowly at a smaller cellpitch ($d < 3 \mu\text{m}$). For SiC, as cellpitch d decreases from $10 \mu\text{m}$, lower β results in higher R_{sp} . This trend can be also explained by the rapidly decreased value of the electron mobility for lower β , as shown in Fig. 3(d).

IV. FIGURE OF MERIT

To find the best tradeoff between R_{sp} and V_B , the FOM, V_B/R_{sp} , at each β and cellpitch is presented in Fig. 6. V_B was calculated from (4). The FOM for both Si and SiC devices

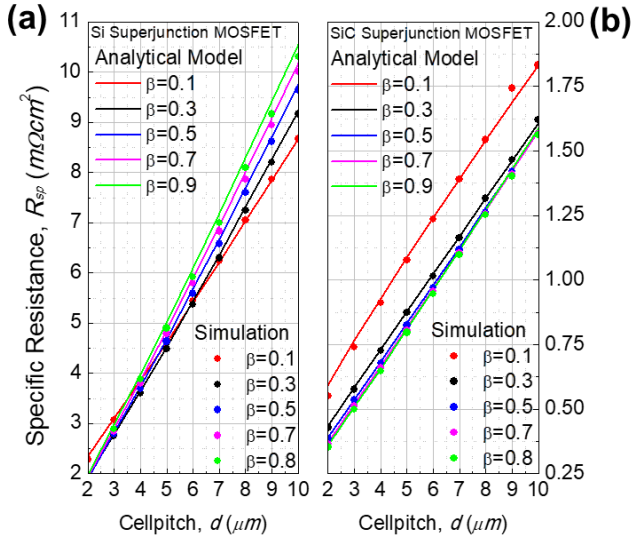


Fig. 5. Analytical model and simulation result of the specific resistance for (a) Si and (b) SiC.

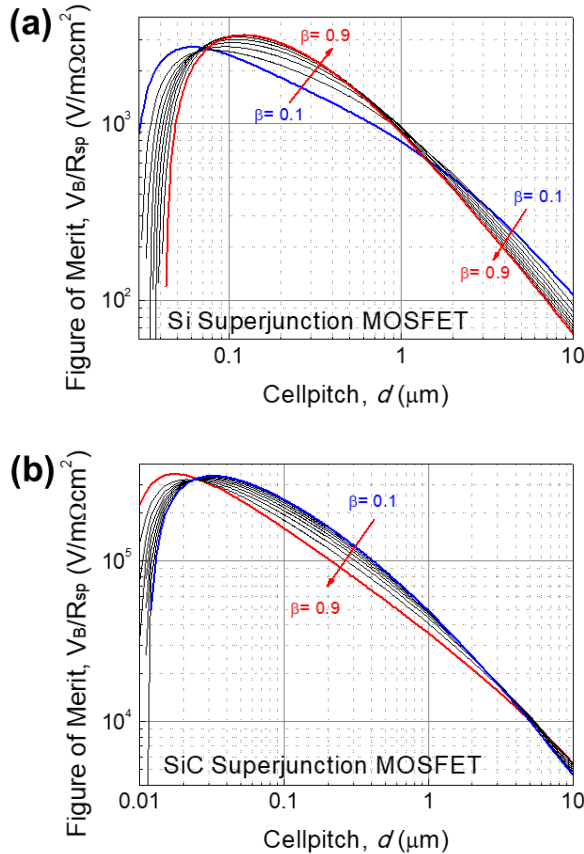


Fig. 6. FOM, V_B/R_{sp} , at a given cellpitch for (a) Si and (b) SiC. β is increased from 0.1 to 0.9 by 0.1.

increases as scaling down the cellpitch owing to the increase in V_B and the decrease in R_{sp} . After reaching a maximum value, it decreases again due to the rapid increase in R_{sp} . In the practical ranges ($d > 2 \mu\text{m}$), lower β has a higher FOM than higher β for Si. In the case of SiC, higher β has higher FOM

above $5\text{-}\mu\text{m}$ cellpitch, but lower β becomes better as scaling down more. Therefore, the best tradeoff between R_{sp} and V_B at a given cellpitch is not in the same width of the pillars in the overall range of cellpitches.

The last step is to find a minimum value of R_{sp} as shown in Fig. 4 to obtain the best FOM for a superjunction MOSFET according to β . For this, N_D , μ_n , and ψ_p in (21) should be expressed with respect to βd for a convenience of the calculation. As derived by (25), the optimum concentration N_D is $5.30 \times 10^{11} \cdot (\beta d)^{-8/7}$ for Si, and $4.80 \times 10^{12} \times (\beta d)^{-8/7}$ for SiC. The impurity-dependent mobility μ_n can be approximated as $1600 \times (\beta d)^{1/2}$ for Si and for $680 \times (\beta d)^{1/2}$ for SiC, as shown in Fig. 3(b) and (d), (bluelines):

$$\mu_n(\text{Si}) \approx 1600 \times (\beta d)^{1/2} \quad (26-1)$$

$$\mu_n(\text{SiC}) \approx 680 \times (\beta d)^{1/2}. \quad (26-2)$$

This approximation for the electron mobility is valid because the minimum point of R_{sp} is located at smaller than when $\beta d = 0.1 \mu\text{m}$. Therefore, the second term of (21) can be expressed as a function of βd

$$R_{sp} = \frac{L}{q\beta} \cdot \frac{1}{\mu_n N_D} \left(\frac{\sqrt{\beta \psi_p}}{\sqrt{\beta \psi_p} - \sqrt{\beta \frac{E_g}{q}}} \right) = \frac{L}{q\beta} \cdot \Psi(\beta d). \quad (27)$$

Since the pinch-off potential ψ_p is a function of $\beta^2 d$ as shown in (15), for a convenience of calculation, both the nominator and the denominator are multiplied by β . The built-in potential ψ_{bi} can be replaced with the potential of the material's bandgap, E_g/q because the minimum R_{sp} happens at a very high impurity concentration, $N_D > 1 \times 10^{17} \text{cm}^{-3}$. By solving a differential form for (27), $\partial \Psi(\beta d)/\partial d = 0$, the condition for a minimum R_{sp} can be found as

$$\sqrt{\frac{\beta \psi_{bi}}{\beta \psi_p}} = \frac{W_D}{\beta d} = \sqrt{\frac{E_g}{q \psi_p}} = \frac{3}{5}, \quad \left(\frac{\partial \Psi(\beta d)}{\partial d} = 0 \right). \quad (28)$$

As mentioned earlier, since the depletion width is proportional to the square root of the applied potential, (28) can be expressed as the ratio of the depletion width in the n-pillar W_D , and the width of the conduction path βd . Unrelating to β , when the depletion width occupies 60% of the conduction path (n-pillar), the device reaches a minimum R_{sp} . By combining optimum concentration relationship, $N_D = \epsilon_S E_C / \sqrt{2} q \beta d$, given by (25) with the pinch-off potential given by (15), the pinch-off potential can be expressed in terms of the critical electric field and the cellpitch

$$\psi_p = \frac{q N_D}{2 \epsilon_S} \beta d^2 = \frac{E_C}{2 \sqrt{2}} d \text{ (V)}. \quad (29)$$

Inserting the pinch-off potential given by (29) into (28), the minimum cellpitch d_{OP} becomes a function of material parameters $d_{OP} = E_g/q E_C$

$$d_{OP} = \frac{50 \sqrt{2}}{9} \frac{E_g}{q E_C} \text{ (cm)}. \quad (30)$$

Intuitively, since lower β has higher critical electric field E_C owing to the higher concentration, lower β will present a

smaller optimum cellpitch than that of higher β . Systematically, by combining (24) and (25), the critical electric field can be expressed in terms of βd

$$E_C(\text{Si}) = 1.26 \times 10^5 \cdot (\beta d)^{-1/7} \text{ (V/cm)} \quad (31-1)$$

$$E_C(\text{SiC}) = 1.27 \times 10^6 \cdot (\beta d)^{-1/7} \text{ (V/cm)}. \quad (31-2)$$

By inserting (31) and $E_g/q = 1.12 \text{ V}$ for Si and 3.25 V for 4H-SiC [15] into (30), the optimum cellpitch with respect to β can be obtained

$$d_{\text{OP}}(\text{Si}) = \frac{50\sqrt{2}}{9} \frac{E_g}{qE_C} = 0.14 \cdot \beta^{1/6} \text{ (}\mu\text{m)} \quad (32-1)$$

$$d_{\text{OP}}(\text{SiC}) = \frac{50\sqrt{2}}{9} \frac{E_g}{qE_C} = 0.032 \cdot \beta^{1/6} \text{ (}\mu\text{m)}. \quad (32-2)$$

As β increases, the device has higher optimum cellpitch owing to lower concentration and the wider depletion width of the n-pillar. Since, a SiC superjunction MOSFET has a higher concentration than that of Si; this device has a smaller optimum cellpitch than that of Si.

Last, for an FOM, the optimum condition given by (28) and the optimum cellpitch given by (30) are inserted into (23)

$$R_{\text{sp}} = \frac{125\sqrt{2}}{9} \frac{E_g}{q\mu_n\epsilon_S E_C^3} V_B \quad (33)$$

According to Hudgins's relationship [15], $E_g^2 \propto E_C$, the minimum specific resistance for 2-D superjunction MOSFET given by (33) is proportional to E_g^5

$$R_{\text{sp}} \propto \frac{V_B}{\mu_n\epsilon_S E_g^5} \quad (34)$$

or is inversely proportional to $E_C^{2.5}$

$$R_{\text{sp}} \propto \frac{V_B}{\mu_n\epsilon_S E_C^{2.5}}. \quad (35)$$

The 2-D FOM for a superjunction MOSFET is determined by the material parameters μ_n , ϵ_S , and especially $E_C^{2.5}$ or E_g^5 . On the surface, the FOM is unrelated to the value of β . However, by inserting the optimum cellpitch given by (30) into the critical electric field given by (24) and the mobility given by (26), the FOM can be rewritten in terms of β

$$\text{FOM} = \mu_n\epsilon_S E_C^{2.5} \propto \epsilon_S \beta^{1/6}. \quad (36)$$

Therefore, when the conduction path factor β is fixed, the FOM given by (36) is only linearly proportional to the permittivity of a semiconductor material. In other words, when the material is the same (the same permittivity), wider n-pillar width (a larger β) has a higher FOM.

It is worthwhile to compare the results from this paper to those earlier reported by Disney and Dolny [8]. In this paper, for a 2-D superjunction (stripe design) MOSFET rated at 1.2 kV, the minimal specific ON-state resistance was obtained for a combination of 129-nm n-pillar width and 13-nm p-pillar width for Silicon ($R_{\text{sp},\text{min}} = 0.380 \text{ m}\Omega \cdot \text{cm}^2$) and 35-nm n-pillar width and 4-nm p-pillar width for 4H-SiC ($R_{\text{sp},\text{min}} = 3.6 \mu\Omega \cdot \text{cm}^2$). The value of the minimum R_{sp} will be increased when the applied ON-state drain bias increases as

previously reported by Disney and Dolny [8] our group [10]. The increased drain bias causes the width of the conducting doping region (the lower side of the n-pillar), $\beta d - W_{\text{Dd}}$, to be smaller owing to the increased depletion width W_{Dd} , as shown in Fig. 2(a) and (14-2). R_{sp} at a specific bias condition can be calculated by using (19) and the electric field-dependent mobility model for a superjunction [10]

$$\mu_n(V_{\text{DS}}, N_D) = \frac{\mu_{n0}}{\left(1 + \left(\frac{V_{\text{DS}}}{E_C L}\right)^{\frac{1}{m}}\right)^{3m}}, \quad m = 1.73. \quad (37)$$

Even though the values were not directly reported, Disney and Dolny's minimum R_{sp} and the cellpitch for a silicon device were around $1.5 \text{ m}\Omega \cdot \text{cm}^2$ and $d = 400 \text{ nm}$ for $N_D = 5 \times 10^{16} \text{ cm}^{-2}$, $L = 40 \mu\text{m}$, and $\beta = 0.5$ at 1-V drain bias. In this paper, when the same conditions are applied ($\beta = 0.5$, $N_D = 5 \times 10^{16} \text{ cm}^{-2}$, $d = 400 \text{ nm}$, $L = 40$, and $V_{\text{DS}} = 1 \text{ V}$) to (19), R_{sp} was $1.42 \text{ m}\Omega \cdot \text{cm}^2$. The two values are similar. Interestingly, in the case of the device with the conditions, $\beta = 0.5$, $L = 40$, and $V_{\text{DS}} = 1 \text{ V}$, the minimum R_{sp} and the cellpitch were $0.85 \text{ m}\Omega \cdot \text{cm}^2$ and 200 nm , respectively, at $N_D = 2.75 \times 10^{17} \text{ cm}^{-2}$. If Disney and Dolny's report had increased the doping concentration, the result would have shown lower R_{sp} at lower cellpitch. Nevertheless, the study by Disney and Dolny did not take into account the additional benefits of the asymmetrical structure as discussed here in this paper, which results in lowering further the ON-state resistance

V. CONCLUSION

This paper provided an insight into the specific ON-state resistance for a 2-D superjunction MOSFET when the width of the n-pillar was varied at a given cellpitch, while maintaining the charge balance between the n- and p-pillars. The analytical model developed here takes into account the parasitic JFET effect and the mobility dependence on the doping, and showed that the assumption that the optimal ON-state resistance occurs for equal widths of the n- and p-pillars is incorrect. For a silicon superjunction MOSFET, a narrower n-pillar width is better than a wider n-pillar above $3\text{-}\mu\text{m}$ cellpitch. The reverse is true for narrower dimensions. Interestingly, for a wide bandgap semiconductor such as 4H-SiC, a wider n-pillar width showed lower R_{sp} than a narrower n-pillar for the range of the cellpitch considered ($0.01\text{--}10 \mu\text{m}$). The model is in very good agreement with the TCAD simulations with the maximum relative error below 3% for the whole range of dimensions considered.

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REFERENCES

- [1] D. J. Coe, "High voltage semiconductor devices," U.S. Patent EP0053854 A1, Jun. 16, 1982.
- [2] T. Fujihira, "Theory of semiconductor superjunction devices," *Jpn. J. Appl. Phys.*, vol. 36, no. 10, pp. 6254–6262, Oct. 1997.

- [3] G. Deboy, N. Marz, J.-P. Stengl, H. Strack, J. Tihanyi, and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Dec. 1998, pp. 683–685.
- [4] F. Udreă, G. Deboy, and T. Fujihira, "Superjunction power devices, history, development, and future prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 713–727, Mar. 2017.
- [5] A. G. M. Strollo and E. Napoli, "Optimal ON-resistance versus breakdown voltage tradeoff in superjunction power devices: A novel analytical model," *IEEE Trans. Electron Devices*, vol. 48, no. 9, pp. 2161–2167, Sep. 2001.
- [6] E. Napoli, H. Wang, and F. Udreă, "The effect of charge imbalance on superjunction power devices: An exact analytical solution," *IEEE Electron Device Lett.*, vol. 29, no. 3, pp. 249–251, Mar. 2008.
- [7] H. Wang, E. Napoli, and F. Udreă, "Breakdown voltage for superjunction power devices with charge imbalance: An analytical model valid for both punch through and non punch through devices," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 3175–3183, Dec. 2009.
- [8] D. Disney and G. Dolny, "JFET depletion in superjunction devices," in *Proc. 20th Int. Symp. Power Semiconductor Devices ICs*, May 2008, no. 2, pp. 157–160.
- [9] W. Saito, "Theoretical limits of superjunction considering with charge imbalance margin," in *Proc. 27th Int. Symp. Power Semiconductor Devices ICs*, May 2015, pp. 125–128.
- [10] H. Kang and F. Udreă, "True material limit of power devices—Applied to 2-D superjunction MOSFET," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1432–1439, Apr. 2018.
- [11] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Springer, 2010.
- [12] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Hoboken, NJ, USA: Wiley, 2006.
- [13] A. E. Taylor, "L'Hospital's rule," *Amer. Math. Monthly*, vol. 59, no. 1, pp. 20–24, 1952.
- [14] M. Ruff, H. Mitlehner, and R. Helbig, "SiC devices: Physics and numerical simulation," *IEEE Trans. Electron Devices*, vol. 41, no. 6, pp. 1040–1054, Jun. 1994.
- [15] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, "An assessment of wide bandgap semiconductors for power devices," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 907–914, May 2003.

Authors' photographs and biographies not available at the time of publication.