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RESEARCH ARTICLE

Method of Single Event Effects Radiation Hardened Design for DC-DC Converter Based Load Transient Detection

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Abstract — Aiming at the impact of load current change on single-event transient, the essential difference between single-event transient and load transient of DC-DC converter is deeply studied. A hardened circuit based on load transient detection is proposed. The circuit detects the load transient information in time and outputs a control signal to control the single event hardened circuit, thereby realizing the improvement of the transient characteristics of the system under dynamic conditions. Based on the 180 nm bipolar-CMOS-DMOS (BCD) process, the design and physical verification of a boost converter are completed. The experimental results show that the input voltage range is 2.9–4.5 V, the output voltage range is 5.8–7.9 V, and the load current is 0–55 mA. During load transients, the load detection circuit turns off the hardened circuit in time, avoiding system oscillation and widening the dynamic range of the hardening circuit. Under the single-event transient, the output voltage fluctuation of the system does not exceed the maximum ripple voltage, and the single-event transient suppression ability reaches more than 86%, the system can work well with linear energy transfer of about 100 MeV·cm^2/mg.
Keywords — DC-DC converter, Analog single-event transient effect, Load transient detection, Radiation hardened by design.
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I. Introduction

Transient radiation effect is usually realized by increasing the capacitance, device size and current driving capability to increase the critical electron required for generating single-event transient (SET). This type of circuit hardened comes at the expense of significant area, power, and bandwidth losses [1], [2], while minimizing these design losses requires an understanding of the circuit or system's main radiation sensitivity and potential response [3]. It is particularly challenging for complex analog and mixed-signal circuits with a large state space and potential signaling paths [4], [5] for SETs.

High-performance analog integrated circuits for applications in space radiation environments need to be robust to analog single event transient (ASET). Radiation hardening technology based on redundant design, such as triple modular redundancy (TMR) technology, provides higher reliability, but sacrifices huge area and power loss [6]–[8]. It saves the same data in three identical physical storage spaces, and then adds a judgment circuit. When the data is stored in three latches and output, the voter maker will compare and determine the three output results. The disadvantage is that its area consumption is large, however, if the area is to be saved, additional delay will be introduced. References [9] and [10] reported a hardened structure named symmetrical multi-path-splitting (SMPS). SMPS splits a node into multiple nodes, while does not increase power loss because no extra transistors are added. But both the split factor and the resistance value affect the hardening effect of the SMPS circuit.

In previous work [11], an SET hardened circuit is proposed. It works well in the steady state of the system, however, it cannot identify system working point adjust-

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ment when the load current changes. The load resistance will change the size of SETs for an operational amplifier, which depends on the magnitude of the current absorbed or supplied by the load resistor, that is, a change in the magnitude of the load current will force the operational amplifier to adjust its operating point [12], which will change its SET characteristics. The SET pulse width has a strong dependence on the node capacitance, but simply increasing the node capacitance may cause pulse width to be amplified, increasing the load capacitance alone is not an option for radiation-hardened designs [13].

Furthermore, there is no standard measure for SET in analog and mixed-signal systems, since the effects of single events depend on circuit topology, circuit type, and mode of operation. Reference [14] greatly reduces the vulnerability of the charge pump to SET by applying a control circuit. Reference [15] uses different hardening techniques to mitigate ASET in the circuit and layout. They make system design complicatedly and can only be used in limited applications. Reference [16] utilizes bulk tied to source (BTS) technology to mitigate ASET in common source amplifier in 40 nm double-well bulk CMOS process. For the N-well process, BTS technology is used to increase the layout area geometrically.

Aiming at the above problems, this work carried out experimental measurement and simulation on the Boost DC-DC converter circuit manufactured in the 180 nm Bipolar-CMOS-DMOS (BCD) process. The transient analysis under dynamic working conditions and radiation exposure is demonstrated. A circuit for single-event hardened based on load transient detection is introduced. By detecting the load transient information of the system when the hardened circuit is working, the hardened circuit is turned off in time to prevent system oscillation. This work has two characteristics: 1) An automatic SET detection and dynamic compensation method is proposed at the circuit and system level; 2) The proposed load transient detection method can distinguish single-event transients from load transients, which expands the application range of the hardened circuit in the dynamic change of the system.

This paper is organized as follows. The characteristics are analyzed with respect to load transients and SETs in Section II. The proposed circuit is described in Section III, while Section IV discusses the simulation results of the proposed circuit. Finally, Section V concludes this work.

II. Single-Event Transient and Load Transient Analysis

DC-DC converters use energy storage elements (such as inductors, capacitors) to transfer energy from the input to the output periodically and efficiently. This type of energy transfer causes the output voltage to vary in value relative to the input voltage, and it provides electrical isolation between the input and output.

In this work, there is a boost DC-DC converter, which is respectively the 2.9–4.5 V V-input (V_{IN}) and 5.8–7.9 V V-output (V_{OUT}). The topology of the boost DC-DC converter studied in this paper shown in Figure 1 includes an inductor, a power MOSFET switch, a power MOSFET synchronous rectifier, an input capacitor, an output capacitor, resistor dividers voltage feedback network and pulse width modulation (PWM) controller. In each period of the PWM output waveform, the time when the output is high is DT (D is the duty cycle, T is the system period).

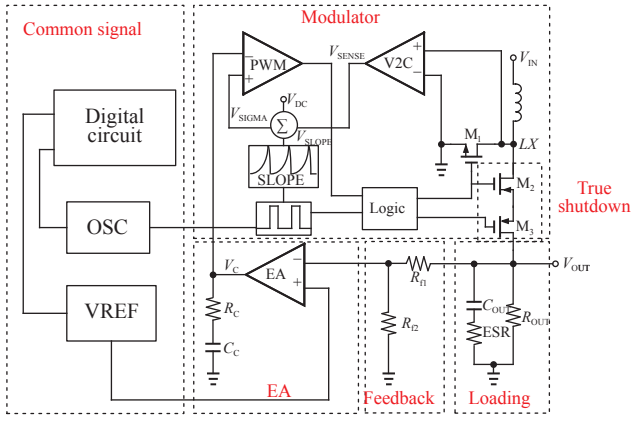

Figure 1 System framework of boost DC-DC converter.

During the charging stage, the switch M_1 is turned on, the switch M_2 is turned off, the input voltage V_{IN} appears across the inductor L, therefore, the current through the inductor rises linearly with time. Its rising rate is proportional to the ratio of input voltage to inductor value. During the discharge stage, M_1 is turned off, M_2 is turned on, the voltage across the inductor L changes suddenly to maintain the current, because the inductor current cannot change suddenly. Its output voltage expression is

$$V_{\mathrm{OUT}} = V_{\mathrm{IN}}/(1-D) \tag{1}$$

where V_{OUT} is the output voltage; V_{IN} is the input voltage. Obviously, the duty cycle is the most critical factor affecting the output voltage. When the load or input voltage changes, the feedback circuit keeps the output voltage constant by adjusting the duty cycle D.

The power loss of DC-DC converter mainly includes conduction loss, switching loss, driving loss and static loss etc. The power loss of the converter refers to the ratio of the output power to the input power. The conversion efficiency expression of the system is

$$\eta = P_{\mathrm{OUT}}/P_{\mathrm{IN}} = (V_{\mathrm{OUT}} \cdot I_{\mathrm{OUT}})/(V_{\mathrm{IN}} \cdot I_{\mathrm{IN}}) \tag{2}$$

where V_{IN} is the input supply voltage and I_{IN} is the input current. The main factor affecting the efficiency under heavy load is the conduction loss. The conduction loss of the power switch is proportional to the square of the load current. As the load current increases, the pro-

portion increases greatly. At light load, the main factors affecting the efficiency are switching loss and driving loss, which are not related to the load current and are proportional to the switching frequency. The higher the frequency, the greater the power loss. The lighter the load, the larger the proportion of switching loss and driving loss in the total loss of the power switch, resulting in lower conversion efficiency at light load.

In Figure 1, the control system with the peak current PWM controller has two loops. One is the voltage loop, including the feedback module, error amplifier (EA), frequency compensation module, and reference voltage module. The feedback signal obtained by dividing the output voltage and the error signal obtained by the error amplification of the reference voltage are sent to the PWM comparator. The other is the current loop, which includes the inductor current sampling module and the slope compensation module, and samples the current signal cycle by cycle. The current signal and the feedback signal jointly control the duty cycle.

Single event effects mainly occur in PWM controllers, and the main effect for PWM controllers is SETs. The SET pulse is superimposed on the modulation pulse, which changes the duty cycle of the system within a period of time. Further, the conduction state of the power switch is changed, so that the output voltage fluctuates or the output voltage ripple increases.

As a transient radiation effect, the SET effect will be further reflected in the dynamic response process of the system. This section gradually analyzes the difference and connection between the load transient effect and the SET effect on duty cycle and related parameters.

1. Load transient analysis

When the load current $I_{\rm OUT}$ changes in a short time, the output voltage $V_{\rm OUT}$ will change. When the load is small, the output voltage increases, and when the load is large, the output voltage decreases. The variation of the output voltage under different loads determines the performance of a power supply, and the load regulation is used in the power supply to characterize this performance index. Load regulation is defined as the ratio of $\Delta V_{\rm OUT}$ (the change of output voltage) to $\Delta I_{\rm OUT}$ (the change of output current). The unit is mV/mA, and its expression is

$$\text{Load\_R} = (\Delta V_{\rm OUT}/\Delta I_{\rm OUT}) \times 100\% \tag{3}$$

Next, this work analyzes the changes of the system parameters in the above two types of load transient processes. The relationship between the average value of the inductor current $I_{L\_\rm AVG}$ and the load current $I_{\rm OUT}$ is shown in (4).

$$I_{L\_\rm AVG} = I_{\rm OUT}/(1-D) \tag{4}$$

When the load changes from a small current to a large current in a short period of time, from the perspective of the current loop, as shown in Figure 2(a), to provide a large enough current to the output terminal, the inductor needs a larger average current which is used for freewheeling of the system. At this time, the duty cycle D of the system is reduced to obtain a larger output current. Since the inductor current cannot change abruptly, the output capacitor is discharged to provide sufficient output current, forcing the output voltage $V_{\rm OUT}$ to drop.

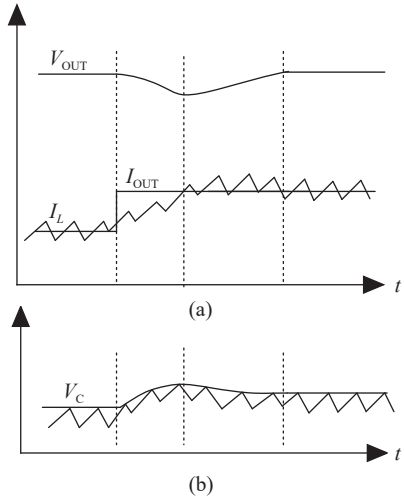

Figure 2 Transient response curve of the system when the load current changes to heavy: a) View of $V_{\rm OUT}$ and I_L following the change of $I_{\rm OUT}$; b) View of $V_{\rm C}$ and $V_{\rm SENCE}$ following the $I_{\rm OUT}$.

The voltage loop feedback voltage $V_{\rm FB}$ decreases, and the output level $V_{\rm C}$ of the EA increases, as shown in Figure 2(b), which in turn makes the inversion point of the PWM comparator lag behind, as shown in (5), when $V_{\rm SLOPE}$ and $V_{\rm DC}$ remain unchanged, due to the increase of $V_{\rm C}$, a larger $V_{\rm SENSE}$ is required to make the PWM comparator reverse. The system duty cycle D increases, and the output voltage gradually increases to a steady state.

$$V_{\rm C} > V_{\rm SIGMA} = V_{\rm SENSE} + V_{\rm SLOPE} + V_{\rm DC} \tag{5}$$

When the load changes from a large current to a small current in a short time, from the perspective of the current loop, as shown in Figure 3(a), to provide a small enough current to the output terminal, the inductor needs a smaller average current used for freewheeling of the system. At this time, the duty cycle D of the system is increased to obtain a smaller output current. Since the inductor current cannot change abruptly, the extra current is absorbed by the output capacitor, forcing the output voltage $V_{\rm OUT}$ to rise. The voltage loop feedback voltage $V_{\rm FB}$ increases, and the output level $V_{\rm C}$ of the EA decreases, as shown in Figure 3(b), which in turn advances the reversal point of the PWM comparator. As shown in (6), when $V_{\rm SLOPE}$ and $V_{\rm DC}$ remain unchanged, due to the decrease of $V_{\rm C}$, a small $V_{\rm SENSE}$ is required to make the PWM comparator reversed. The duty cycle D decreases, the output voltage gradually de-

creases to a steady state.

$$V_{\mathrm{C}} < V_{\mathrm{SIGMA}} = V_{\mathrm{SENSE}} + V_{\mathrm{SLOPE}} + V_{\mathrm{DC}} \tag{6}$$

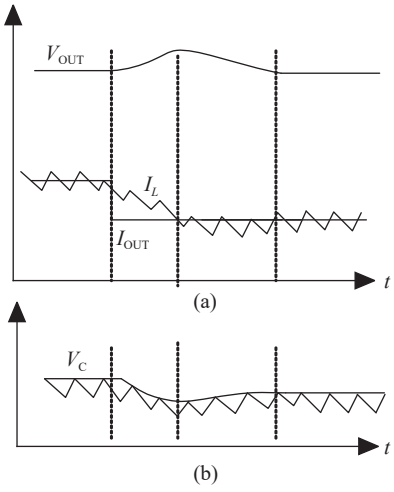

Figure 3 Transient response curve of the system when the load current changes to light. a) View of V_{OUT} and I_L following the change of I_{OUT}; b) View of V_{C} and V_{SENCE} following the I_{OUT}.

2. Single-event transient analysis

When the energetic particles bombard the output node of the EA, it will cause the output level V_{C} to jump up or down, and then the flip point of the PWM comparator will advance or lag behind, which will break the steady state of the system and cause large fluctuations in the output voltage. It will affect the normal use of the subsequent circuit and greatly affect the life of the semiconductor integrated circuit. As shown in Figure 4, when the high-energy particles generate a transient electrical pulse current I_{SET} at the EA output node, the output voltage V_{C} of the EA decreases rapidly and then slowly recovers, resulting in a long time for the output voltage V_{OUT} to return to the initial state.

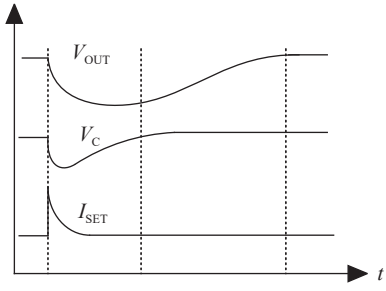

Figure 4 Single-event transient system response waveform.

Similar to the load transient process, when high-energy particles bombard the sensitive nodes of the DC-DC system, it will also cause fluctuations in the output voltage and increase in ripple voltage. The process can be described in two cases: When the particle bombardment causes V_{C} to increase, the system duty cycle D increases, and the output voltage V_{OUT} increases. Under the action of negative feedback in the voltage loop, the increase in the feedback voltage V_{FB} will cause V_{C} decreases to maintain a steady state; Similarly, when particle bombardment causes V_{C} to decrease, the system duty cycle D decreases, the output voltage V_{OUT} decreases, and the negative feedback of the system increases V_{C} to maintain a steady state.

3. Differences and connections

The essential difference between load transients and SETs lies in their generation mechanisms. SET is a kind of radiation effect in which the transient current generated when high-energy particles bombard sensitive nodes of semiconductor materials (usually devices containing reverse-biased PN junctions) induces abnormal changes in the system. As shown in Figure 5, taking an NMOS device as an example (assuming it is working in saturation region), there is a strong reverse bias electric field between the drain and the substrate. When high-energy particles bombard the sensitive node, the charge column generated on the particle path releases the carriers, causing charge diffusion and charge drift in the semiconductor material, forming a transient current from the drain to the substrate I_{SET}, causing V_{D} to decrease until it recovers. If I_{D} is regarded as an independent variable and V_{GS} is regarded as a dependent variable, then equation (7) can be used to describe the load transient. When the I_{D} changes, V_{GS} makes corresponding adjustments to ensure that "=" is established. This change is irreversible during a load transient, the operating point of the device changes from one state to another, and the device obtains a new V_{D}.

$$V_{\mathrm{GS}} = \sqrt{\frac{2I_{\mathrm{D}}}{\mu_n C_{\mathrm{ox}} w/l}} - V_{\mathrm{TH}} \tag{7}$$

When the above two transient processes occur in the DC-DC system, key parameters such as the system duty cycle D, the inductor current I_L, the output voltage V_{OUT}, and the PWM comparator flip point have similar changing trends. The difference is that the load transient process is a system fluctuation allowed by the DC-DC system, it will provide a new operating point for the system, and the system will reach a new steady state. Although the SET can be restored to the initial state by the system changing within a certain period of time, this change is not allowed by the system. It will greatly affect the work of the post-stage load circuit. How to detect and distinguish these two transient processes be-

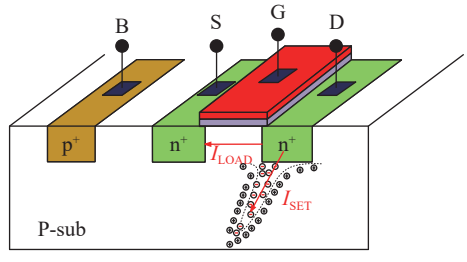

Figure 5 Schematic diagram of NMOS device.

comes the key to solving the SET problem.

III. Single Event Hardened Method Proposed in This Work

Through the previous analysis of the SET and load transient in the DC-DC system, it can be known that the change trend of V_C in the voltage loop is different in the two transient processes.

For SETs, when V_C changes cause the system to respond, V_C returns to the value in the original system steady state after a long-term change. In the load transient process, since the change of the output current I_{OUT} is an irreversible result in a transient process, the inductor current decreases, so that the V_{SENSE} changes in (5) and (6). To keep V_{OUT} unchanged, V_C needs to be adjusted to the value that makes (5) and (6) "=" hold true. Based on this change, this work proposes an SET hardening circuit as shown in Figure 6 based on previous work [11] to speed up system recovery and suppress SETs.

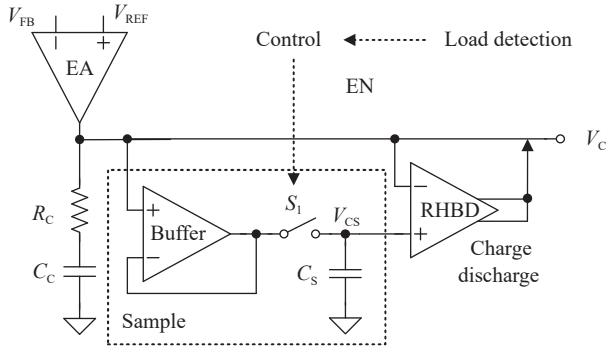

Figure 6 Circuit-level single-event hardened circuit framework.

Using the sampling capacitor C_S to store the voltage value V_{CS} of the EA output voltage V_C in the steady state of the system, the Buffer is used to isolate the V_C and V_{CS} nodes. The negative terminal of the hardened circuit is directly connected to V_C for detecting SETs. The control module is used to detect load transients. When the system generates load transients, the hardened circuit is turned off in time to prevent system oscillation.

Its working principle is: When high-energy particles bombard the EA output node to generate an SET, the hardened circuit detects the V_C voltage jump variable ΔV_C:

$$\Delta V_C = V_C - V_{CS} \tag{8}$$

When $\Delta V_C > V_t$, the hardened circuit provides a discharge current to release the excess charge of the V_C node to speed up the recovery of V_C. When $\Delta V_C < -V_t$, the hardened circuit provides a charging current to supplement the lost charge of the V_C node to speed up the recovery of V_C. $\pm V_t$ is the set threshold, which provides a certain margin to avoid circuit misoperation. Different radiation hardening requirements can be achieved by adjusting the current. The preset hardening effect of the hardened circuit proposed in this work is to quickly eliminate the influence of SET under the condition of linear energy transfer (LET) =100 MeV·cm^2/mg, so that the output voltage fluctuation is less than a maximum output voltage ripple voltage V_{ripple_max}.

In this work, two four-input comparators in Figure 7 are used to detect the load transient process and control the hardened circuit, where V_{FB} and V_{REF} are the feedback voltage and reference voltage, V_H and V_L are the comparator flipping thresholds, and EN1 and EN2 are the enable signals for the control logic of the hardened circuit. It is one of the enable signals of the hardened circuit control logic.

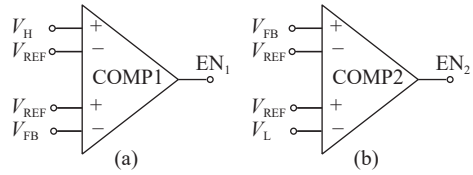

Figure 7 Schematic diagram of load transient detection circuit.

It is the load jump detection circuit topology proposed in this work in Figure 7(a), which is used to detect the process of the load current jumping from a large current to a small current. When equation (9) is established, COMP1 outputs "EN1 = 1" to close the hardened circuit. It is a load transient up-jump detection circuit topology in Figure 7(b), which is used to detect the process of the load current jumping from a small current to a large current. COMP2 outputs "EN2=1" to close the hardened circuit when equation (10) is established.

$$V_H - V_{REF} < V_{FB} - V_{REF} \tag{9}$$

$$V_{REF} - V_L < V_{REF} - V_{FB} \tag{10}$$

By setting the size of V_H, V_L can distinguish SET and load transient process. During the operation of the radiation-hardened-by-design (RHBD) circuit, the maximum fluctuation of the output voltage is V_{ripple_max}, and the result of voltage division through the voltage divider network of the feedback module is ΔV_{FB_SET}, which satisfies

$$\Delta V_{FB\_SET} = (R_{f2}/R_{f1} + R_{f2}) \cdot V_{ripple\_max} \tag{11}$$

Assuming that the maximum jump variables of the output voltage V_{OUT} during the load transient down-jump and up-jump are ΔV_{OUT_H} and ΔV_{OUT_L} respectively, then ΔV_{FB_LOAD} satisfies (12) and (13) respectively after being divided by the voltage dividing network of the feedback module,

$$\Delta V_{FB\_LOAD\_L} = (R_{f2}/R_{f1} + R_{f2}) \cdot V_{OUT\_H} \tag{12}$$

$$\Delta V_{\mathrm{FB\_LOAD\_H}} = (R_{\mathrm{f2}}/R_{\mathrm{f1}} + R_{\mathrm{f2}}) \cdot V_{\mathrm{OUT\_L}} \tag{13}$$

where, $\Delta V_{\mathrm{FB\_LOAD\_L}}$ represents the transient change of feedback voltage V_{FB} when the load jumps from high current to low current, and $\Delta V_{\mathrm{FB\_LOAD\_H}}$ represents the transient change of feedback voltage V_{FB} when the load jumps from small current to high current. Then the flipping thresholds V_{H} and V_{L} of the comparator meet the requirements of distinguishing SET and load transient when they satisfy (14) and (15) respectively.

$$\Delta V_{\mathrm{FB\_LOAD\_L}} > V_{\mathrm{H}} > V_{\mathrm{FB\_SET}} \tag{14}$$

$$\Delta V_{\mathrm{FB\_LOAD\_H}} > V_{\mathrm{L}} > V_{\mathrm{FB\_SET}} \tag{15}$$

Both COMP1 and COMP2 are realized by the four-input folded cascode comparator shown in Figure 8. The difference is only in the connection of the input to the gate signal of the tube. The gate of M_1 is connected to the threshold V_{H}, the gates of M_2 and M_3 are connected to the reference voltage V_{REF}, and the gate of M_4 is connected to the feedback voltage V_{FB}. A four-input comparator is formed by two sets of differential structures of $M_{1,2}$ and $M_{3,4}$, which are used to compare the magnitude of the differential signal $V_{\mathrm{H}} - V_{\mathrm{REF}}$ and $V_{\mathrm{FB}} - V_{\mathrm{REF}}$, and detect the transient load jump process. When the gate of M_1 is connected to the feedback voltage V_{FB}, the gates of M_2 and M_3 are connected to the reference voltage V_{REF}, and the gate of M_4 is connected to the threshold V_{H}, it is used to compare the magnitude of the differential signal $V_{\mathrm{REF}} - V_{\mathrm{L}}$ and $V_{\mathrm{REF}} - V_{\mathrm{FB}}$ and detect the load transient up-jump process. The advantage of using a four-input comparator is that the use of differential signals for comparison can well suppress the influence of noise on the performance of the comparator. Table 1 lists the device size.

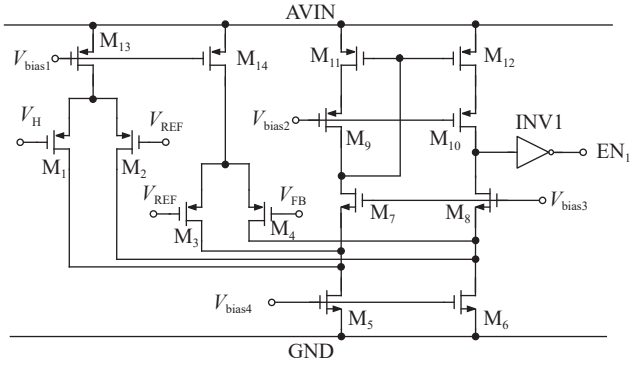

Figure 8 Load transient detection circuit.

To make any reversal of the output signals EN1 or EN2 of COMP1 and COMP2 can be used as the enable signal EN of the hardened circuit, as shown in Figure 9, the output of EN1, EN1 and the sampling clock CK of the hardened circuit sampling module after logic operation are used as the EN signal to control S_1 (transmission gate) by using a three-input OR gate.

Table 1 Device size

Name	w/l (μm/μm)	Name	w/l (μm/μm)
$M_{1,2}$	25/2	$M_{9,10}$	8/2
$M_{3,4}$	25/2	$M_{11,12}$	8/2
$M_{5,6}$	4/2	$M_{13,14}$	8/2
$M_{7,8}$	4/2	–	–

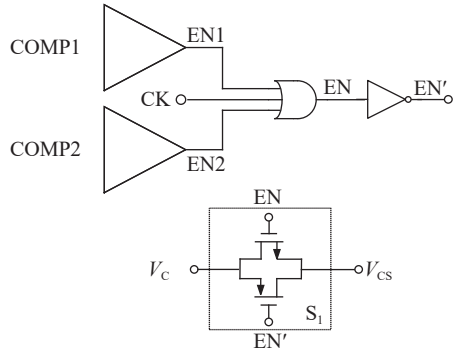

Figure 9 Hardened circuit control logic.

When the hardened circuit charges and discharges the V_{C} node when $|\Delta V_{\mathrm{C}}| > |\Delta V_t|$, the load transient detection circuit must turn over before the variation of V_{C} exceeds, and close the hardened circuit. Therefore, the inversion delay t_{delay} of the comparator needs to satisfy (16).

$$t_{\mathrm{delay}} > C_{\mathrm{C}}\mathrm{d}V_t/\mathrm{d}i_{\mathrm{C}} + t_{\mathrm{EA}} + t_{\mathrm{RHBD}} \tag{16}$$

where, $C_{\mathrm{C}}\mathrm{d}V_t/\mathrm{d}i_{\mathrm{C}}$ is the time required for the EA to compensate for the charge change on the capacitor $Q = C_{\mathrm{C}}V_t$, t_{EA} is the delay required for the EA to respond to the load transient from the input terminal to the output terminal, and t_{RHBD} is the required delay for the hardened circuit response.

When COMP1 and COMP2 meet the above conditions, the hardened circuit can be closed in time during the load transient jump process, which expands the working range of the hardened circuit, so that the hardened circuit does not interfere with the system during the dynamic process; While distinguishing SET from the load transient, ensuring the normal operation of the hardened circuit can effectively improve the system's single-event hardened capabilities.

IV. Simulation Results and Analysis

Based on the 180 nm BCD process, the proposed circuit has been designed and silicon implemented. Figure 10 shows the layout of the DC-DC converter. The die area is about 1444 μm×1100 μm. The sampling capacitor C_s is realized by poly-poly capacitor, and the resistances are realized by polysilicon resistance, which is immune to radiation effect. The EA is physically isolated from the hardened circuit, which increases the direct physical distance between the hardened circuit and the normal circuit, thereby avoiding single-event sensitivity between

the hardened circuit and the normal circuit caused by high-energy particles bombarding the chip. The hardened circuit area is 263 μm × 99 μm.

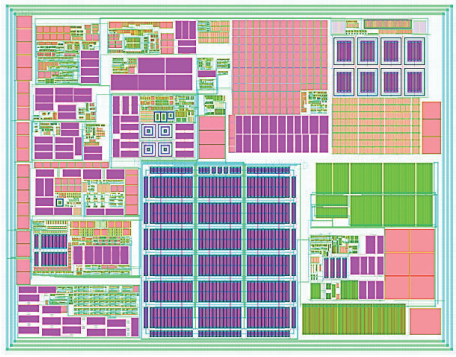

Figure 10 Layout of DC-DC converter.

The system input voltage is 2.9–4.5 V, the output voltage is 5.8–7.9 V, the system clock frequency is f = 1.5 MHz, and the load current is 0–55 mA. The following simulations are based on the specter simulation of cadence software.

In order to verify the feasibility and innovation of the proposed method, a detailed test and verification of the loop transient was carried out. At TT corner, room temperature 27 ℃, and 3.7 V input voltage, Figure 11 shows the waveform of the key signal before the system is hardened, when the input voltage is 3.7 V and the load is 55 mA, the average output voltage is 7.6015 V, and the output voltage ripple $V_{\text{ripple}} = 1$ mV. The average inductor current $I_{L\_\text{AVG}} = 120.14$ mV.

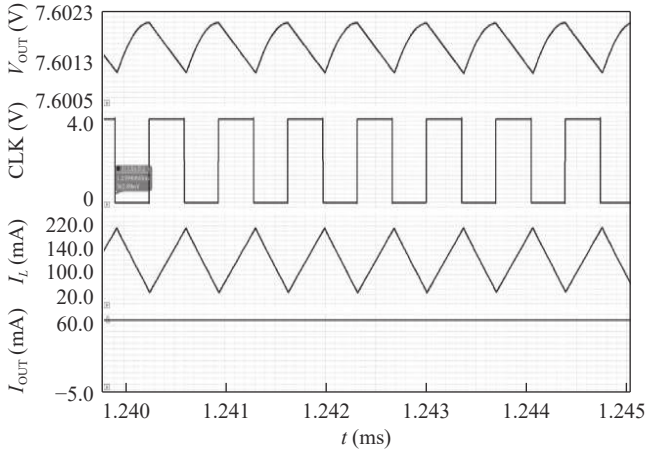

Figure 11 System key signal waveform.

According to the transient characteristics of single events, the transient current pulse is modeled using the double-exponential current model [17]–[19]. The double-exponential current can be expressed as:

$$I_t > I_0\left(\exp(-t/\tau_\alpha) - \exp(-t/\tau_\beta)\right) \tag{17}$$

where, the maximum charge collection current at I_0 is equal to $Q/(\tau_\alpha - \tau_\beta)$, where τ_α and τ_β are the rising and falling time constants of the current pulse, respectively. In this work, τ_α and τ_β are set to 500 ps and 10 ps respectively. The current model is injected into the EA output node to simulate an SET.

Figure 12 shows the double-exponential transient current pulse waveform, LET = 50 MeV·cm^2/mg, the current peak value is 905 μA, and the pulse width is about 3 ns.

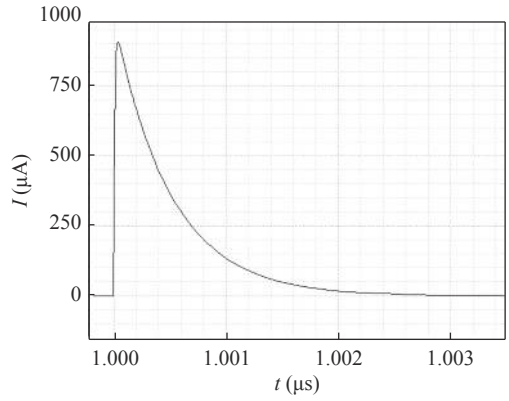

Figure 12 Single-event transient current pulse waveform.

When the system's load current changes in a short time, as shown in Figure 13, at 2 ms, the load current I_{OUT} jumps from 55 mA to 1 mA within 5 μs, and the system is forced to adjust the operating point. The maximum jump of the output voltage V_{OUT} before hardening is ΔV_{OUT} = 21.34 mV until recovery; The hardened circuit fails to recognize the adjustment of the system operating point without load transient detection circuit, the output voltage V_{OUT} has a large oscillation until the system operating point returns to the original state, that is, the load current I_{OUT} jumps again after reaching 55 mA (at 3.5 ms, the load current I_{OUT} jumps from 1 mA to 55 mA within 5 μs), it recovers slowly; The hardened circuit can identify the adjustment of the system working point in time through the load transient detection circuit, close the hardened circuit, and make the sampling module continue to follow the change of the system operating point, so that the load transient characteristics after hardened are basically consistent with those before hardened. The maximum output voltage jump is 26.99 mV, but the system recovery time is basically the same as before hardened.

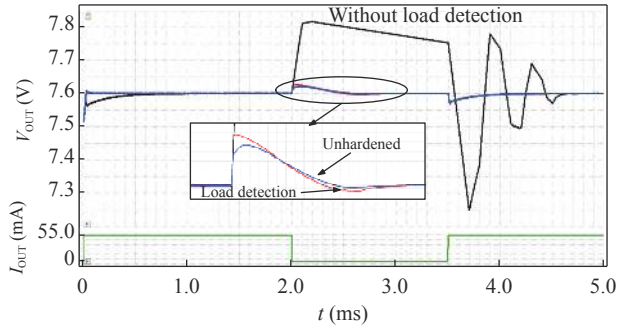

Figure 13 Post-simulation results of system load transient.

Figures 14(a) and (b) are the detection signal output waveforms of the load detection circuit during load transient up-jump and down-jump respectively. As shown in Figure 14(a), when the load current I_{OUT} jumps from 55 mA to 1 mA, COMP1 detects the load transient up-jump process, outputs a high level "EN1 = 1", and COMP2 maintains a low level "EN2 = 0", CK is the sampling clock signal, EN signal is the final output signal of the hardened circuit control module.

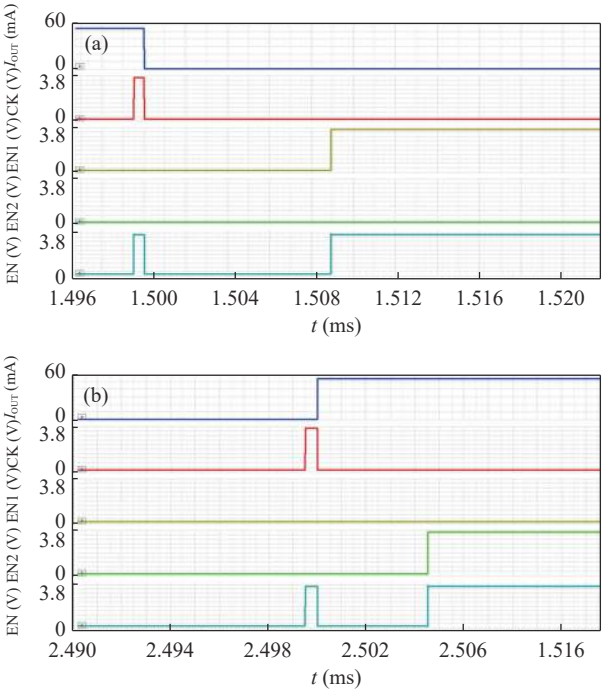

Figure 14 Output waveform of the load detection circuit.

When the load jumps up, COMP1 turns over to close the sampling switch S_1, and the sampling circuit enters the continuous sampling stage, which prevents the hardened circuit from providing charging current to the EA output node; When the load current I_{OUT} jumps from 1 mA to 55 mA, COMP2 detects the load jumping process, and outputs a high level "EN2 = 1", COMP1 keeps outputting a low level "EN1 = 0", EN flips to make S_1 close and enter the continuous sampling stage, avoiding the hardened circuit provides a discharge path to the EA output node in Figure 14(b).

In order to further verify the control effect of the load transient detection circuit on the hardened circuit, the process-voltage-temperature (PVT) verification was carried out at SS, TT, FF process corners and the temperature of −40 ℃ to 85 ℃, and the results are shown in Figures 15(a) and (b). In Figure 15(a), when the load current jumps down, the output voltage V_{OUT} tends to increase gradually. At this time, the load transient detection circuit outputs a high level "EN = 1" to close the sampling switch S_1; It is the process that the output voltage V_{OUT} tends to decrease when the load jumps up and then gradually recovers in Figure 15(b), the load transient detection circuit outputs a high level "EN = 1"

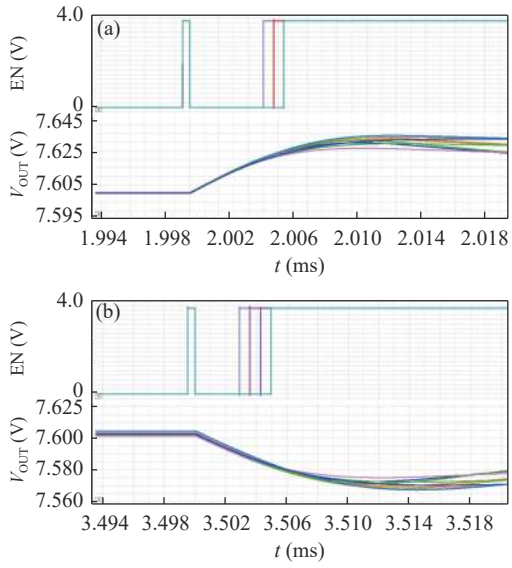

Figure 15 PVT simulation results of load transient detection circuit.

to close S_1. The simulation results in Figure 15 show that under different process angles and temperatures, the load transient detection circuit can detect load changes in time and output high level "EN = 1" in time to make the sampling module enter the continuous sampling stage.

Figure 16 shows the change waveform of the EA output voltage V_C and the sampling module sampling voltage V_{CS} when the load current is from 0 to 55 mA under the action of the EN control signal during the load transient process. The simulation results show that at 3.5 ms, the current starts to change suddenly. When the load change is detected, the EN signal is pulled high, and V_{CS} starts to follow the change of V_C, and the difference between the two is less than 5 mV, which is less than the start-up threshold V_t of the hardened circuit. The hardened circuit is in standby.

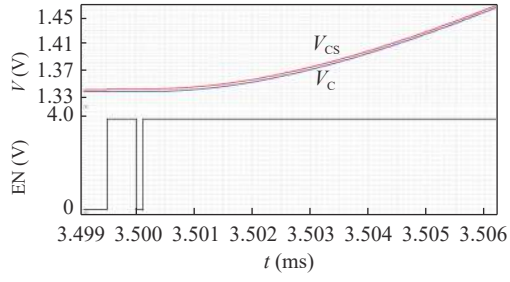

Figure 16 Output waveform of load jump sampling module.

With LET = 50 MeV·cm^2/mg, the SET PVT characteristics in the system were verified, as illustrated in Figure 17. In the SS process corner, the influence of ASET on the output voltage is greater than that of the TT and FF process corners, and the worst case is that the power supply voltage V_{IN} = 3.7 V and T = 85 ℃.

The results of output voltage changed normal and hardened are shown in Figure 18, which is a comparison

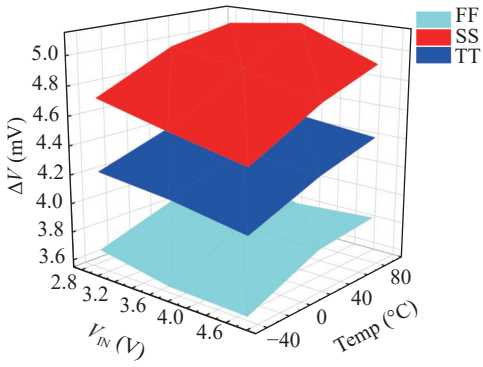

Figure 17 Single-event transient results of PVT.

of the effect before and after hardened under the worst case of PVT under different LET values. The results show that with the increase of the LET value, the fluctuation value of the normal output voltage V_{OUT} gradually increases; The offset of the hardened output voltage is suppressed within 1 mV, and the SET amplitude can be suppressed to more than 86%.

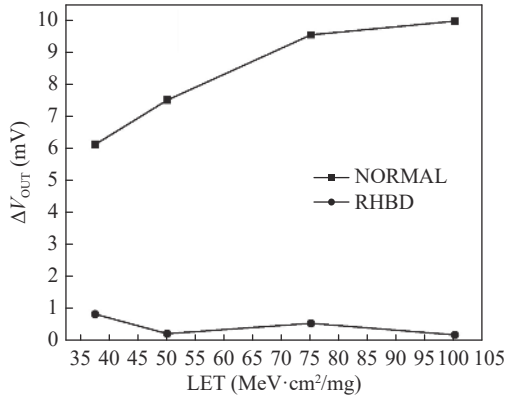

Figure 18 The results of different LET on the output voltage in the worst case of PVT.

At TT process corner, 25 ℃, $V_{\mathrm{IN}} = 3.7$ V, $V_{\mathrm{OUT}} = 7.6$ V, the conversion efficiency of the chip is simulated in the whole load range, the results are shown in Figure 19, the

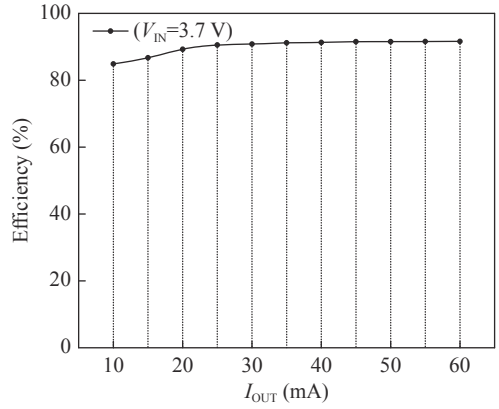

Figure 19 System conversion efficiency.

conversion efficiency of the system designed in this paper can reach 91.6%.

In this work, the proposed circuit is 84.5% of the area of the EA (220 μm × 110 μm). It is 1.639% of the system area (1444 μm × 1400 μm). This work has a great advantage in area. The power loss of the circuit proposed is 153 μA, which is 455% of the power loss of the EA (33.6 μA). Compared with system, power dissipation increased by 0.12% at maximum load. Normally, the voltage variation amplitude of ASET to EA output node is 1.641 V, after hardening, the voltage variation amplitude is reduced to 0.221 V.

The characteristics of this work are summarized and compared with other state-of-art techniques in Table 2. Compared with these techniques, this work can tolerate particle energies up to LET = 100 MeV·cm^2/mg. The pulse magnitude of ASET was reduced by more than 86%. The power and area losses are negligible.

V. Summary

Aiming at the problem that the hardened circuit cannot recognize the transient information of the system in the previous work, this work analyzes the SET and load transient characteristics in the DC-DC converter, and studies the influence of the two on the loop response.

Table 2 References comparison

Parameter	This work	[10] (2022)	[14] (2018)	[15] (2022)	[16] (2020)
Process	180 nm BCD	28 nm CMOS	130 nm CMOS	28 nm CMOS	40 nm CMOS
Application	DC-DC	LDO	Charge pump	Band-gap	CS amplifier
Method	Current compensation	SMPS	Control circuit	–	BTS
Harding level	Circuit	Circuit	Circuit	Circuit and layout	Transistor
Unhardened (V)	1.641	0.207	0.101	0.65	0.518
Hardened (V)	0.221	0.04	0.01	0.09	0.381
Tolerance (%)	>86%	80.8%	90.1%	86.15%	62%, 75.8%*
LET (MeV·cm^2/mg)	100	–	50	76.3	30
Power (comparing with the original structure)	0.12% increment	1.75% increment	–	450 μW**	Negligible
Area (comparing with the original structure)	1.64% increment	–	20% increment	230 μm×95 μm**	Negligible

Note: *Pulse width reduced. **Unhardened area and power loss are not found.

According to the analysis and verification results, a load transient detection method is proposed at the circuit level. By detecting the load transient information of the system when the hardened circuit is working, the hardened circuit is turned off in time, and the application range of the hardened circuit in the dynamic change of the system is realized, which broadens the scope of application of the hardened circuit. Based on the 180 nm BCD process, the circuit design and comprehensive verification are completed. The results show that the proposed method can suppress the influence of SET on the converter. Especially, the hardened circuit does not affect the normal operation of the system under the dynamic change of the system load. The system can be immune SET of LET = 100 MeV·cm^2/mg, the output voltage fluctuation does not exceed one ripple voltage, and the suppression of SET amplitude reaches more than 86%.

Acknowledgements

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