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RESEARCH ARTICLE

Realization of Complete Boolean Logic and Combinational Logic Functionalities on a Memristor-Based Universal Logic Circuit

Xiaojuan LIAN, Chuanyang SUN, Zeheng TAO, Xiang WAN, Xiaoyan LIU, Zhikuang CAI, and Lei WANG

College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210023, China

Corresponding author: Lei WANG, Email: leiwang1980@njupt.edu.cn
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Abstract — Memristors are a promising solution for building an advanced computing system due to their excellent characteristics, including small energy consumption, high integration density, fast write/read speed, great endurance and so on. In this work, we firstly design three basis logic XNOR1, XNOR2 and XOR gates by virtue of memristor ratioed logic (MRL), and further construct 1-bit numerical comparators, 2-bit numerical comparators and full adder 1 based on the above XNOR1, XNOR2 and XOR gates. Furthermore, we propose and design a universal logic circuit that can realize four different kinds of logic functions (AND, OR, XOR, XNOR) at the same time. Subsequently, a full adder 2 is built using XOR function of this universal logic circuit. Compared with the traditional CMOS circuits, the universal logic circuit designed in this work exhibits several merits such as fewer components, less power, and lower delay. This work demonstrates that memristors can be used as a potential solution for building a novel computing architecture.
Keywords — Memristor, Universal logic circuit, Memristor ratioed logic, Numerical comparator, Full adder.
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I. Introduction

Since the invention of the transistor, it has been widely used in various electronic devices [1]. With the appearance of integrated circuits, the volume and power consumption of traditional circuits are greatly reduced, which promotes the rapid development of the field of microelectronics, and the size of transistors is gradually reduced to the nanometer level. This allows hundreds of millions of transistors to be integrated into a chip of unit area. Gordon Moore came up with what is known as Moore's Law, which predicts that the number of transistors on a chip doubles every 18 months [2]. However, up to now, Moore's Law is being challenged in terms of multiple aspects such as materials, processes and costs [3]. Similarly, the traditional von Neumann structure is constrained by Moore's Law. This kind of computing architecture requires frequent data transfer between computing units and storage units, which seriously affects the power consumption and speed of the system [4]. In order to address such challenges, many strategies have been proposed in the post-Moore era, including optimizing the preparation process of device circuits or exploring a novel logical computing architecture [5].

Among various solutions, the use of memristors to build a novel logical computing architectures is considered as one of the best means. Memristor, originally proposed by Leon O. Chua in 1971 [6], was first physically implemented by Williams team of Hewlett-Packard (HP) Laboratory in 2008 [7]. It is considered to be the fourth basic electronic component in addition to resistance, capacitance and inductance. Nowadays, memristors are considered to be one of the most competitive candidates for the next generation of low-power and high-density stor-

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age devices because of their simple structure, ultra-low switching speed, low power consumption, continuously adjustable conductance state and compatibility with existing complementary metal oxide semiconductor (CMOS) processes [8]–[10]. The storage function of memristors depends on their electronic properties, and under external excitation, they can switch reversibly between two different resistance states. The two resistance states correspond to the 0 and 1 states in a digital circuit, respectively [11].

At present, two types of memristors categories can be directly applied for logic circuits applications, i.e., state logic circuit and level logic circuit. The state logic is represented by the high resistance R_{off} and low resistance R_{on} of the memristor, which are considered as logics "0" and "1", respectively. The state logic circuit mainly includes the material implication logic operation (IMP), memristor-aided logic (MAGIC) and memristor-as-driver gates (MAD) [12]. The IMP requires multiple steps to implement the required logic, including operations such as set 0, set 1, and clear, which increases the time for logical calculations during the process [13], [14]. MAGIC and MAD logics, on the other hand, require a write to the memristor before each operation, and their circuit structures are not conducive to large-scale integration [15]–[17]. In contrast, the level logic is represented by the voltage level, where the high voltage V_{high} and low voltage V_{low} are considered as logics "1" and "0", respectively. The memristor ratioed logic (MRL) is mainly the level logic that is compatible with current CMOS technologies because its logic states are defined as all voltage levels [18]. Compared with traditional CMOS circuits, the MRL-based circuits have many advantages, such as lower power consumption, higher integration density, and fewer devices [19]. Compared with the state logic circuits, the MRL-based circuits also have great advantages, which can complete the combinational logic functionalities without complex peripheral circuits and more operation steps [20], [21].

In this work, we leverage the computational principles of MRL to harness the unique advantages offered by memristors as fundamental computational logic elements. We integrate these advantages with the voltage-controlled characteristics of metal oxide semiconductor (MOS) technology to conceive the hybrid circuit. Firstly, we proposed three basic logic XNOR1, XNOR2 and XOR gates on the basis of the MRL design, and further built 1-bit numerical comparators, 2-bit numerical comparators and full adder 1 based on the above XNOR1, XNOR2 and XOR gates. In addition, we designed a universal logic circuit that can realize four different kinds of logic functions (AND, OR, XOR, XNOR) at the same time, and then a full adder 2 was further built using XOR function of this universal logic circuit. Compared with traditional CMOS circuits, the logic circuits designed in this paper exhibit fewer devices, less power, and lower delay. These innovative logic circuits hold immense potential for emerging technologies, particularly in the domain of associative memory. They offer enhanced capabilities for tasks such as pattern recognition, information retrieval, and cognitive computing, thereby driving innovation in memory-dependent fields [22]–[24].

II. Logic Circuit Modelling Strategies

1. Electrical characteristics of the memristor model

Here the well-known HP memristor model is adopted. In 2008, Strukov *et al.* [7] at HP Laboratories designed and fabricated a memory device based on $Pt/TiO_2/Pt$ sandwich stack structure. The conduction mechanism of $Pt/TiO_2/Pt$ devices can be explained by the motion of TiO_2/TiO_{2-x} interface caused by oxygen vacancy migration under external electric field [7]. Under the action of voltage excitation, the thickness of TiO_2 and TiO_{2-x} changes, that is, the proportion in the functional layer changes [25]. The mathematical expression is

$$M(t) = \left(R_{\text{on}} \frac{w(t)}{D} + R_{\text{off}} \left(1 - \frac{w(t)}{D}\right)\right) \tag{1}$$

where $w(t)$ is the thickness of the TiO_{2-x} film; R_{on} is equivalent to the resistance of the doped layer; R_{off} is equivalent to the resistance of the undoped layer; D is total thickness of the film. The differential equation satisfied by $w(t)$ is

$$\frac{\mathrm{d}w(t)}{\mathrm{d}t} = \mu_v \frac{R_{\text{on}}}{D} i(t) f(w) \tag{2}$$

where μ_v is the average ion mobility. Since the memristor is a nano device, when a small voltage is applied into the memristor externally, a large electric field will be generated in the resistance switching layer, resulting in the nonlinear movement of the storage ions. To more accurately simulate ion migration, we can simulate the nonlinear motion of ions by multiplying the right side of (2) by a Strukov window function $f(w) = 1 - 4(w/D - 0.5)^2$ [12], and thus the pinch hysteresis loop of the oblique "8" is obtained after simulating the nonlinear transition model constructed above. In the context of our proposed logic operation method, it is imperative to highlight that the most substantial factor influencing the accuracy of logic operations is the OFF/ON ratio exhibited by the memristor. Through extensive simulation and analysis, we can obtain that when $R_{\text{on}} = 1$ kΩ, the logic circuit can guarantee the correct logic output as long as R_{off} varies between 30 kΩ and 120 kΩ. Therefore, the parameters of HP memristor model used in this work are $R_{\text{on}} = 1$ kΩ, $R_{\text{off}} = 100$ kΩ and $D = 2$ nm respectively. The parameters of the NMOS transistor in the simulation are $L = 180$ nm and $W = 220$ nm respectively.

2. Design principles of the MRL

The concept of MRL was proposed by Kvatinsky *et al.* in 2012 arising from the nonlinear property of the

memristor that is similar to the transistor operated in the triode region [18]. One of the standout features of MRL logic lies in its ability to achieve AND and OR operations with just two components, leading to a substantial reduction in the overall device counts compared to traditional CMOS logic gates, especially for simple logic operations. Consequently, when tasked with the design of complex combinatorial logic circuits, the advantages of reduced device count become increasingly evident, directly resulting in a reduction in circuit area.

Figure 1(a) represents AND gate. When $V_{in1} = V_{in2} =$ "1"/"0", $V_{out} =$"1"/"0"; when $V_{in1} =$"1", $V_{in2} =$"0", the current flows from M1 to M2. In this case, M1 shows R_{off}, while M2 exhibits R_{on}. The output voltage is therefore calculated according to the voltage division principle [18]:

$$V_{out} = \frac{R_{on}}{R_{on} + R_{off}} V_{high} \approx 0 \tag{3}$$

Figure 1(b) represents OR gate. When $V_{in1} = V_{in2} =$ "1"/"0", $V_{out} =$"1"/"0"; when $V_{in1} =$"1", $V_{in2} =$"0", the current flows from M3 to M4. In this case, M3 shows R_{on}, while M4 exhibits R_{off}. The output voltage is therefore calculated according to the voltage division principle [18]:

$$V_{out} = \frac{R_{off}}{R_{on} + R_{off}} V_{high} \approx 1 \tag{4}$$

Since MRL achieves its logic function based on voltage calculation, this feature makes MRL circuits have good compatibility with CMOS circuits. Based on this, Kvatinsky *et al.* further implemented NAND and NOR logics by adding a CMOS inverter in [18], as shown in Figure 1(c) and 1(d).

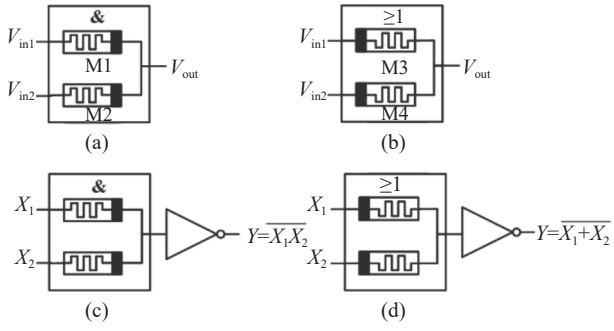

Figure 1 (a) AND, (b) OR, (c) NAND, and (d) NOR gates.

III. Memristor-Based Universal Logic Circuit

Using memristors to construct the basic digital logic gates is the basis of realizing complex combinatorial logic gates, and it is also one of the solutions to building in-memory computing devices. In this part, we further designed three basic logic gates to achieve XNOR and XOR functions, named as XNOR1, XNOR2 and XOR respectively, as shown in Figure 2. The working principle is introduced in detail below.

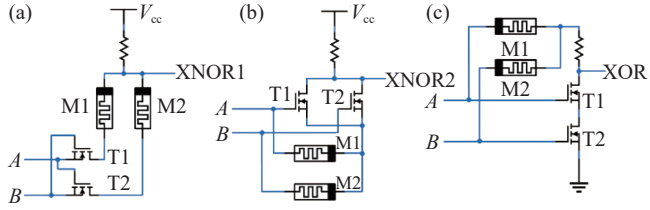

Figure 2 (a) XNOR1, (b) XNOR2, and (c) XOR gates.

For XNOR1 shown in Figure 2(a), i) when $A = B =$ "0", transistors T1 and T2 are both turned off, and the level of the output point is pulled to V_{cc}, resulting in XNOR1 ="1"; ii) when $A = B =$"1", the whole circuit is in a high-level environment, making XNOR1 ="1"; iii) when $A =$"1", $B =$"0", transistor T1 is turned off, and transistor T2 is turned on. The resistance state of M1 remains unchanged, and the resistance state of M2 is set to R_{on} , leading to XNOR1="0"; iv) when $A =$"0", $B =$"1", transistor T2 is turned off, while transistor T1 is turned on. The resistance state of M2 remains unchanged, and M1 resistance state is set to R_{on}, resulting in XNOR1 = "0".

The working principle of XNOR2 gate illustrated in Figure 2(b) is completely different from the XNOR1. For XNOR2, M1 and M2 form an AND gate. Only when $A = B =$"1", the drain terminal of the transistor shows a high level, otherwise it is a low level. At this time the circuit is in a high-level environment, thus XNOR2="1". Besides, the two parallel transistors are turned off at the same time only when $A = B =$"0", blocking the path between the output and the OR gate. This makes the output point level pulled to V_{cc} at this time, causing XNOR2 ="1". When $A =$"1", $B =$"0" or $A =$"0", $B =$ "1", there is a conductive path connecting OR gate at the output point, then XNOR2 ="0".

The XOR gate shown in Figure 2(c) is designed according to the dual structure of XNOR2. The OR gate composed of M1 and M2 is in low level only when $A = B =$"0", or it is in high level. At this time the circuit is in a low-level environment and XOR="0". In addition, the two transistors connected in series are turned on at the same time only when $A = B =$"1", thus forming a path between the output point and ground, and resulting in XOR="0"; when $A =$"1", $B =$"0" or $A =$"0", $B =$"1", there is no conduction path, consequently making XOR ="1".

Compared with the XNOR and XOR logic gates proposed in the previous literatures [26]–[30], aforementioned logic gates XNOR1, XNOR2 and XOR designed in this work use fewer memristors and transistors, as shown in Table 1 and Table 2. In addition, we conducted power and area consumption calculations for XNOR1, XNOR2, and XOR gates. For the circuit simulations performed in Cadence Virtuoso, calculating power consumption for transistors or resistors is a straightforward process. This involved exporting transient power waveform

Table 1 Quantity comparison of transistors and memristors of different XNORs

Device type	[27]	[29]	[30]	XNOR1	XNOR2
Transistor	6	3	3	2	2
Memristor	2	4	3	2	2

Table 2 Quantity comparison of transistors and memristors of different XORs

Device type	[26]	[28]	[29]	XOR
Transistor	4	2	3	2
Memristor	2	6	4	2

data directly from Cadence and subsequently computing the average power using the "average" function. However, the retrieval of power waveform data for modeled memristors proves to be less straightforward. In these instances, we calculated the average power consumption for each memristor by determining the voltage difference across its terminals and multiplying it by the transient current flowing through the memristor, as per the formula $P_{\text{average}} = \text{average}\left(\Delta U_{\text{tran}} \times I_{\text{tran}}\right)$. Then, we summed up the power consumption for each module. As a result, the power consumption values are as follows: XNOR1: 22.64 μW; XNOR2: 36.28 μW; XOR: 25.77 μW.

Concerning the device area calculations, the individual memristor occupies an area of 0.0011 μm^2 [31], while transistors, determined by their W/L ratio, have an area of 0.0396 μm^2. Additionally, the resistors of 50 kΩ used in the work encompass an area of 0.4 μm^2. Therefore, XNOR1, XNOR2, and XOR gates that employ an equal number of components have an approximate device area size of 0.5 μm^2.

Furthermore, we simulated the waveforms of the three basic logic gates, as shown in Figure 3. It is worth noting that there exist some unwanted spikes in XNOR1 gate when the resistance state is changed, but not observed in XNOR2 gate. This can be explained by different switching speed between memristors and transistors. For the XNOR1 gate, when $A =$"0", $B =$"1", $R(\text{M1}) = R_{\text{on}}$, $R(\text{M2}) = R_{\text{off}}$. When $A = B =$"0", M1 maintains the previous low-impedance state unchanged, while M2 switches to a low resistance state due to the faster switch speed of memristor. Accordingly, the output voltage is first briefly reduced to lower voltage level, and then returns to a high voltage level as the transistor is completely turned off.

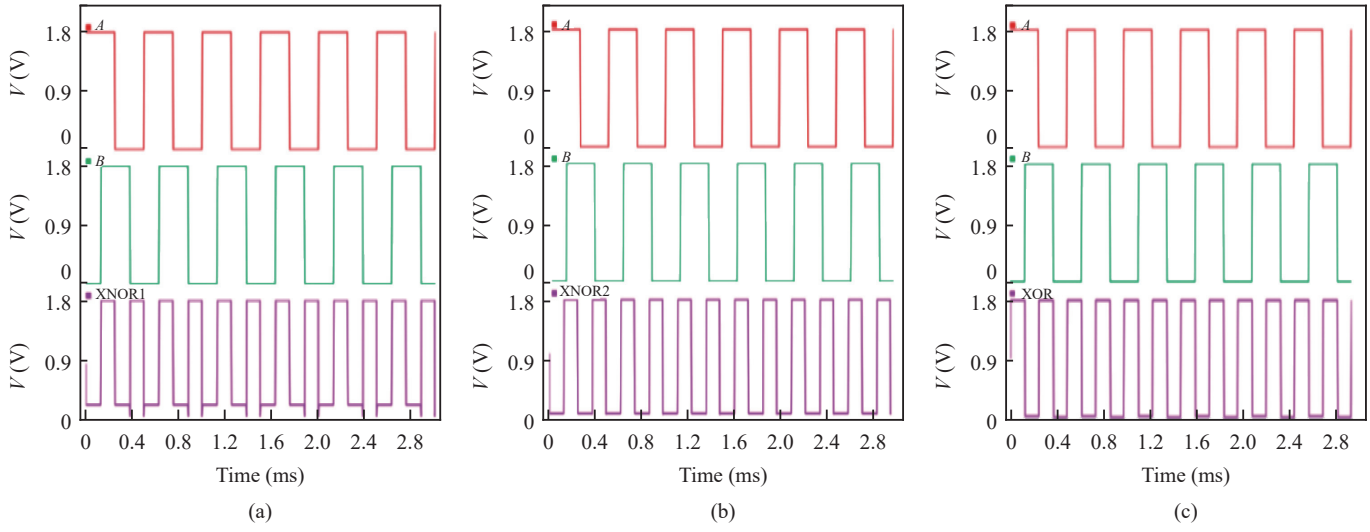

Figure 3 The simulation waveforms of (a) XNOR1 gate; (b) XNOR2 gate and (c) XOR gate.

IV. Combinational Logic Circuit Based on XNOR1/XNOR2/XOR Design

Combinational logic circuits are one of the key components to realize any digital logic circuits. Among them, adder and numerical comparator play a key role in combinational logic circuits [32]. In this section, we designed a memristor-based logic circuit using XNOR and XOR gates proposed in Section III. Two kinds of 1-bit numerical comparators based on XNOR1 and XNOR2 gates have been designed respectively. We further extended to 2-bit numerical comparators on the basis of the designed 1-bit numerical comparators. In addition, we designed a 2-bit full adder using XOR logic gate.

1. Numerical comparator based on XNOR1/XNOR2 design

In digital circuits, two binary inputs (A, B) are usually compared to determine their output. A circuit with this logic function is called a numerical comparator. The expression of input and output for a 1-bit numeric comparator is

$$Y_0\left(A > B\right) = A\overline{B} \tag{5}$$

$$Y_1\left(A = B\right) = \overline{A}\,\overline{B} + AB \tag{6}$$

$$Y_2\left(A < B\right) = \overline{A}B \tag{7}$$

Through (6), it is noticed that when $A = B$, the

output logic is consistent with the logic expressed by $A \odot B$. Therefore, based on the XNOR1/XNOR2 proposed in Section III, two kinds of 1-bit numerical comparators were built, as shown in Figure 4.

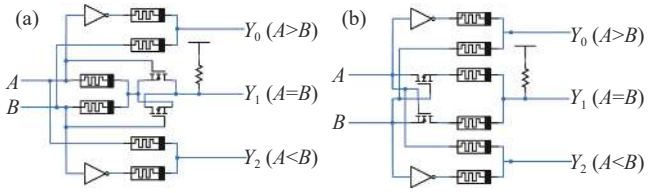

Figure 4 (a) 1-bit numerical comparator built by XNOR1 gate; (b) 1-bit numerical comparator built by XNOR2 gate.

Similarly, a 2-bit numerical comparator that can compare 2-bit binary numbers has two 2-bit inputs, i.e., A_1A_0 and B_1B_0, respectively. The truth table is shown in Table 3, and the logic expression is as follows:

$$Y_0\,(A > B) = A_1\overline{B_1}\,(A_1 \odot B_1)\,A_0\overline{B_0} \tag{8}$$

$$Y_1\,(A > B) = \overline{A_1}B_1 + (A_1 \odot B_1)\,\overline{A_0}B_0 \tag{9}$$

$$Y_2\,(A = B) = (A_1 \odot B_1)(A_0 \odot B_0) \tag{10}$$

Table 3 2-bit numeric comparator truth table

Input				Output		
A_1	B_1	A_0	B_0	$Y_0\ (A > B)$	$Y_1\ (A < B)$	$Y_2\ (A = B)$
$A_1 > B_1$		Random		1	0	0
$A_1 < B_1$		Random		0	1	0
$A_1 = B_1$		$A_0 > B_0$		1	0	0
$A_1 = B_1$		$A_0 < B_0$		0	1	0
$A_1 = B_1$		$A_0 = B_0$		0	0	1

The extended 2-bit numerical comparators are illustrated in Figure 5. Due to the inevitable voltage division effect of the MRL, the original signal level of the output terminal also causes the presence of unwanted spikes, and thus two additional NOT gates have been added to mitigate the output signal. Compared to traditional CMOS logic circuits [33], both 2-bit numerical comparator circuits use fewer devices (only 22 memristors, 28 transistors and 2 resistors) and consume less power (0.135 mW for the circuit of Figure 5(a) and 0.146 mW for the circuit of Figure 5(b)).

Full adder is a basic combinational logic circuit that uses gate circuit to realize the addition of two binary numbers and generate the sum. It is also one of the most popular circuits based on memristor designs. Its logical expression is as follows:

$$S = A \oplus B \oplus C_{i-1} \tag{11}$$

$$C_i = AB + C_{i-1}\,(A \oplus B) = AB + C_{i-1}(A + B) \tag{12}$$

According to above expressions, we designed a full adder 1 combined with the XOR gate proposed in Section III, as shown in Figure 6. Compared with the full adder made by CMOS process [34], a full adder circuit (named as full adder 1) proposed in this section uses only 10 memristors, 16 transistors and 2 resistors to realize the function of full addition of binary numbers. There has been a noticeable decrease in the number of transistors used. Furthermore, we summed up the power consumption for each module, and the resulting data is presented in Figure 6.

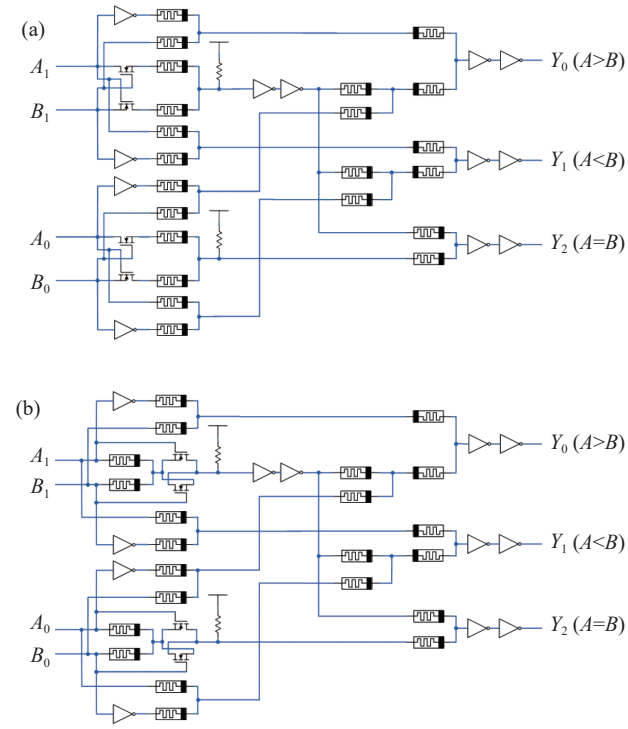

Figure 5 (a) 2-bit numerical comparator built using XNOR1 gate; (b) 2-bit numerical comparator built using XNOR2 gate.

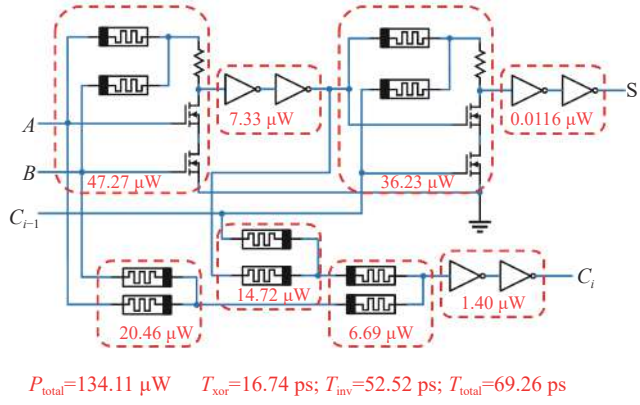

Figure 6 Full adder 1 on the basis of proposed XOR gate.

When calculating circuit timing relationships, we defined the delay time as the time interval between the moments when the input and output signals transitioned to their 50% states. This delay time calculation specifically pertained to the path from C_{i-1} to S, which included the first-level XOR gate and a pair of inverters. Consequently, the total delay time was the sum of the

delay times associated with these two segments. Detailed delay time data for individual segments within this path is provided in Figure 6.

2. Simulation results and analysis

In addition, we simulated and analyzed the proposed combinational logic circuits in Section IV by Cadence simulation software. The simulation results show that two 1-bit numerical comparators can correctly realize the comparison function of two 1-bit binary inputs, as shown in Figures 7(a) and (b). Due to the voltage division, the simulation waveforms of two 1-bit numerical comparators show a "staircase" shape when the output Y_0 and Y_2 are at low level. However, such signal fluctuation is still far smaller than the defined low logic level, and would not cause logic errors. Figures 7(c) and (d) show the simulation results of two 2-bit numerical comparators that can correctly realize the comparison function of 2-bit binary numbers.

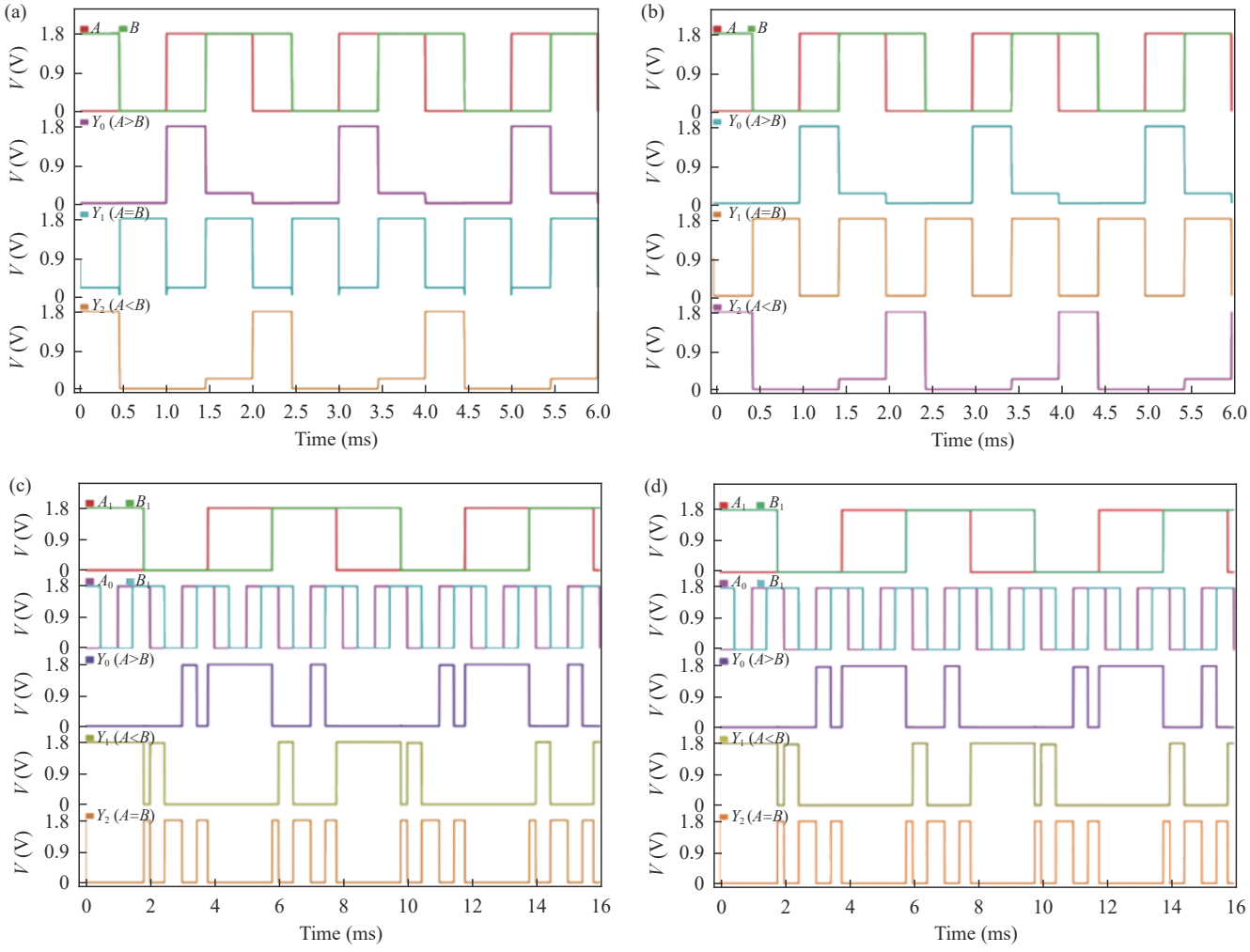

Figure 7 Simulation results of 1-bit numerical comparators built by (a) XNOR1 gate and (b) XNOR2 gate; Simulation results of 2-bit numerical comparators designed by (c) XNOR1 gate and (d) XNOR2 gate.

We further calculated the power consumption of the 2-bit numerical comparators by solving the formula of average circuit power consumption $P_{\text{average}} = P_{\text{resistance}} + P_{\text{transistor}} + P_{\text{memristor}}$, and obtained the power consumption of 0.135 mW for the circuit of Figure 5(a) and 0.146 mW for the circuit of Figure 5(b).

Figure 8 shows the simulation waveform of full adder 1 designed in this section. The output sum bit S and the carry bit C_i are in the correct logical relationship, realizing the function of a full adder. Compared to the MRL-based 1-bit full adder [35], the full adder 1 designed in this section exhibits lower power consumption and delay, as shown in the table of next section.

V. Memristor-Based Universal Logic Circuit

At present, the proposed digital circuits based on memristors can only achieve one or two logic functions [36]–[38]. Realization of more logic functions usually requires more devices and circuit modules, which consumes more energy. Therefore, in this section we propose a universal logic circuit that can realize four differ-

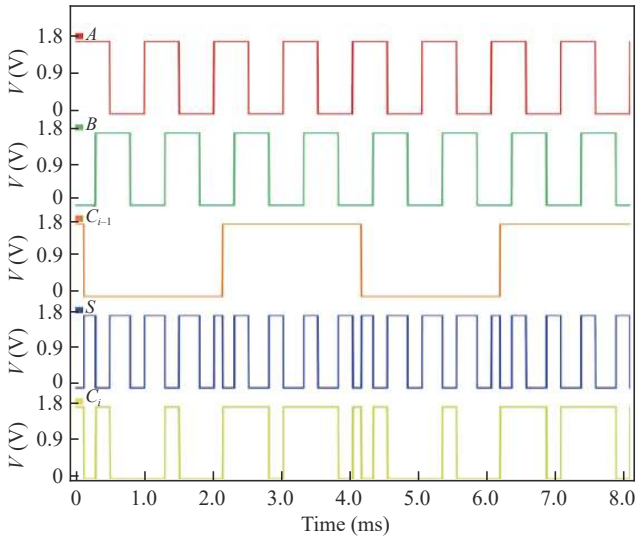

Figure 8 The simulation waveform of full adder 1 built by XOR gate.

ent kinds of logic outputs (AND, OR, XOR, XNOR) at the same time. Such designed circuit enables much higher integration density and much lower power consumption than previously reported counterparts, as shown in Figure 9.

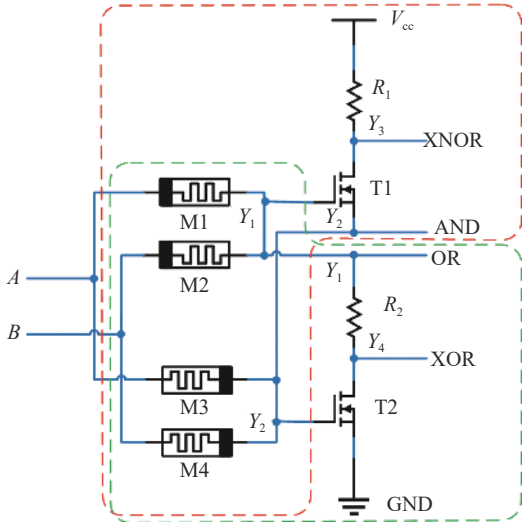

Figure 9 A memristor based universal logic circuit.

The working principle of this universal logic circuit is described below. After inputting signals to terminal A and terminal B, M1 and M2 first realize the function of OR, and M3 and M4 realize the function of AND. Then the OR signal is input to the gate terminal of the T1 transistor and the source terminal of the T2 transistor respectively, whereas the AND signal is input to the source terminal of the T1 transistor and the gate terminal of the T2 transistor respectively. Such connections assign the output Y_3 with XNOR function (red frame): i) when $A=B=$"0", $Y_1=Y_2=$"0", and $V_{GS}\approx$"0" < V_{TH} (V_{TH} is the threshold voltage of the transistor); the transistor T1 is therefore in the off state, making $Y_3=$"1"; ii) when $A=$"1", $B=$"0", then $Y_1=$"1", $Y_2=$"0", and $V_{GS}\approx$"1" > V_{TH}; the transistor T1 is thus in the on state, $Y_3=$"0"; iii) when $A=$"0", $B=$"1", then $Y_1=$"1", $Y_2=$"0" is similar to ii), causing $Y_3=$"0"; iv) when $A=B=$"1", $Y_1=Y_2=$"1", and $V_{GS}\approx$ "0" < V_{TH}. T1 in this case is turned off, and $Y_3=$"1".

Similarly, above design also endows the output Y_4 with XOR function (green frame): i) when $A=B=$"0", $Y_1=Y_2=$"0", and $V_{GS}\approx$ "0" < V_{TH}; the transistor T2 is therefore in the off state, driving $Y_4=$"0"; ii) when $A=$ "1", $B=$"0", $Y_1=$"1", and $Y_2=$"0", while $V_{GS}\approx$"0" < V_{TH}. Accordingly, the transistor T2 is cut off, making $Y_3=$"1"; iii) when $A=$"0", $B=$"1", the output case is the same as ii), $Y_3=$"1"; iv) when $A=B=$"1", $Y_1=Y_2=$"1", and $V_{GS}\approx$ "1" > V_{TH}; the transistor T2 is thus turned on, making $Y_3=$"0".

The simulation waveform of this universal logic circuit is shown in Figure 10. As can be clearly seen from Figure 10, the waveform shows the correct logic relationship. Our universal logic circuit enables multiple logic functions secured in the same circuit structure, which significantly improves the integrated density of the logic circuit and reduces the power consumption. Furthermore, we constructed another full adder circuit (named as full adder 2) using XOR function of the universal logic circuit (the green frame part), as shown in Figure 11, and its simulation waveform is given in Figure 12.

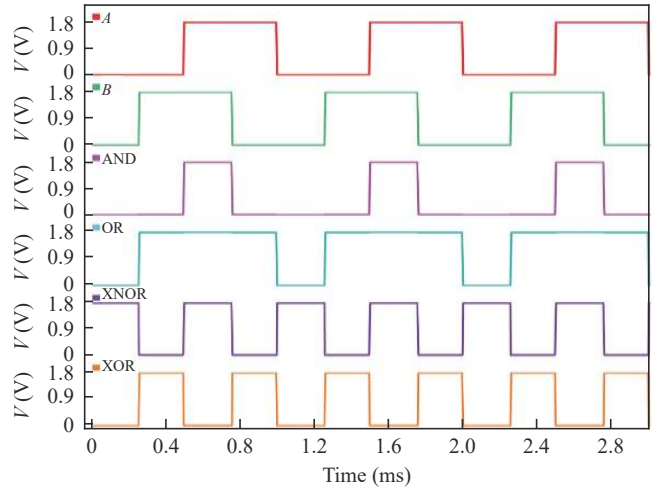

Figure 10 The simulation waveform of the general logic circuit.

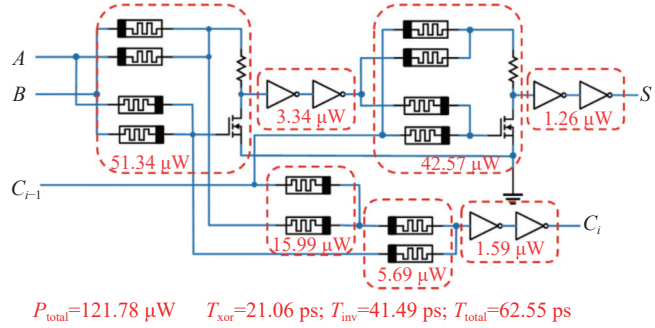

Figure 11 A full adder 2 using XOR function of the universal logic circuit.

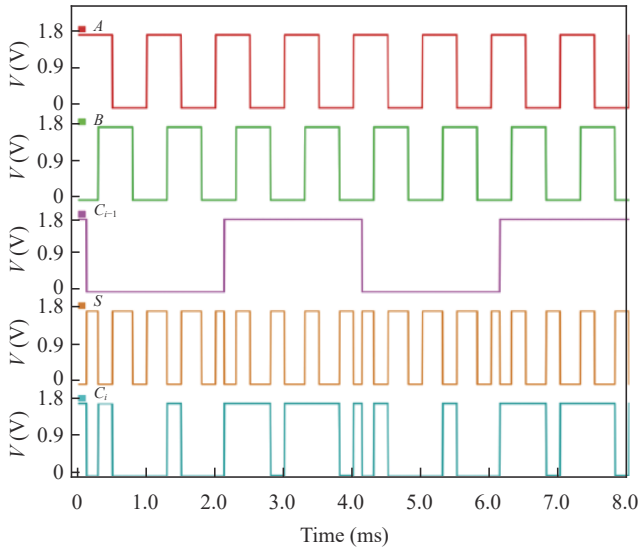

Figure 12 The simulation waveform of full adder 2.

Moreover, we compared the performances of the full adder 1 and full adder 2 proposed in this work and the other full adder in CMOS processes, as shown in Table 4. The full adder 2 uses fewer devices and has lower delay than the full adder 1, whereas the full adder 1 consumes less power than the full adder 2. Because the amount of the memristor is much smaller than the traditional MOSFET transistor, two full adders proposed in this work have obvious advantages in terms of power consumption and delay compared with CMOS-based full adder [39]. Besides, the lower delay could be due to the lower boundary mobility between the doped and undoped regions of the memristor, which is much smaller than the mobility of electron and hole in the MOS tube [40]. Compared to the MRL-based 1-bit full adder [35], although our devices utilize more memristor cells, the power consumptions of the full adder 1 and the full adder 2 are both tremendously reduced, and the delay is reduced by 23% for the full adder 1 and 30.4% for the full adder 2 respectively.

Table 4 Comparison of full adder parameters

Parameter	CMOS-based 1-bit full adder [39]	MRL-based 1-bit full adder [35]	Full adder 1	Full adder 2
Number of devices	28	22	28	26
Power consumption (mW)	37.18	6.2	0.134	0.122
Delay (ps)	224	90	69.3	62.6

VI. Conclusion

In conclusion, we leverage the computational principles of MRL to harness the unique advantages offered by memristors as fundamental computational logic elements, and thus three basic logic gates XNOR1, XNOR2 and XOR are firstly designed. Subsequently, some combinatorial logic circuits, such as 1-bit numerical comparators, 2-bit numerical comparators and full adder 1, are then constructed based on XNOR1, XNOR2 and XOR gates. Additionally, we proposed and designed a universal logic circuit that can realize four different kinds of logic functions (AND, OR, XOR, XNOR) at the same time. Moreover, a full adder 2 has been built using XOR function of the universal logic circuit. The logic functions of all the circuits designed above were further verified using Cadence simulation software. Compared with the traditional CMOS counterparts, the logic circuits designed in this paper utilize fewer devices, and exhibit lower power consumption and lower delay, making them promising candidates for high-performance artificial intelligence computing system, particularly in the realm of associative memory. These systems offer significant potential for improving tasks related to pattern recognition, information retrieval, and cognitive computing.

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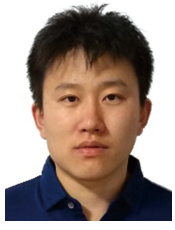
Xiaojuan LIAN received the B.S. degree in electronic science and technology and the M.S. degree in physical electronics from Xidian University, Xi'an, China, in 2008 and 2011 respectively. She received the Ph.D. degree in electrical engineering from the Universitat Autònoma de Barcelona, Spain, in 2014. She is currently an Associate Professor at the College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing, China. Her research interests include memristive devices (RRAM, PCRAM and so on), information storage technology, and neuromorphic computing applications.
(Email: xjlian@njupt.edu.cn)

Chuanyang SUN received the B.E. degree in electronic information engineering from the Bengbu College, Bengbu, China, in 2021. He currently pursuing for the M.S. degree with Nanjing University of Posts and Telecommunications, Nanjing, China, engaged in the research of memory-computing integration based on memristor.

Zeheng TAO received the B.E. degree in electronic science and technology from Hunan University of Technology, Zhuzhou, China, in 2021. He is currently working towards the M.S. degree at Nanjing University of Posts and Telecommunications, Nanjing, China, focusing on research related to the integration of memory and computing using memristors.



Xiang WAN received the B.S. degree in applied physics and the M.S. degree in materials engineering from University of Science and Technology of China, Chengdu, China, in 2011 and 2014 respectively. He received the Ph.D. degree in electronic science and technology from Nanjing University, Nanjing, China, in 2017. From 2019 to 2021, he held the Postdoc Position at the National Institute for Materials Science. He is currently a Lecturer at the College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing, China. His current research interests are the design, fabrication and modeling of electronic devices and systems for neuromorphic computation.

Xiaoyan LIU received the Ph.D. degree in microelectronics and solid-sate electronics from Fudan University, Shanghai, China, in 2019. She is currently an Associate Professor with Nanjing University of Posts and Telecommunications, Nanjing, China, working on the researches mainly including the micro-LED array devices for visible light communication in free-space and underwater, memeristive devices for neuromorphic computing and artificial synapse.

Zhikuang CAI received the B.S. degree in information engineering from Nanjing University of Posts and Telecommunications, Nanjing, China, in 2005, and the Ph.D. degree from ASIC System Center at Southeast University, Nanjing, China, in 2014. He is currently a Professor at the College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing, China. His research interests include low power SoC design and test, and chiplet package and test.

Lei WANG received the B.S. degree in electrical engineering from Beijing University of Science and Technology, Beijing, China, in 2003, the M.S. degree in electronic instrumentation systems from University of Manchester, Manchester, UK, in 2004, and the Ph.D. degree in 2009 at University of Exeter, Exeter, UK. Between 2008 and 2011, he was employed as a Postdoctoral Research Fellow with University of Exeter, Exeter, UK, to work on a fellowship funded by European Commission. In 2020, he joined Nanjing University of Posts and Telecommunications, Nanjing, China, as a Full Professor. His research interests include phase-change memories, neural networks, and other phase-change based optoelectronic devices and their potential applications.
(Email: leiwang1980@njupt.edu.cn)