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RESEARCH ARTICLE

An Ultra-wideband Doubler Chain with 43–65 dBc Fundamental Rejection in Ku/K/Ka Band

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Abstract — In this paper, a double-balanced doubler chain with >43-dBc fundamental rejection over an ultra-wide bandwidth in 0.13-μm SiGe BiCMOS technology is proposed. To achieve high fundamental rejection, high output power, and high conversion gain over an ultra-wideband, a double-balanced doubler chain with pre- and post-drivers employs a bandwidth broadening technique and a ground shielding strategy. Analysis and comparison of the single-balanced and double-balanced doublers were conducted, with a focus on their fundamental rejection and circuit imbalance. Three doublers, including a passive single-balanced doubler, an active single-balanced doubler, and a passive double-balanced doubler were designed to verify the performance and characteristics of the single- and double-balanced doublers. Measurements show that the proposed double-balanced doubler chain has approximately 15 dB better fundamental rejection, and more than twice the relative bandwidth compared to the single-balanced doubler chain fabricated with the same process. Over an 86.9% 3-dB bandwidth from 13.4 GHz to 34 GHz, the double-balanced doubler chain delivers 14.7-dBm peak output power and has >43-/33-dBc fundamental/third-harmonic rejection. To the authors' best knowledge, the proposed double-balanced doubler chain shows the highest fundamental rejection over an ultra-wideband among silicon-based doublers at millimeter-wave frequency bands.

Keywords — Bandwidth, Doubler, Double-balanced, Fundamental rejection, Single-balanced.
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I. Introduction

Millimeter-wave (mmWave) with abundant spectrum resources have been released, such as the n257 band from 26.50 GHz to 29.50 GHz, n258 band from 24.25 GHz to 27.50 GHz, and n260 band from 37.00 GHz to 40.00 GHz, which are expected to meet the high speed, high capacity, and low latency expectations. The frequency bands used vary from country to country and region to region, thus broadband performance is necessary to improve the adaptability of communication systems [1]–[10].

Doubler is a key device in mmWave systems, which can effectively circumvent the problem of poor phase noise performance of local oscillators (LOs) in mmWave bands [11], [12]. Compared to single-ended, distributed and Gilbert doublers, balanced architectures are preferred due to their power combining and inherent odd harmonic rejection ability [13], [14]. The single-balanced doubler can achieve excellent fundamental rejection if the circuit is perfectly balanced. Many efforts have been reported in achieving effective fundamental rejection [13]–[19]. However, this architecture is sensitive to amplitude and phase errors. The imbalance from the input balun and layout asymmetry will cause the fundamental rejection to deteriorate rapidly, making it generally impossible to operate over a wide frequency band. The distributed architecture reported in [20] achieves an ultra-wide bandwidth at the cost of chip size and has mediocre fundamental rejection. The Kimura active doubler reported in [21] demonstrates an ultra-wide 3-dB bandwidth, while the fundamental rejection drops to 25 dBc over the wide frequency band. Several studies on the double-balanced doubler have been reported [22], [23].

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The double-balanced doubler reported in [22] exhibits both excellent fundamental rejection and bandwidth simulation results. Whereas the measured 3-dB bandwidth was compressed. Therefore, this architecture urgently needs further experimental validation.

Active doublers are popular because of the higher conversion gain [21], [24]–[27]. However, it is difficult to provide enough gain to significantly reduce the power requirement of the LO. Typically, a driver is still required for the input of the doubler. Also, there is a certain optimal range of output power for doublers due to the transistor characteristics. When higher power is required in the system, additional drivers are needed at the output port of the active doubler. Implementing a double-balanced architecture in an active doubler is particularly challenging due to the limitations of DC path, which can easily cause circuit imbalance. These factors make active doublers very constrained in practice. Compare with active doublers, passive doublers cascade pre- and post-drivers offer the advantages of system-definable gain, input and output power, and flexibility in circuit architecture. Various works on doublers have been reported, each achieving excellent performance in different aspects [9]–[26], while few of the reported silicon-based mmWave doublers have achieved high fundamental rejection, high gain, and high output power simultaneously over an ultra-wide bandwidth.

This paper presents a double-balanced doubler chain that demonstrates high fundamental rejection, high output power, and high conversion gain over an ultra-wideband. The double-balanced doubler architecture is compared to single-balanced counterparts, including a passive single-balanced doubler, an active single-balanced doubler, and a passive double-balanced doubler, all fabricated in 0.13-μm SiGe BiCMOS technology. Through systematic analysis and comparison, it was found that the double-balanced doubler has superior performance in terms of fundamental rejection and operating bandwidth. The proposed double-balanced doubler chain was fabricated in 0.13-μm SiGe BiCMOS technology and compared to [28]. The use of pre- and post-drivers in both doubler chains helps to reduce the power demand on the LO while providing high output power. The double-balanced doubler chain achieves approximately 15-dB better fundamental rejection and over more than twice the relative bandwidth compared to the single-balanced doubler chain, thanks to the advantages of the double-balanced architecture, bandwidth broadening technique, and ground shielding strategy.

The remainder of this paper is organized as follows: Section II analyzes the effect of circuit imbalance on single- and double-balanced doublers and compares them. In Section III, an experimental comparison of the single- and double-balanced doublers was performed. Section IV introduces two doubler chains based on the single- and double-balanced architectures while comparing these works with state-of-the-art doublers in the mmWave band. Finally, a summary is given in Section V.

II. Analysis of Single- & Double-Balanced Doublers

In this section, the relationship between the fundamental rejection capability and the imbalance components of single-balanced and double-balanced structures is analyzed and compared. Section II.1 introduces the concept of amplitude and phase error components for a single-balanced doubler. Section II.2 distinguishes the input and output imbalance components of a double-balanced doubler based on their different characteristics, and introduces a frequency factor to characterize the imbalance at the fundamental and second harmonic. The difference in the fundamental rejection capability of single-balanced and double-balanced architectures with respect to the imbalance component is also given, as well as the difference in the input impedance characteristics of the two structures.

1. Single-balanced doubler

Figure 1 illustrates the architecture of the single-balanced doubler. The amplitude-normalized voltages at the input ports are expressed as

$$\begin{cases} v_1 = \cos\omega t \\ v_2 = \cos(\omega t - \pi) = -\cos\omega t \end{cases} \tag{1}$$

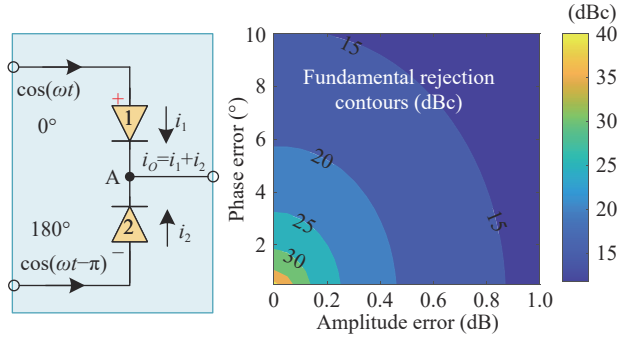

Figure 1 Architecture and fundamental rejection versus amplitude and phase errors of the single-balanced doubler.

Bring (1) into Taylor expansion, and one gets

$$\begin{cases} i_1 = A_0 + A_1\cos\omega t + A_2(\cos\omega t)^2 + A_3(\cos\omega t)^3 + \cdots \\ i_2 = A_0 - A_1\cos\omega t + A_2(\cos\omega t)^2 - A_3(\cos\omega t)^3 + \cdots \end{cases} \tag{2}$$

At point A in Figure 1,

$$i_O = i_1 + i_2 = 2A_0 + 2A_2(\cos\omega t)^2 + 2A_4(\cos\omega t)^4 + \cdots \tag{3}$$

where odd harmonics cancel each other out. If the input signals are not balanced, then a fraction of the odd harmonics remain. To quantify this effect, we lump the imbalances of input balun as an amplitude error, ε, and a phase error, θ. In the in-phase path, i.e., the input wave-

form is expressed as $(1+\varepsilon)\cos(\omega t+\theta)$ and the other as $-\cos(\omega t)$. Equation (2) can be rewritten as:

$$\begin{cases} i_1 = 1+(1+\varepsilon)\cos(\omega t+\theta)+\big((1+\varepsilon)\cos(\omega t+\theta)\big)^2 \\ \qquad +\big((1+\varepsilon)\cos(\omega t+\theta)\big)^3+\cdots \\ i_2 = 1-\cos\omega t+(\cos\omega t)^2-(\cos\omega t)^3+\cdots \end{cases} \tag{4}$$

where the normalized amplitude of each order component is assumed for simplicity. Noting that the average power of $a\cos(\omega t+\theta)+b\cos(\omega t)$ is given by $(a^2+2ab\cos\theta+b^2)/2$, and the second-harmonic average power in $(a\cos(\omega t+\theta))^2+(b\cos(\omega t)^2)$ is given by $(a^4+b^4+2a^2b^2\cos(2\theta))/8$, the fundamental rejection (FR) is expressed as

$$\mathrm{FR_S}=\frac{1}{4}\frac{(1+\varepsilon)^4+1+2(1+\varepsilon)^2\cos 2\theta}{(1+\varepsilon)^2-2(1+\varepsilon)\cos\theta+1} \tag{5}$$

According to (5), the relationship between $\mathrm{FR_s}$ and amplitude/phase error is depicted in Figure 1. With 0.5-dB amplitude error or 6° phase error, the fundamental rejection drops rapidly below 20 dBc. At point (1 dB, 10°), the rejection is less than 12 dBc. This shows that the single-balanced doubler is highly sensitive to phase and amplitude errors, requiring a perfectly balanced balun. The bandwidth of the balun will strictly limit the operating bandwidth of the circuit.

2. Double-balanced doubler

To enhance the fundamental rejection and extend operating bandwidth, the double-balanced doubler shown in Figure 2 was proposed. Similar to Section II.1, when we lump the input amplitude error, ε, and phase error, θ, into the in-phase path. The i_1, i_2, i_3, and i_4 in Figure 2 can be expressed as

$$\begin{cases} i_1 = -(1+\varepsilon)\cos(\omega t+\theta)+\dfrac{(1+\varepsilon)^2}{2}\cos(2\omega t+2\theta)-\cdots \\ i_2 = (1+\varepsilon)\cos(\omega t+\theta)+\dfrac{(1+\varepsilon)^2}{2}\cos(2\omega t+2\theta)+\cdots \\ i_3 = -\cos(\omega t)+(\cos 2\omega t)/2\ -\cdots \\ i_4 = \cos\omega t+(\cos 2\omega t)/2\ +\cdots \end{cases} \tag{6}$$

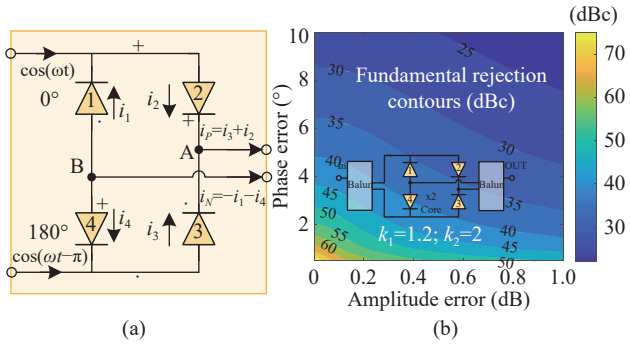

Figure 2 (a) Architecture and (b) Fundamental rejection versus amplitude and phase errors of the double-balanced doubler.

where DC and higher contents are hidden in the omitted parts to simplify the formulas. Note from (6) that if the output balun is perfectly balanced, this architecture can still achieve perfect fundamental rejection despite the imbalances from the input. Different from the input balun, the imbalances from the output balun won't go through the non-linear transfer function. To simplify the analysis, we lump the imbalances into the i_P path, and lump the output imbalances at the second harmonic frequency as ε and θ. The imbalances at the fundamental frequency are lumped as $k_1\varepsilon$ and $k_2\theta$, where k_1 and k_2 are used to characterize the frequency characteristics of the output balun. Thereby, equation (6) can be rewritten as

$$\begin{cases} i_1 = -(1+\varepsilon)\cos(\omega t+\theta) \\ \qquad +(1+\varepsilon)^2\cos(2\omega t+2\theta)/2\ -\cdots \\ i_2 = (1+k_1\varepsilon+\varepsilon)\cos(\omega t+\theta+k_2\theta) \\ \qquad +(1+4\varepsilon+\varepsilon^2)\cos(2\omega t+3\theta)/2\ +\cdots \\ i_3 = -(1+k_1\varepsilon)\cos(\omega t+k_2\theta) \\ \qquad +(1+\varepsilon)\cos(2\omega t+\theta)/2\ -\cdots \\ i_4 = \cos\omega t+(\cos 2\omega t)/2\ +\cdots \end{cases} \tag{7}$$

Note that the average power of $a\cos(\omega t+i\theta)+b\cos(\omega t+j\theta)+c\cos(\omega t+k\theta)+d\cos(\omega t)$ is given by $(a^2+b^2+c^2+d^2+2ab\cos(i-j)\theta+2ac\cos(i-k)\theta+2ad\cos(i\theta)+2bc\cos(j-k)\theta+2bd\cos(j\theta)+2cd\cos(k\theta))/2$. Thereby, the fundamental rejection of the double-balanced doubler ($\mathrm{FR_D}$) is expressed as (8).

$$\mathrm{FR_D}=\frac{\begin{pmatrix}(1+\varepsilon)^4+(1+\varepsilon^2+4\varepsilon)^2+(1+\varepsilon)^2+1+2[(1+\varepsilon)^2(1+\varepsilon^2+4\varepsilon)\cos\theta+(1+\varepsilon)^3\cos\theta \\ +(1+\varepsilon)^2\cos 2\theta+(1+\varepsilon^2+4\varepsilon)(1+\varepsilon)\cos 2\theta+(1+\varepsilon^2+4\varepsilon)\cos 3\theta+(1+\varepsilon)\cos\theta]\end{pmatrix}}{\begin{pmatrix}2[((1+\varepsilon)^2+(1+k_1\varepsilon+\varepsilon)^2+(1+k_1\varepsilon)^2+1]+4[-(1+\varepsilon)(1+k_1\varepsilon+\varepsilon)\cos k_2\theta+(1+\varepsilon)(1+k_1\varepsilon)\cos(1-k_2)\theta \\ -(1+\varepsilon)\cos\theta-(1+k_1\varepsilon+\varepsilon)(1+k_1\varepsilon)\cos\theta+(1+k_1\varepsilon+\varepsilon)\cos(k_2+1)\theta-(1+k_1\varepsilon)\cos k_2\theta])\end{pmatrix}} \tag{8}$$

When frequency factors k_1 and k_2 are set to 1.2 and 2, respectively, the fundamental rejection can be depicted as Figure 1(b). At (1 dB, 10°), the fundamental rejection is up to 22 dBc. Considering the performance of balun, the reasonable value of k_1=1.2 and k_2=2 implies that the amplitude error at the fundamental frequency point is 0.79 dB worse compared to the second harmonic point, while the phase error is 1.6 times worse. Assuming that the amplitude/phase error at the second harmonic point is 0.2 dB/1°, the amplitude/phase error at the fundamental frequency point would be 0.99 dB/1.6°. The difference between Figure 1 and Figure 2 shows that the double-balanced architecture has a more prominent advantage as the circuit balance conditions improve. Even when the balance conditions are poor (1 dB, 10°), the double-balanced doubler still outperforms the single-

balanced doubler by more than 10 dB. This demonstrates the robust fundamental rejection of the double-balanced doubler over a wide frequency band where balance conditions may fluctuate.

To further study the impedance characteristics of these two architectures, the equivalent models of the single- and double-balanced architectures are depicted in Figure 3. In the single-balanced doubler, one diode is forward-biased and the other is reverse-biased, and only one diode is on at the same time, resulting a high input impedance for the single-balanced architecture. The model of an on-state diode can be equated to a resistor and capacitor in parallel. The off-state diode can be simplified to a capacitor C_{off} [29]. As shown in Figure 3(a), the input impedance can be expressed as

$$Z_{\text{in\_S}} = \frac{R_{\text{on}}}{1+(\omega C_{\text{on}} R_{\text{on}})^2}(1-\text{j}\omega C_{\text{on}} R_{\text{on}}) + \frac{Z_L}{1+(\omega C_{\text{off}} Z_L)^2}(1-\text{j}\omega C_{\text{off}} Z_L) \quad (9)$$

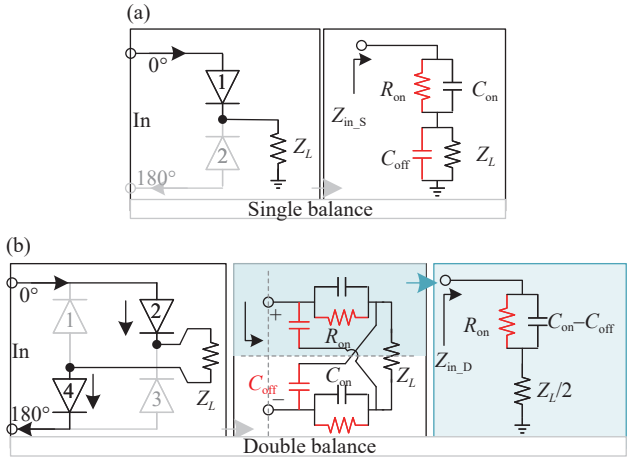

Figure 3 Equivalent model of the (a) Single-balanced and (b) Double-balanced architecture.

For a double-balanced doubler, a pair of on-state diodes provides a path for the signal over the full period, resulting in a lower input impedance than the single-balanced architecture. Moreover, as visualized in Figure 3(b), off-state diodes (1 and 3) operate as neutralizing capacitors, limiting the parasitical capacitance of on-state diodes (2 and 4). The input impedance can be expressed as follows:

$$Z_{\text{in\_D}} = \left\{\frac{R_{\text{on}}}{1+[\omega(C_{\text{on}}-C_{\text{off}})R_{\text{on}}]^2}\right\} \times [1-\text{j}\omega(C_{\text{on}}-C_{\text{off}})R_{\text{on}}] + \frac{Z_L}{2} \quad (10)$$

Comparing the first item of (9) and (10), as well as the second item of (9) and (10), it is noticeable that the double-balanced architecture exhibits a lower input Q value, leading to a naturally broader impedance matching range [30].

III. Design of Single- & Double-Balanced Doublers

For the proof of concept, three test chips were designed: a passive single-balanced doubler, an active single-balanced, and a passive double-balanced doubler. A comparison of the three doublers is performed at the end of this section.

1. Single-balanced passive doubler

Figure 4 illustrates the architecture of the passive single-balanced doubler. A pair of differential signals are fed into the doubler core from the inputs. Due to the nonlinear characteristics of the transistors, the doubler core will generate various harmonics. Among them, even harmonics are in phase and added at the combining point A, and odd harmonics are differentially canceled at point A. The collector and base of the triode are shorted together to act as a diode in this design. A layout view of the passive doubler core is shown in Figure 4. The differential transistors are arranged symmetrically to ensure the balance of the circuit.

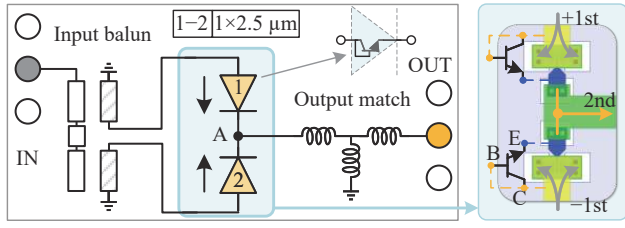

Figure 4 Schematic of the passive single-balanced doubler, and layout of the doubler core.

To fully excavate the performance of the transistor, the output power and impedance characteristics of the transistor were evaluated for different sizes, as shown in Figure 5. According to the simulation result, transistors with larger size yield higher second-harmonic power within a range of 10 μm. Whereas, the output power of the doubler also depends on a good output matching network before it can be delivered to subsequent circuits. The right part in Figure 5 depicts the output impedance versus transistor size. The circuit has a match-friendly output impedance when the transistor length is between 2 μm and 3 μm. In this design, a length of 2.5 μm was selected. Although the corresponding output power is about 1 dB lower than the optimal value, this can easily be compensated by a post-amplifier.

Figure 6 shows a micrograph of the passive single-balanced doubler with a compact core size of 0.15 mm^2. The performance of the doubler was measured by a signal generator Agilent E8267D, a power meter E4416A and a signal analyzer R&S FSW85. As shown in Figure 7, the passive single-balanced doubler shows a relative operating bandwidth of 38.8% from 27 GHz to 40 GHz. With 13-dBm input power, the fundamental/third-harmonic rejection is 8–32/24–37 dBc.

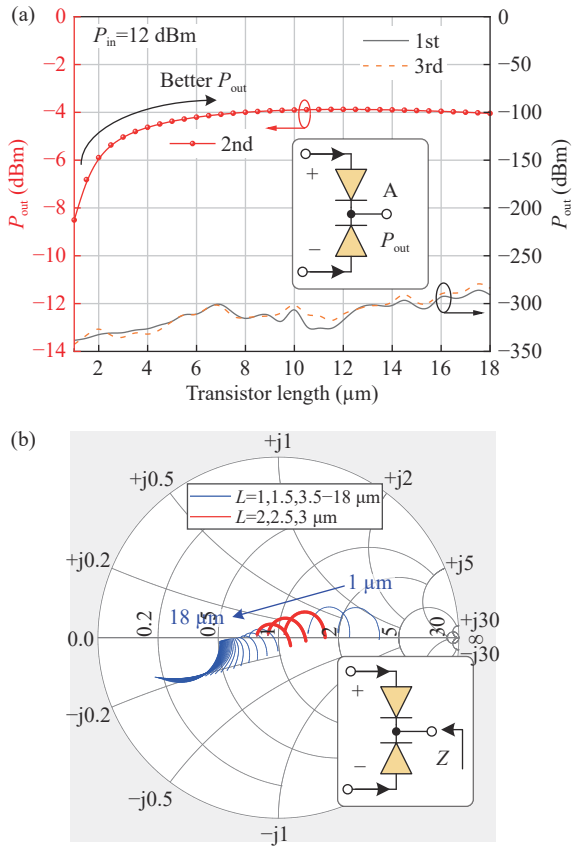

Figure 5 Characteristics of the transistor. (a) Output power vs. transistor length; (b) Ouput impendance vs. transistor length.

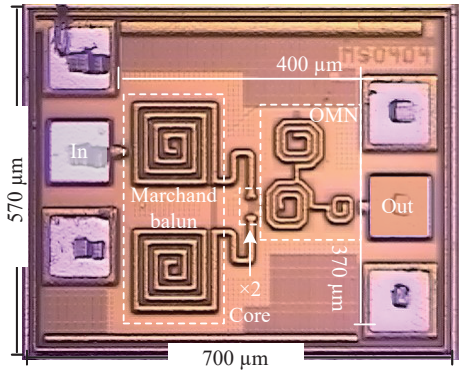

Figure 6 Micrograph of the passive single-balanced doubler.

2. Single-balanced active doubler

Benefiting from the stacked structure, cascode (CC) amplifiers offer higher gain compared to comparably sized common-emitter amplifiers [31]. In this design, the CC structure is employed to achieve positive conversion gain in the active frequency doubler. Figure 8(a) shows the harmonic content of the CC core. Note a sweet region between 0.5 V and 0.65 V, where the second harmonic power peaks and the third harmonic power falls into a valley. The chosen 0.6-V V_b is biased through a current mirror. In addition, transistors with 16-μm length were selected to balance harmonic performance and power consumption. The schematic diagram is shown in Figure 8(b), where all necessary power supplies

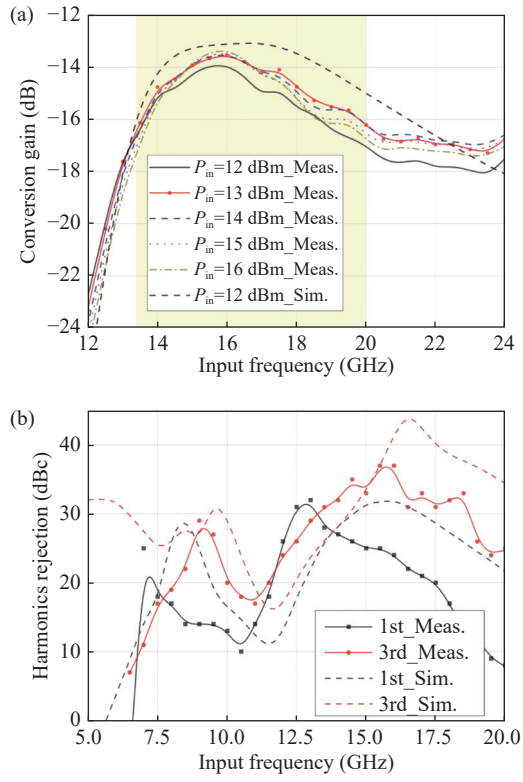

Figure 7 (a) Conversion gain and (b) Harmonic rejection of the single-balanced doubler (Meas.=Measure, Sim.=Simulated).

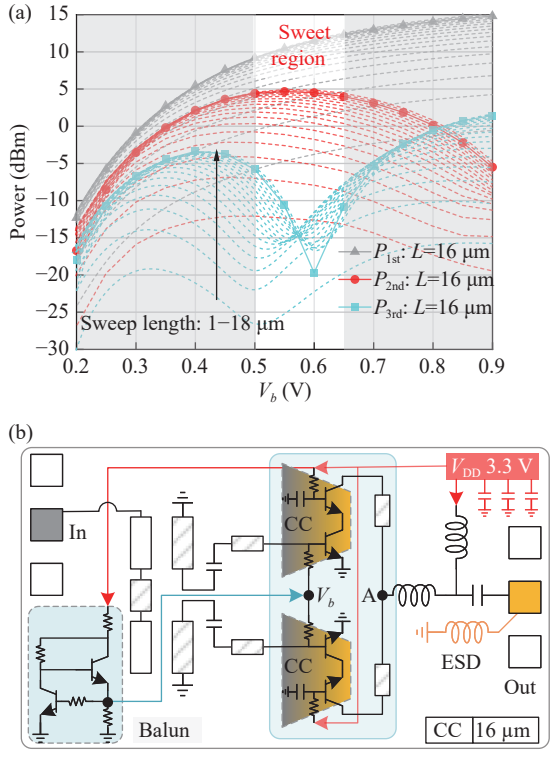

Figure 8 (a) Harmonic contents power versus bias voltage (V_b) and transistor length of the CC structure; (b) Schematic of the active single-balanced doubler.

are derived from a single 3.3-V source. Bulky bypass capacitors are deployed in the DC supply network to ensure RF grounding. A ground inductor is introduced at

the output to provide electro-static discharge (ESD) functionality.

In Figure 5, the single-balanced architecture demonstrates ideal odd-harmonic rejection, however, in actual implementation, circuit imbalance can significantly diminish this performance. To enhance the balance performance, a Marchand balun with a compensation line was proposed in [32]. If the Y-parameter and the electrical length θ_c of the compensation line satisfy the equation

$$Y_c \tan\frac{\theta_c}{2} = \frac{Y_e Y_o(\cot\theta_e \csc\theta_o - \cot\theta_o \csc\theta_e)}{Y_o \csc\theta_o - Y_e \csc\theta_e} \quad (11)$$

The Marchand balun will achieve a perfect balance. On the right-hand side of (11), Y_e and Y_o are the even- and odd-mode characteristic admittance of the coupled lines. θ_e and θ_o are the even- and odd-mode electrical lengths of the coupled lines. In this design, a compensation line with 50-Ω characteristic impedance and 2° electrical lengths was selected. Figure 9 shows the performance of the Marchand balun with and without a compensation line. Notice that the compensation line allows the balun to achieve perfect balance, which ensures the odd-harmonic rejection of the circuit.

A micrograph of the test chip is shown in Figure 10 (a). The active single-balanced doubler has a compact core size of 0.18 mm^2. As shown in Figures 10(b)–(d), the active single-balanced doubler achieves a measured relative operating bandwidth of 40.6% from 26.5 GHz to 40 GHz. The measured fundamental/third-harmonic rejection is 24–45/23–43 dBc at 6-dBm input power, and the peak PAE is 17%.

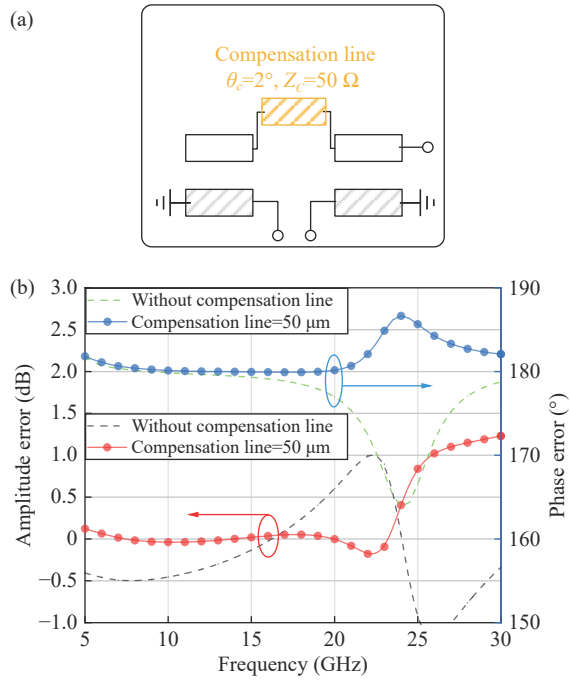

Figure 9 (a) Schematic of the Marchand balun with compensation line; (b) Performance of the Marchand balun with and without compensation line.

3. Double-balanced passive doubler

Figure 11 depicts a schematic of the passive double-balanced doubler. Unlike single-balanced doublers, the double-balanced doubler core consists of four transistors,

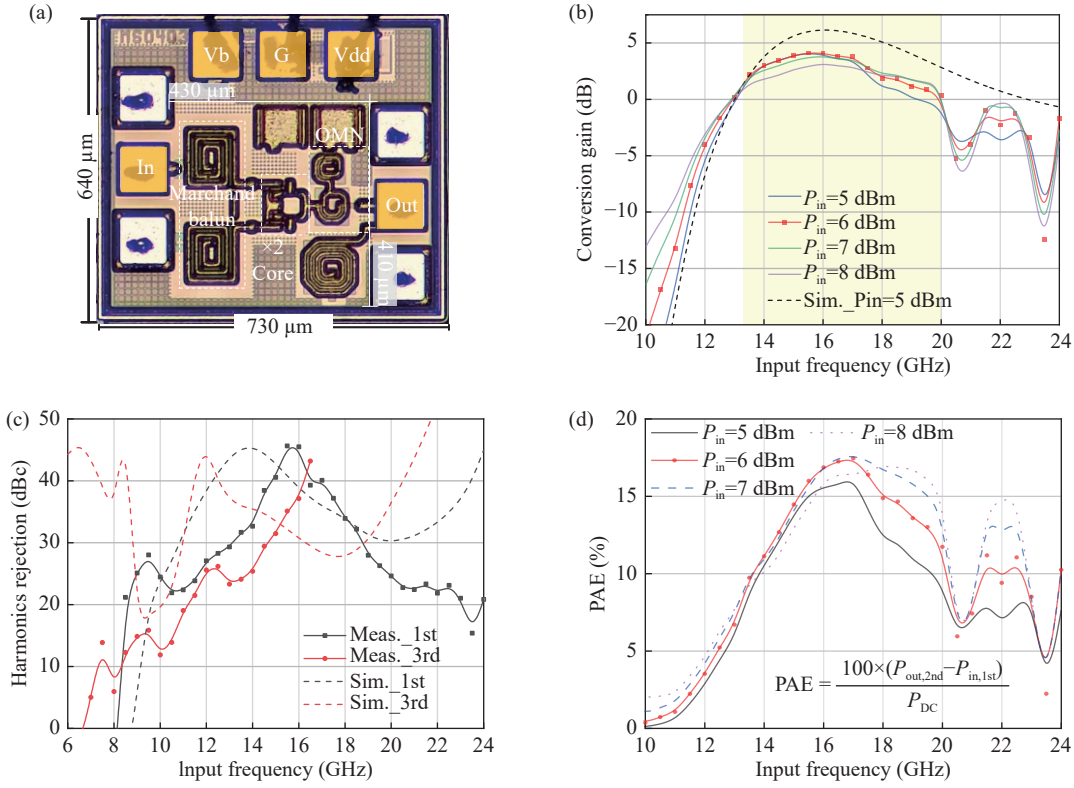

Figure 10 (a) Micrograph of the active single-balanced doubler. (b) Conversion gain, (c) Harmonic rejection, and (d) Measured power added efficiency of the active single-balanced doubler.

and the output is converted from the differential to single-ended by a balun. Each of these four transistors contains a pair of input and output ports, resulting in eight RF alignments around the compact ring core. Irregular alignments will introduce imbalance and unwanted signal coupling, thus deteriorating the fundamental rejection of the circuit.

Figure 12(a) shows a symmetrical layout without ground shielding. Both input and output differential signals have perfectly symmetrical paths, thus ensuring the balance of the circuit. However, this layout has a strong input-output coupling, which can significantly degrade fundamental rejection performance. To address this issue, a ground shielding technique is introduced (Figure 12(a), lower left), where the input and output paths are deployed on the upper and lower sides of the ground plane to cut off the signal coupling. With the help of ground-shielding technique, the coupling is reduced by about 20 dB. The proposed layout for the doubler core is shown in Figure 12(b). The metal layer MQ serves as the ground, with four transistors arranged symmetrically below it. Additionally, the doubler core is surrounded by ground shielding walls. In this symmetrical layout, the differential mode signals experience a mutual enhancement of the magnetic coupling, while the common-mode signals experience a mutual weakening of the magnetic coupling.

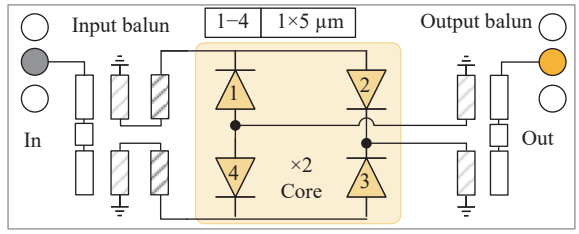

Figure 11 Schematic of the double-balanced doubler.

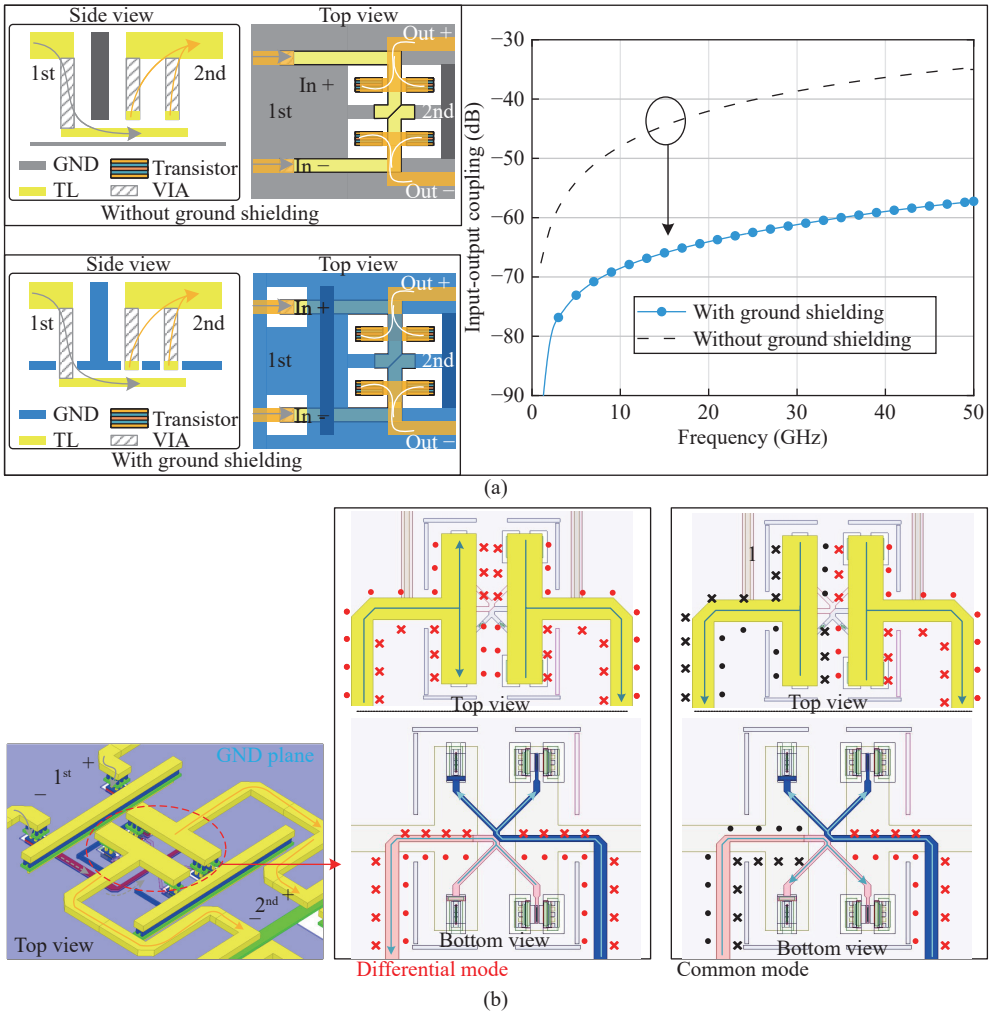

Figure 12 (a) Diagrams of the layout without and with ground shielding, and the corresponding coupling between input and output ports. (b) Layout of the ring core and the corresponding magnetic coupling in differential mode and common modes.

A micrograph of the double-balanced doubler is shown in Figure 13. The core size is 0.21 mm^2. According to the measured results in Figure 14, the relative operating bandwidth is 114.3% from 12 GHz to 44 GHz, which is more than doubled compared to both active and passive single-balanced doublers. If the odd-harmonic rejection is limited to greater than 29 dBc, the relative bandwidth is 95.7% from 12 GHz to 34 GHz. The funda-

mental/third-harmonic rejection is 29–46/36–57 dBc, which is about 15 dB better than the passive single-balanced doubler.

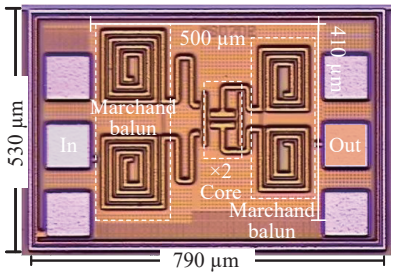

Figure 13 Micrograph of the passive double-balanced doubler.

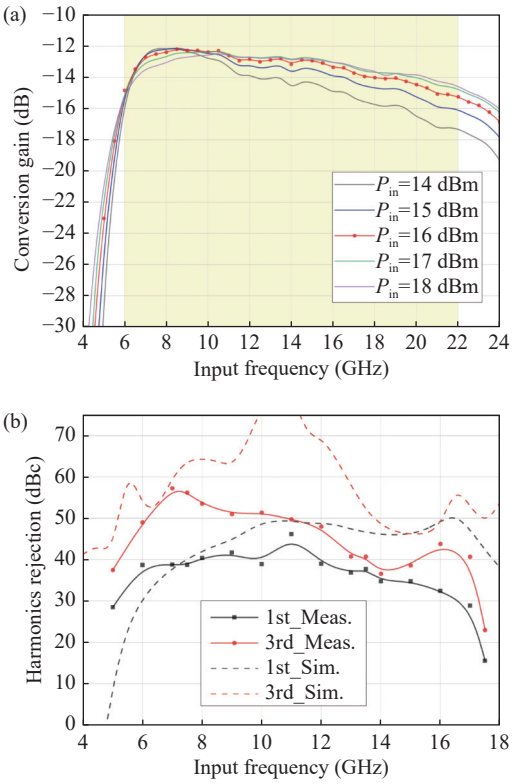

Figure 14 (a) Conversion gain of the double-balanced doubler. (b) Harmonic rejection of the double-balanced doubler.

Measurement results of these three doublers are listed in Table 1. Compared to single-balanced doublers, the double-balanced doubler offers significant advantages in both bandwidth and fundamental rejection, but requires high input driving power. The active balanced doubler shows the highest gain and good harmonic rejection but lacks advantages in operating bandwidth. Taking into consideration the discussions in Section I, passive doubler chains are found to be more practical in terms of performance and flexibility.

IV. Single- & Double-Balanced Doubler Chains

Based on the comparison work in Section III, the double-balanced doubler is anticipated to exhibit high fundamental rejection over a broad frequency range. This section presents a double-balanced doubler chain that boasts high fundamental rejection, high output power, and high gain over a wide frequency band. Furthermore, compared to the single-balanced doubler chain utilizing the same 0.13-μm SiGe BiCMOS technology, the double-balanced architecture has a significant advantage in terms of fundamental rejection and bandwidth.

Table 1 Performance comparison of the proposed three doublers

Technology	0.13-μm SiGe		
Architecture	Single balance		Double balance
Type	Active	Passive	Passive
3-dB BW (%)	40.6	38.8	114.3
f_{out} (GHz)	26.5–40	27–40	12–44
Peak conversion gain (CG) (dB)	4	–13	–12
1st rejection (dBc)	24–45	8–32	29–46*
3rd rejection (dBc)	23–43	24–37	36–57*
P_{DC} (mW)	140	0	0
Core size (mm^2)	0.176	0.148	0.205

Note: *Over 95.7% relative bandwidth from 12 GHz to 34 GHz.

1. Single-balanced doubler chain

Figure 15(a) depicts the schematic of the proposed single-balanced doubler chain. Pre- and post-drivers

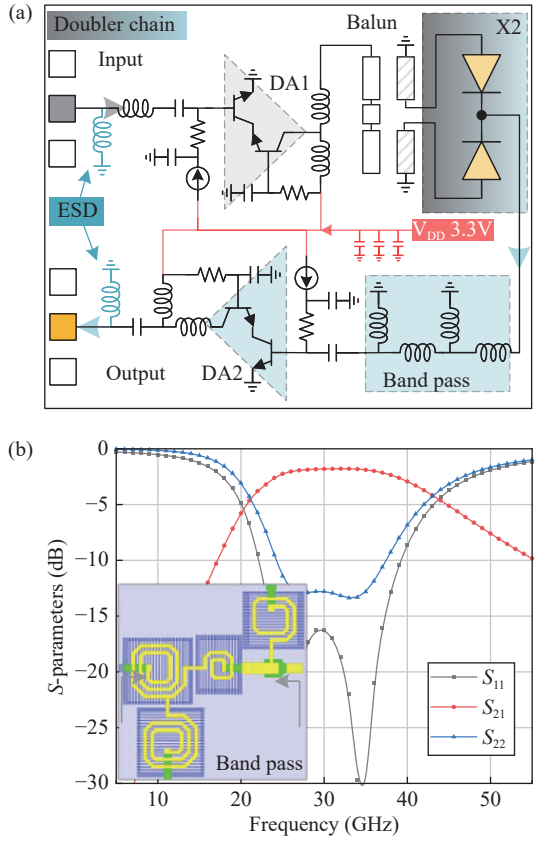

Figure 15 (a) Schematic of the single-balanced doubler chain. (b) Simulated S-parameters of the bandpass structure.

adopt the CC structure to provide sufficient gain. To provide 12-dBm input power to the doubler core, the transistor length of the pre-driver DA1 was chosen to be 12 μm. To provide output power over 10 dBm in the second-harmonic frequency band, the transistor length of the post-driver DA2 was chosen to be 2 × 8 μm. To suppress out-of-band harmonics, a bandpass matching network is introduced between the doubler core and DA2. As shown in Figure 15(b), the bandpass structure suppresses the fundamental content by about 10 dBc while providing better than −12-dB return loss for the interstage matching. Both input and output ports use grounded inductors for impedance matching to achieve ESD effects. Both drivers are biased by current mirrors. These two current mirrors share a 3.3-V DC with the supply voltage, which simplifies the bias circuit.

Figure 16(a) shows a micrograph of the single-balanced doubler chain with a core size of 0.4 mm^2. The performance of the chip was measured by a probe station. Figure 16(b) shows the measurement environment. In this case, the signal generator Agilent E8267D, signal analyzer N9030A, power meter E4416A, and Keysight E3648A were used. According to Figures 16(c)–(f), the proposed doubler chain shows a maximum power of 13 dBm, a gain of 11 dB, and a 3-dB bandwidth of 10 GHz from 26 to 36 GHz. The measured fundamental rejection is from 35 to 40 dBc and the third-harmonic rejection is from 28 to 41 dBc in the band of 28–36 GHz.

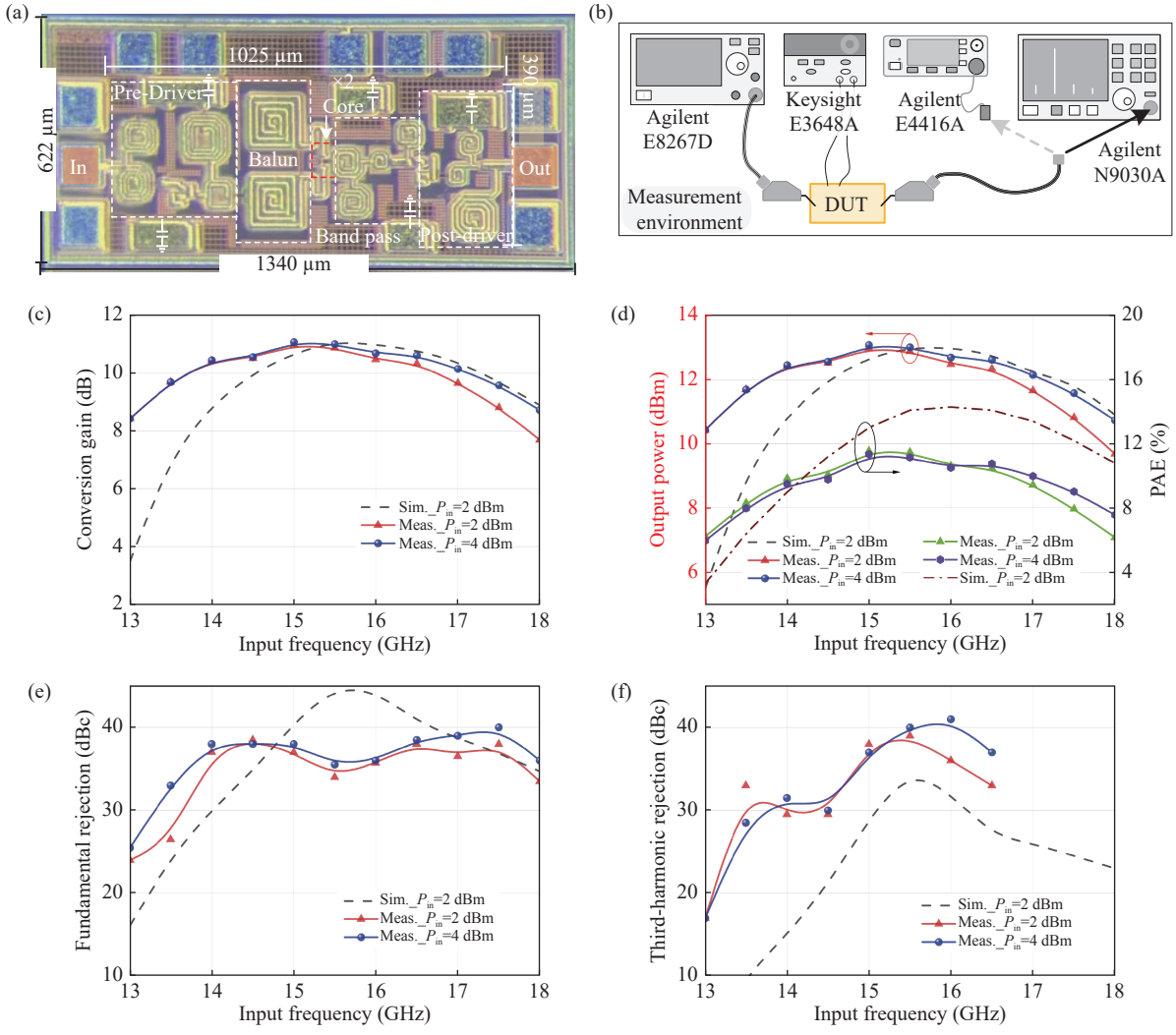

Figure 16 (a) Micrograph of the single-balanced doubler chain. (b) Measurement environment. (c) The measured conversion gain, (d) Output power and PAE, (e) Fundamental rejection, and (f) The third-harmonic rejection of the single-balanced doubler chain.

2. Double-balanced doubler chain

The double-balanced doubler offers significantly higher fundamental rejection and wider bandwidth compared to a single-balanced doubler. Therefore, the double-balanced doubler with pre- and post-drivers is currently the most effective solution for achieving high fundamental rejection, high output power, and high gain specifications over an ultra-wide bandwidth. The ultra-wide bandwidth of the double-balanced doubler, exceeding 100%, presents a challenge for the pre- and post-drivers. A promising solution has been introduced in the drivers to address this challenge.

Figure 17(a) illustrates the impedance of the post-driver core, where $Z_{11} = 10.8 - j40.4$, and $Z_{22} = 37.8 - j106.5$ at 26 GHz. Both impedances are far from the center of the Smith chart, which would severely limit the operating bandwidth. Typically, an emitter negative feedback inductor can be introduced to increase the real part of the input impedance, thus improving the input matching [33]. However, this scheme does not improve the output impedance. According to Figure 17(b), the RC feedback scheme can simultaneously improve the input and output impedance, and the max gain suppression effect at low frequencies is significantly greater than that at high frequencies, which will facilitate broadband amplifier design. In addition, the RC feedback scheme is more compact compared with the L_s scheme. Therefore, the RC feedback scheme is used for both the pre- and post-drivers in this design. As shown in Figure 17(c), the input return loss of this doubler chain is better than −10 dB (7–17.5 GHz input frequency band) and the output return loss is better than −8 dB (14–35 GHz output frequency band). A limitation of the doubler chain is the bulky chip size. In this design, the pre-driver uses a differential architecture for power combining, and the driver and doubler are matched directly by a differential network, thus simplifying the matching network. The co-design scheme saves approximately one balun, which is considerable at the low-frequency end. In addition, the center tap of the transformer simplifies the DC supply network for the driver. The overall gain of the doubler chain depends on the sum of the doubler core, pre- and post- drivers. After careful co-design, the doubler chain yields a simulated 3-dB output frequency band from 12 GHz to 34 GHz (see Figure 18(d)).

Figure 18(a) illustrates the schematic of the double-balanced doubler chain. To enhance out-of-band rejection, a bandpass filter is deployed between the doubler and the post-driver, rather than after the chain, thus avoiding deteriorating the output power of the post-driver. Figure 18(b) shows a micrograph of the double-balanced doubler chain. The layout is folded at the bandpass filter

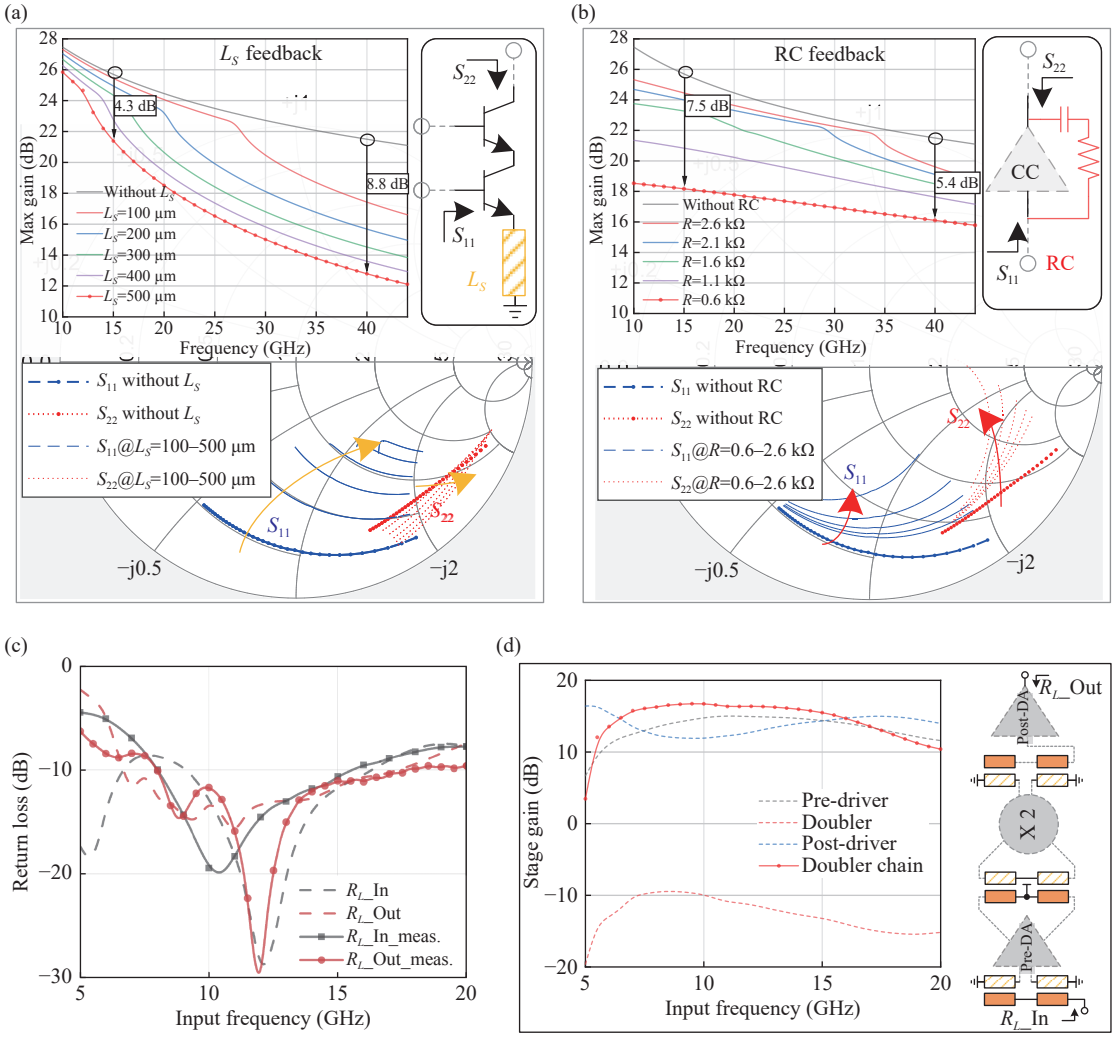

Figure 17 (a) Influence of emitter inductance on performance of CC structure. (b) Influence of RC feedback on CC structure performance. (c) Simulated (dashed line) and measured (solid line) return loss of the doubler chain. (d) Simulated stage gain of the doubler chain without bandpass filter.

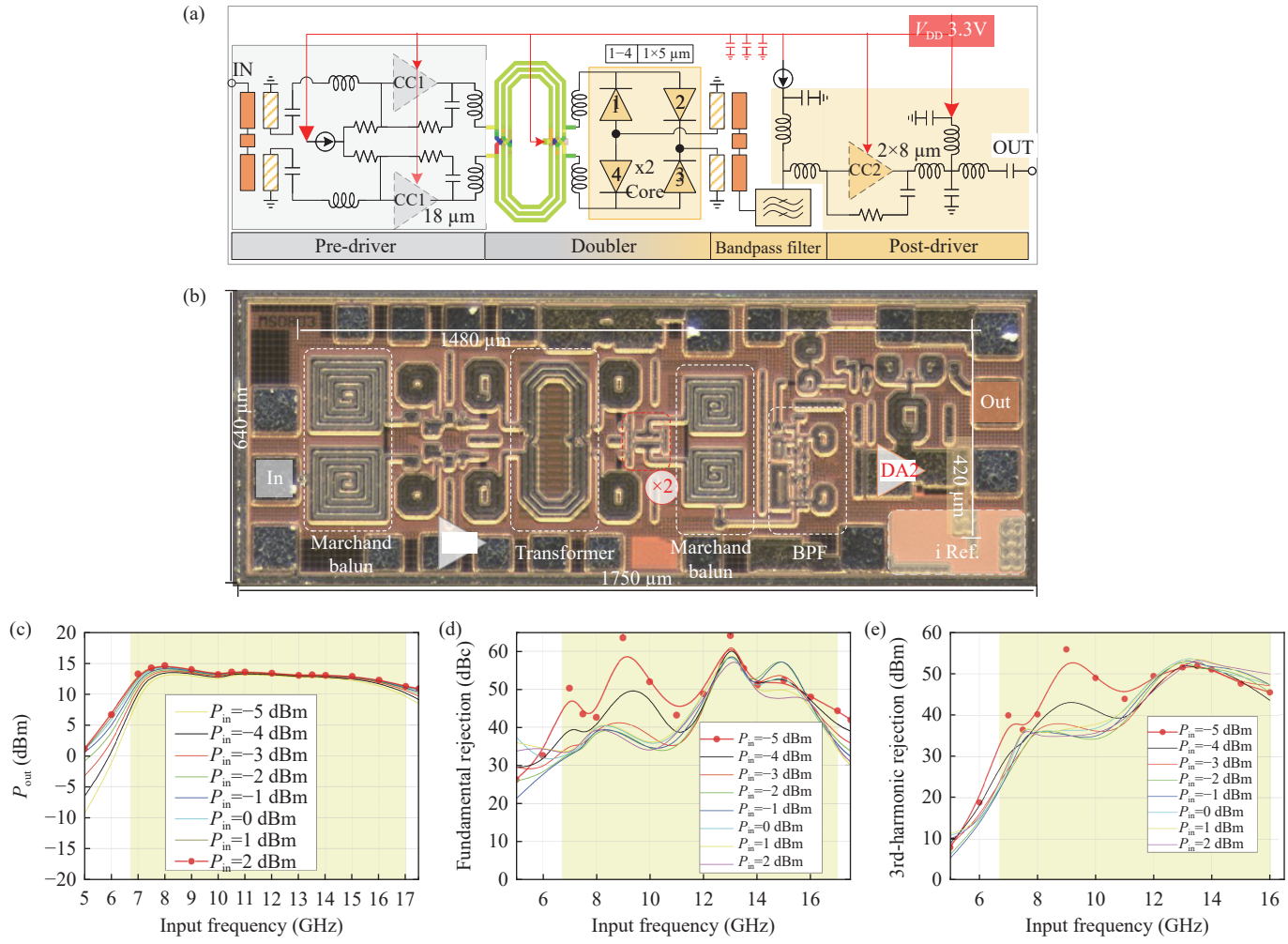

Figure 18 (a) Schematic. (b) Micrograph of the double-balanced doubler chain. (c) Measured output power, (d) Fundamental rejection, and (e) The third-harmonic rejection of the double-balanced doubler chain.

to achieve a more compact 0.62-mm^2 chip size. The chip has an integrated current reference source to ensure the accuracy of the bias circuit. Figure 18(c) depicts the measured power performance of the double-balanced doubler chain. The peak output power is 14.7 dBm at an input power of 2 dBm. The doubler chain shows a 3-dB bandwidth of 86.9% from 13.4 GHz to 34 GHz. The fundamental and third-harmonic rejections are shown in Figures 18(d)–(e). In the band of interest, the fundamental rejection is from 43 dBc to 64 dBc and the third harmonic rejection is from 33 dBc to 56 dBc for an input power of −5 dBm. Compared to the single-balanced doubler chain, the double-balanced doubler chain more than doubles the relative operating bandwidth and improves the fundamental rejection by about 15 dB.

Table 2 summarizes a comparison of the double-balanced doubler chain with previously reported mmWave silicon-based doublers. The double-balanced doubler chain proposed in this paper achieves the highest fundamental rejection and the highest output power over an ultra-wide frequency band. The area efficiency of the design is taken into account in the power density metric, which demonstrates that this design has good area efficiency. A figure of merit (FOM) is used for doublers, where $P_{\text{out,2nd}}$ is the second harmonic output power, $P_{\text{in,1st}}$ is the input fundamental power, FR is the fundamental rejection and BW is 3-dB fractional bandwidth [13], [20]. This double-balanced doubler chain shows a calculated FOM of 37.7/41.1, which is superior to that of other published works. To take the area efficiency into account, we modified the FOM to be FOM1, where S_{core} is the core size of the chip. The results show that the proposed double-balanced doubler chain maintains its superiority in terms of FOM1.

V. Conclusion

This work presents a double-balanced doubler chain that demonstrates high fundamental rejection, high output power, and high conversion gain over an ultra-wide frequency band. The concepts of amplitude and phase errors, as well as frequency factors, were introduced in the analysis and comparison of single-balanced and double-balanced doublers. The analysis and experimental results indicate that the double-balanced architecture exhibits superior performance in terms of fundamental rejection and operating bandwidth. A comparison of the single-

Table 2 Performance comparison with previously reported Si-based mmWave doublers

References	This work			[13]	[15]	[17]**	[20]	[21]	[22]	[32]
Technology	0.13-μm SiGe			0.13-μm SiGe	45-nm SOI	0.13-μm SiGe	0.35-μm SiGe	90-nm SiGe	0.18-μm CMOS	0.18-μm CMOS
Architecture	Double balance		Single balance	Single balance	Single balance	Single balance	Distributed single-balance	Kimura	Double balance	Single balance
	P_{in}=2 dBm	P_{in}=−5 dBm								
3-dB BW (%)	**86.9**	**78.5**	32.3	46.2	63.7	41.2	93.3*	133.3	48.3*	82.4
f_{out} (GHz)	**13.4–34**	**14.4–33**	26–36	25–40	46–89	27–41	4–11*	10–50	33–54*	15–36
1st Rej. (dBc)	**>33**	**>43**	>25	>35*	>38* (50–90 GHz)	>26	>23	>25*	>32	>33
3rd Rej. (dBc)	**>33**	**>25**	>17	N/A	42.2 (30 GHz)	N/A	N/A	N/A	N/A	N/A
Peak P_{out} (dBm)	**14.7**	**13.3**	13	13	7.4	4.3	−10	−4	3	−5.2
Peak CG (dB)	**13**	**18**	11	14	−4	20	−3	12	−11	−10
P_{DC} (mW)	**270**	**250**	150	87	20	22	60	250	0	11
Peak PAE† (%)	**10.3**	**8.4**	11.4	22	<0	16.9	<0	N/A	N/A	<0
Size# (mm^2)	**0.62**	**–**	0.40	0.30*	0.10	0.24*	0.49	0.20*	0.18*	0.25*
Power density (mW/mm^2)	**47.6**	**34.5**	50.0	66.5	54.9	11.2	0.2	2.0	11.1	1.2
FOM‡	**37.7**	**41.1**	11.7	22.4	32.0	15.2	14.2	22.7	19.8	29.9
FOM1§	**39.5**	**42.7**	13.0	24.9	38.4	17.7	17.1	32.0	23.4	34.9

Note: #Exclude test pads. *Graphically estimated. **At –8.5-dBm input power. †$\mathrm{PAE} = 100 \times (P_{\mathrm{out,2nd}} - P_{\mathrm{in,1st}})/P_{\mathrm{DC}}$.
‡$\mathrm{FOM} = \left[10\log\left(\frac{100\times P_{\mathrm{out,2nd}}}{P_{\mathrm{in,1st}}+P_{\mathrm{DC}}}\right)+\mathrm{FR}\right]\times \mathrm{BW}$. §$\mathrm{FOM1} = \left[10\log\left(\frac{100\times P_{\mathrm{out,2nd}}}{P_{\mathrm{in,1st}}+P_{\mathrm{DC}}}\cdot\frac{1}{S_{\mathrm{core}}}\right)+\mathrm{FR}\right]\times \mathrm{BW}$.

balanced and double-balanced doubler chains is consistent with the analysis, showing that the double-balanced doubler chain has approximately 15-dB better fundamental rejection over more than twice the relative bandwidth. Ground shielding strategy and bandpass filters were implemented to enhance the fundamental rejection. A bandwidth broadening technique was employed to realize broadband drivers, ensuring the ultra-wideband performance of the doubler chain. The proposed double-balanced doubler chain delivers a peak output power of 14.7 dBm. Over 86.9% 3-dB bandwidth from 13.4 GHz to 34 GHz, the fundamental rejection is from 43 dBc to 65 dBc, and the third harmonic rejection is from 33 dBc to 56 dBc. This architecture comparison work provides useful insights for doubler designers and the proposed double-balanced doubler chain is a suitable candidate for mmWave applications due to its ultra-wideband, high fundamental rejection, high power, and high gain.

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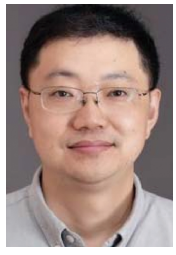

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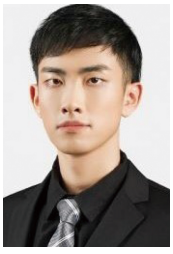

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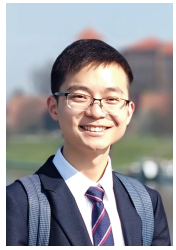

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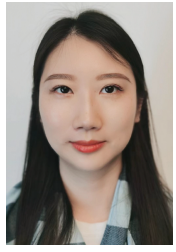

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