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RESEARCH ARTICLE

High Power GaN Doubler with High Duty Cycle Pulse Based on Local Non-reflection Design

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Abstract — The study focuses on the development of gallium nitride (GaN) Schottky barrier diode (SBD) frequency doublers for terahertz technology. The low conversion efficiency of these doublers limits their practical applications. To address this challenge, the paper proposes a multi-objective local no-reflection design method based on a three-dimensional electromagnetic structure. The method aims to improve the coupling efficiency of input power and reduce the reflection of power output. Experimental results indicate that the proposed method significantly improves the performance of GaN SBD frequency doublers, achieving an efficiency of 16.9% and a peak output power of 160 mW at 175 GHz. These results suggest that the method can contribute to the further development of GaN SBD frequency doublers for terahertz technology.

Keywords — Gallium nitride, Frequency doubler, Multi-objective optimization, Local non-reflection design.
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I. Introduction

Terahertz (THz) technology has been used in radar imaging, security, environmental monitoring, medical testing, high-speed communications and many other fields [1]–[7]. As part of the THz system, how to achieve high power output of terahertz frequency multiplier is an urgent problem to be solved. The traditional ways to increase the output power are increasing the number of anodes or using the power combination techniques. However, these methods are limited in effectiveness due to the low power-handling capabilities of gallium arsenide (GaAs).

In 2017, Dahlbäck *et al.* proposed a compact waveguide-encapsulated frequency doubler that utilizes Schottky diodes as varactors arranged in a 128-element grid. This doubler is capable of producing a peak output power of 0.25 W at 183 GHz with an input power of 1.32 W, resulting in a conversion efficiency of 19% [8]. In 2018, Siles *et al.* from JPL Lab reported a high-power 165–195 GHz doubler that features 24 anodes on a single 50 μm thick GaAs chip. The device comprises four multiplying structures, each containing six anodes on a Si-doped epitaxial layer. It can handle up to 3 W input power, providing a maximum output power of 800 mW [9]. In 2022, Dong *et al.* proposed a frequency doubler based on meta structure for the first time. By adding split-ring resonator (SRR) at the bottom of the diode, the electric field at the diode was strengthened, and the coupling efficiency between the diode and electromagnetic energy was improved. The performance of maximum output power is 45.2% better than of the traditional structure [10]. However, the tolerable power of GaAs Schottky barrier diode (SBD) limits the potential power output.

In recent years, there has been increasing interest in gallium nitride (GaN) semiconductor materials due to their significantly larger bandgap compared to traditional semiconductors such as GaAs. This unique property enables GaN-based power devices to achieve higher break-

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down voltages, resulting in their ability to handle greater power capacities [11]–[17]. Liang *et al.* from CEC 13 has published a series of GaN-based doubler, which cover frequencies of 180 GHz, 210 GHz and 300 GHz, achieving the highest power output in the pulsed state [18]–[21]. In 2020, Zhang *et al.* utilized an eight-node GaN SBD to improve the power handling capability of a 220 GHz tripler. The results showed that the maximum power processing capacity exceeded 1100 mW, with efficiency and maximum output are 1.6% and 17.5 mW, respectively [22]. In 2022, Liu *et al.* designed a GaN diode on a sapphire substrate, which demonstrated a high breakdown voltage of 54.9 V but achieved only a maximum efficiency of 3% with 500 mW input power.

Many of the published GaN frequency doublers suffer from low conversion efficiency, which can be attributed to various factors. One of the reasons is that the rapid increase in device temperature at high power input, which leads to a decrease in electron mobility. This decrease in electron mobility further exacerbates the rise in series resistance (R_s). Both the reduction in electron mobility and the increased R_s contribute to a decrease in the conversion efficiency of the device and can result in impedance mismatch.

To address the issue of high temperatures under high-power input, this study adopts a pulse testing method, which effectively reduces the average temperature of the device and mitigates the degradation of R_s. Moreover, by employing a multi-objective local non-reflection design method based on a three-dimensional electromagnetic model, the power losses of the device have been effectively reduced, resulting in an increased conversion efficiency. Ultimately, with an input power of 947 mW and utilizing a 10% duty cycle pulse model, the overall conversion efficiency approached 17%. This method provides a solution to the low efficiency problem in GaN doublers under high power input.

II. Frequency Doubler Based on GaN SBD

1. The design of GaN SBD

Silicon carbide (SiC) is a popular choice for substrate material in electronic devices to improve their power-handling capability. This is due to its close lattice match with GaN, which enables the growth of high-quality GaN films with excellent thermal conductivity on SiC substrates. Hence, SiC is well-suited for designing high-power electronic devices.

The structure of the diode is shown in Figure 1(a). To reduce parasitic effects, the thickness of the base is decreased to 30 μm. Furthermore, a highly-doped n^+ GaN layer (8×10^{18} cm^{-3}) with a thickness of 2 μm has been added to minimize ohmic contact resistance and spreading resistance. The epitaxial layer consists of a 200 nm n^- GaN layer (4×10^{17} cm^{-3}). The specific fabrication steps can be found in [19]–[21].

It should be noted that as the frequency increases,

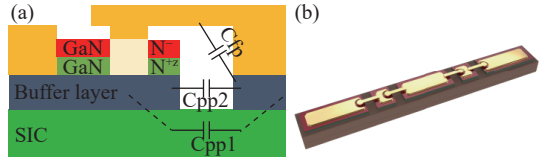

Figure 1 (a) Schematic cross-section of the GaN SBD; (b) 3D views of the GaN-based SBD chip.

the significance of parasitic effects in the terahertz frequency range becomes increasingly pronounced. The parasitic parameters between different layers and the physical structure of the SBD have a substantial impact on device performance. Hence, the establishment of a three-dimensional (3D) electromagnetic model is necessary.

Based on the layout provided by CETC 13th Research Institute, we accurately established a 3D SBD model and conducted simulations using HFSS, as depicted in Figures 1(a) and (b). This approach provides a higher level of confidence in achieving consistency between actual testing and simulation.

This paper presents the results of measuring the *C-V* and *I-V* (short for capacitance-voltage and current-voltage) characteristics of a single 6 μm diameter anode at room temperature. The *C-V* measurements show that the capacitance decreases from 58 fF to 13 fF as the anode voltage is swept from 0 V to −15 V, as depicted in Figure 2(a). The *I-V* measurements, plotted semi-logarithmically in Figure 2(b), indicate that the diode has a turn-on voltage (V_T) of 0.72 V and a reverse breakdown

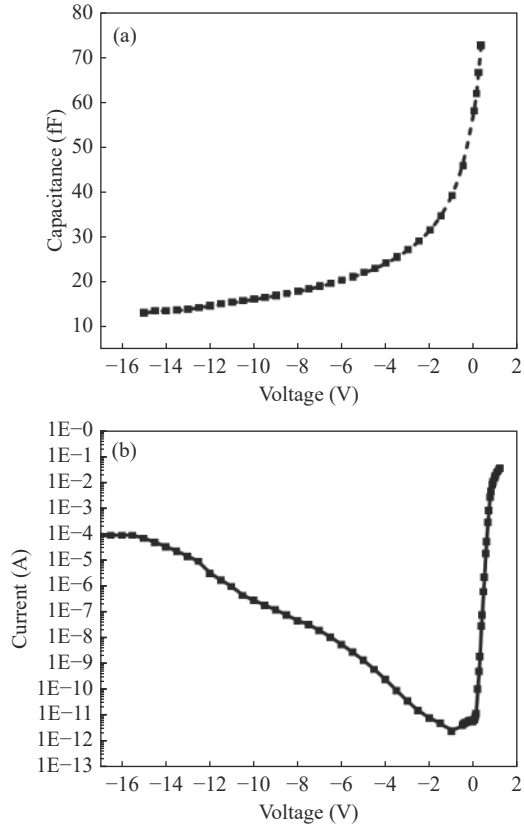

Figure 2 Characteristics of the fabricated GaN-based SBD. (a) Measured *C-V* curves. (b) Measured *I-V* curve.

voltage (V_{br}) of 15 V.

2. The design of frequency doubler

Figure 3 depicts the design process of a frequency multiplier, which involves the establishment of an ideal diode model and the extraction of diode parameters. Subsequently, a structure that can suppress odd harmonics is selected to enhance the conversion efficiency. Finally, impedance matching techniques are applied to design the circuit based on local non-reflection design. The design steps for the frequency doubler can be summarized in the block diagram as follows.

1) SBD impedance extraction

Initially, it is necessary to determine the theoretical maximum conversion efficiency of a single anode using the load-pull technique. As a nonlinear device, the operating state of a Schottky diode changes with drive power, working frequency, bias voltage, leading to fluctuations in the embedded impedance.

Figure 4(a) depicts the impedance extraction circuit of the diode in ADS. Using source pulling as an example, the diagram shows the impedance extraction circuit of a diode. To achieve the optimal frequency conversion efficiency, the circuit's source impedance (*Z*_source) needs to match the diode's fundamental impedance, while the load impedance (*Z*_load) needs to match the diode's harmonic impedance. This ensures efficient power transfer into the diode, enabling nonlinear operation and reflection-free output of harmonic power.

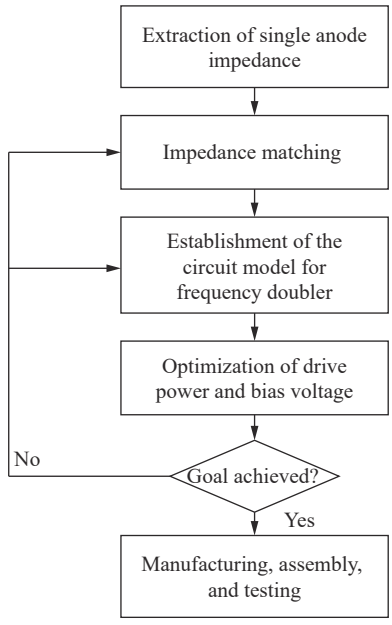

Figure 3 The block diagram of frequency doubler design.

Based on this, the source impedance (*Z*_source is 19.3 + j66.13 Ω) remains fixed, while the optimization of the load impedance (obtained through ADS for both input and output power) allows for the calculation of corre-

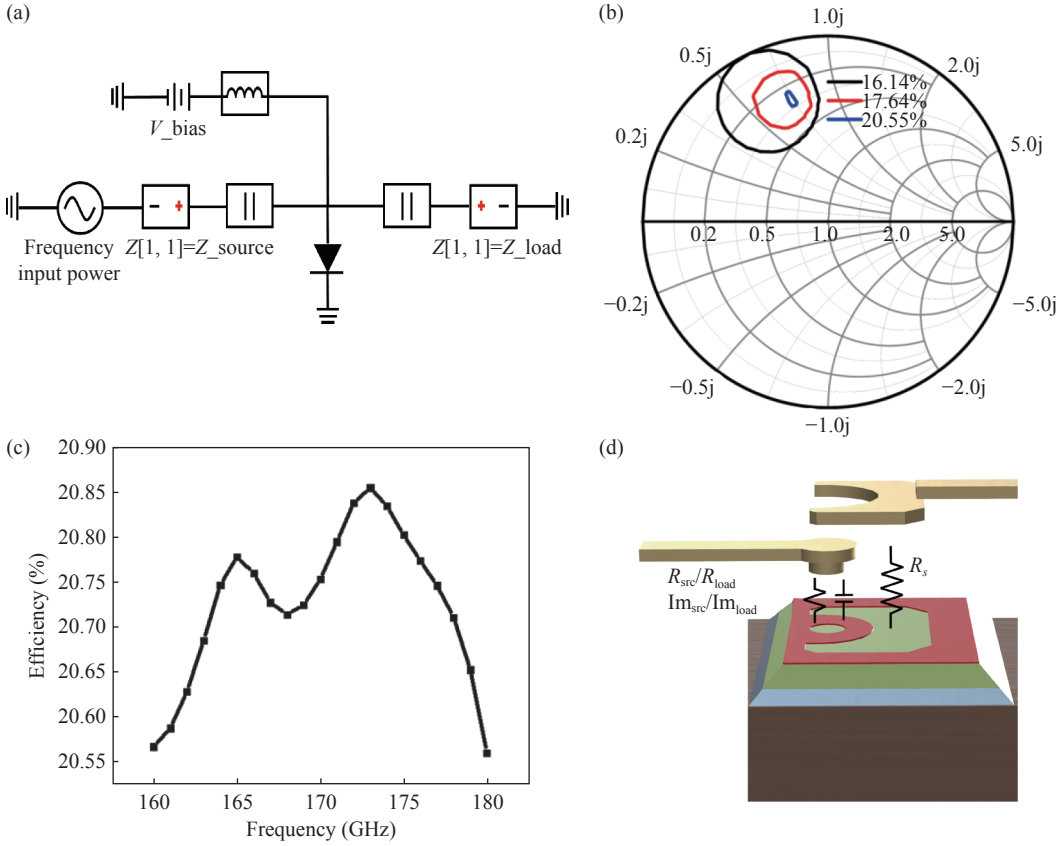

Figure 4 (a) The schematic diagram of diode impedance extraction circuit; (b) The diagram of the equal efficiency Smith circle; (c) The diagram of single anode optimum conversion efficiency; (d) The schematic diagram of diode embedded impedance.

sponding frequency conversion efficiency using the formula $P_{out}/P_{in} \times 100\%$. The equivalent efficiency Smith chart for different load impedances is shown in Figure 4 (b). When the conversion efficiency reaches its maximum, the load impedance can be determined. Similarly, load pulling is performed iteratively to optimize the source impedance.

The optimization results are shown in Figure 4(c), which indicate that the frequency doubler efficiency of a single anode exceeds 20% within the frequency range of 160 GHz to 180 GHz. Furthermore, the best driving power for the diode was found to be 25 dBm, with the optimal bias voltage being −6.5 V. The source impedance is 19.3 + j66.13 Ω, while the load impedance is 24.12 + j33.97 Ω which is embedded in the model shown in Figure 4(d). These optimized parameters ensure that the diode operates at maximum efficiency, providing reliable performance for frequency doubler applications.

2) The structure design of frequency doubler

To achieve high power output, a balanced structure is employed, featuring a diode connected in reverse series to the input fundamental signal and in parallel to the output harmonic signal. This design effectively suppresses the odd harmonics and greatly improves the system's efficiency which is shown in Figure 5.

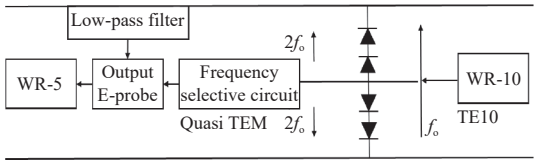

Figure 5 Circuit schematic architecture of the balanced structure.

The fundamental signal is fed directly to the diode chip via the WR-10 standard waveguide. Each harmonic generated by the nonlinear effect of the diode is in the TEM mode. In the balanced structure, input and output modes are well-isolated, preventing higher harmonic leakage into the input waveguide. Impedance matching is utilized to filter out unnecessary high harmonics, enabling only the second harmonic output to be retained. The resulting output signal is then transmitted to the standard waveguide WR-5 via a probe. The DC bias voltage connector is linked to a low-pass filter to supply power to the diode.

3) A multi-objective local non-reflection design method based on 3D electromagnetic structure

This paper proposes a multi-objective local non-reflection design method based on 3D electromagnetic structure to address the low efficiency issue in GaN frequency doublers. This method has two key features.

- In the terahertz band, the diode structure's parasitic parameters cannot be ignored due to the comparable wavelength and geometric size. To address these problems, we have adopted a novel approach, whose schematic diagram is shown in Figure 4(d), where we embed the extracted source and load impedances into a 3D electromagnetic model using HFSS. This method includes the influence of the anode impedance and electromagnetic structure in the *S*-parameters.
- Since the TE10 mode in the input waveguide is orthogonal to the harmonic quasi-TEM mode, the input and output parameters exhibit little influence. Therefore, as shown in Figure 6, the optimal efficiency can be achieved by independently optimizing the fundamental reflection coefficient and harmonic transmission coefficient through the adjustment of their respective structural parameters.

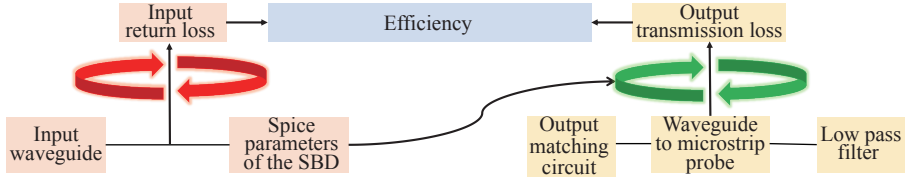

Figure 6 The diagram of a multi-objective local non-reflection design method.

The input and output matching circuits play a crucial role in the balanced structure of the frequency doubler. The input matching circuit is responsible for coupling the input signal into the diode, which is placed at the center of the wide side of the waveguide. As shown in Figure 7(a), a reduced-height waveguide extends to the opposite side of the diode pair, forming a backshort where the fundamental signal is reflected back into the input channel and separated from the output. By optimally adjusting the waveguide length (In_L1), width (In_W1), and shorted section length (In_L2), the input power can be efficiently coupled to the diodes.

Figure 7(b) shows that by optimizing the aforementioned parameters, we were able to achieve a reflection coefficient of −15 dB within the frequency range of 84 GHz to 87 GHz.

Due to the nonlinear effect of the Schottky diode pairs, the fundamental signal generates various harmonics. Therefore, it is necessary to design an output matching circuit to select the second harmonic output and suppress other higher harmonics. Figure 8(a) shows the HFSS model of the output matching circuit.

The output matching circuit consists of two parts: The first part is the matching circuit composed of suspension lines, which is used to select the output second harmonic; the second part is to use mode isolation to re-

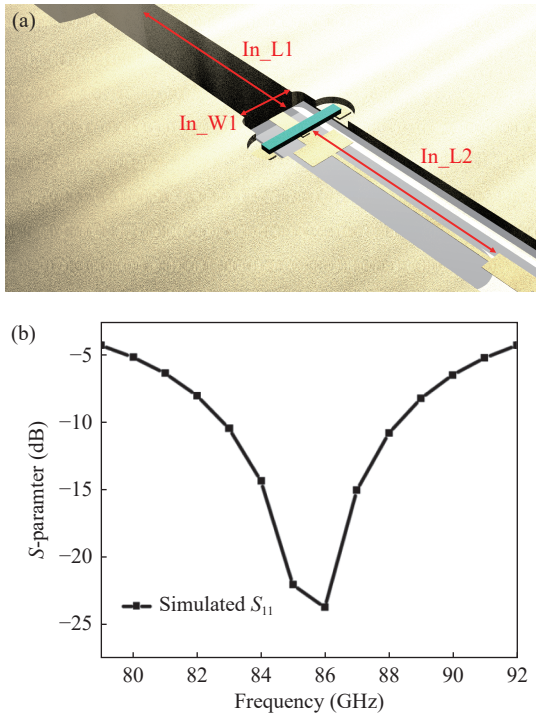

Figure 7 (a) The diagram of input structure of frequency doubler; (b) The reflection coefficient of input.

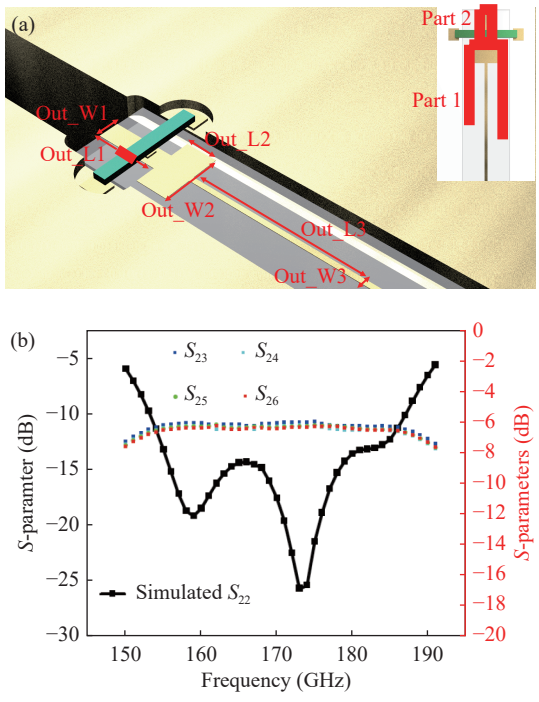

Figure 8 (a) The diagram of output structure of frequency doubler; (b) The reflection coefficient and transmission coefficient of output.

flect the second harmonic back to the diode pair.

The first part consists of the harmonic impedance matching branches, where the optimization of the length (Out_L2 and Out_L3) and width (Out_W2 and Out_W3) of the branch lines enables efficient transmission of the second harmonic. It should be noted that due to the fixed circuit structure and the impedance phase matching designed specifically for the second harmonic, other harmonics cannot efficiently propagate through the system.

At the end of the substrate, the suspended microstrip in the second part acts as a short circuit due to mode isolation and impedance mismatch. By optimizing the length (Out_L1) and width (Out_W1), the higher harmonic components generated by the diode are reflected back into the frequency multiplication circuit.

The optimization method is similar to the input matching circuit, where Out_W1, Out_W2, Out_W3, Out_L1, Out_L2, and Out_L3 are iteratively optimized until S_{22} is below −15 dB. The optimization results are shown in the Figure 8 (b), indicating that the total transmission coefficient remains around −6 dB and the reflection coefficient is lower than −15 dB from 155 GHz to 185 GHz.

Once the design of each individual component was completed, they were combined. The doubler model is shown in Figure 9, and the S-parameter generated by HFSS was imported into the ADS circuit. Then the relationship between the conversion efficiency, driving power, and bias voltage of the frequency doubler was analyzed. The HFSS model was further improved until the design requirements were met.

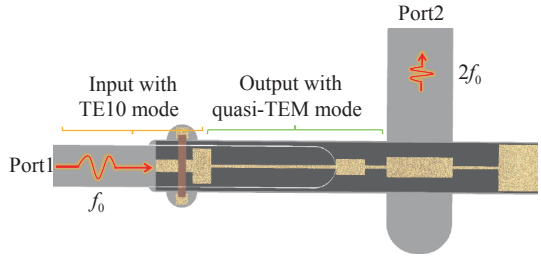

Figure 9 The diagram of frequency doubler based on GaN.

III. Simulation and Experiment

This paper presents a design method of 50 μm quartz substrate assembly for discrete GaN SBD, which effectively minimizes dielectric losses and enhances the efficiency of signal output.

As a portion of the input power is converted into higher-order harmonics, the majority of the power is converted into heat. Especially under high-power input, it leads to an increase in the anode temperature of the diode, resulting in lattice scattering and a decrease in electron mobility. This decrease in electron mobility, in turn, causes an increase in series resistance. On the other hand, at high power levels, the saturation of current significantly reduces the efficiency of the multiplier, as the junction capacitance cannot be optimally charged. Moreover, higher temperatures accelerate the power saturation, further compromising the device's performance [23], [24].

To reduce the average temperature of the device, a pulse input with a duty cycle of 10% is being utilized.

The block diagram of the experimental platform is illustrated in Figure 10(a). It consists of a signal generator and the six-times frequency multiplication stage. After that, an adjustable attenuation is connected to control the power into the 85 GHz power amplifier and stabilize the power into the GaN doubler at about 1 W. In addition, the input power required by GaN doublers can be adjusted through the attenuator to obtain a variable input power.

The performance of the optimized frequency doubler is shown in Figure 10. The conversion efficiency is maximum when the drive power is 1000 mW and the bias voltage of a single diode is −13 V. At the frequency of 174 GHz, the efficiency of the frequency doubler reaches 17.7%, and the output power is greater than 160 mW within the range of 171 to 178 GHz. Additionally, there is little difference in the performance of the extracted anode impedance when biased at −6.5 V and driven by a single anode power of 24 dBm.

Based on the theoretical analysis and simulations described, we have successfully fabricated and tested a GaN frequency doubler. The experimental results are in good agreement with the simulation results. When the bias voltage is set to −13 V, we observed the maximum output power, which is consistent with the simulation results. We obtained a maximum output power of 160 mW and a maximum efficiency of 16.9% at 175 GHz for an input power of 947 mW, with a pulse width of 100 μs and a duty cycle of 10%. Moreover, In the frequency range of 171 to 184 GHz, we achieved a typical output power of more than 100 mW and an efficiency of more than 10%.

Table 1 displays the available frequency doubler devices. It is clear that GaAs doublers have limited power handling capabilities, which significantly restricts the potential power output of THz doublers. On the other hand, some of the published GaN doublers exhibit superior power handling capabilities and higher power output, highlighting the advantages of GaN materials.

However, it should be noted that the development of continuous wave GaN doublers is a pressing issue that needs to be addressed in the future. Although some research institutions have proposed methods for continuous wave operation, as mentioned in references, these

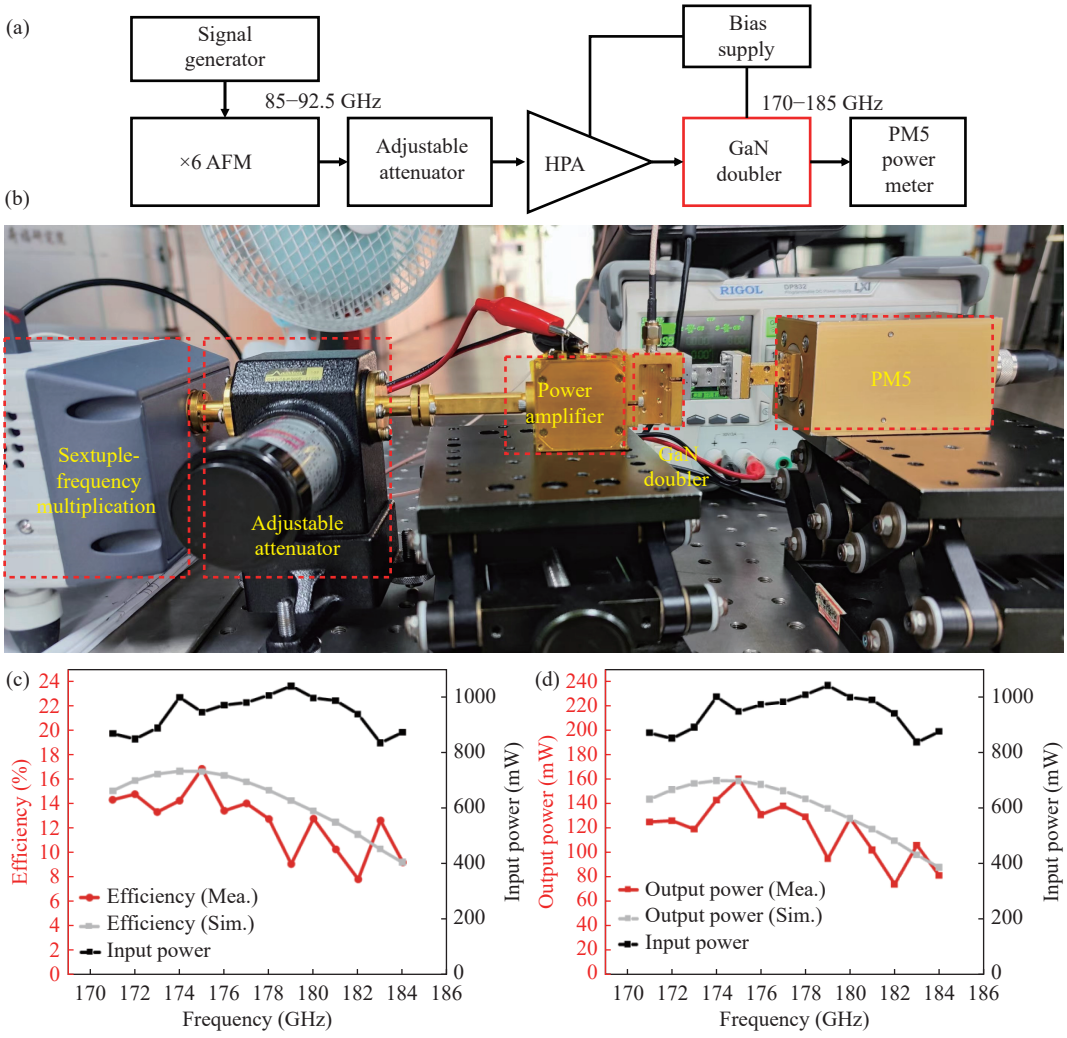

Figure 10 (a) The circuit diagram of the test circuit; (b) The photograph of the experimental platform; (c) Plot of simulated and measured output power (P_{out}) versus frequency; (d) Plot of simulated and measured conversion efficiency versus frequency.

Table 1 Summary of frequency doubler based on SBD

Reference	Frequency (GHz)	Duty	Anode number	Input power (mW)	Output power (mW)	Efficiency (%)
GaAs SBD-based frequency multipliers						
[25]	140–220	CW	2	32	4	12.7
[26]	110–170	CW	16	166	13.1	7.9
[27]	200–230	CW	6	214	38.2	17.8
GaN SBD-based frequency multipliers						
[21]	175–185	10%	8	2140	244	11.4
[19]	190–220	0.1%	12	7000	1006	15
[20]	290–307	1%	6	1320	183.4	13.9
[28]	100–110	CW	4	220	1.3	0.59
[29]	117–125	CW	6	500	15.1	3
[22]	200–220	CW	8	1100	17.5	1.59
[27]	205–230	CW	8	400	18.4	4.7
This work	170–185	10%	4	947	160	16.9

methods often exhibit lower efficiency.

To address the issues mentioned above, we will explore various solutions in the future, such as utilizing substrates with high thermal conductivity, employing structures with low thermal resistance, or using diamond substrates.

IV. Conclusion

To increase the output power of the frequency doubler, we use a GaN SBD with high power tolerance. Then, a multi-objective local no-reflection design method based on a three-dimensional electromagnetic structure is proposed. This method enhances the coupling efficiency of input power to the diode and reduces the power reflection of the second harmonic from the diode to the output waveguide. Experimental results demonstrate that the proposed method achieves a maximum output power of 160 mW at an input power of 947 mW, and a maximum efficiency of 16.9% at 175 GHz with a pulse width of 100 μs and a duty cycle of 10%.

Acknowledgements

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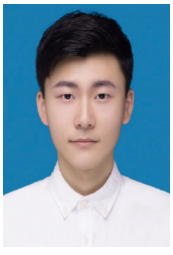

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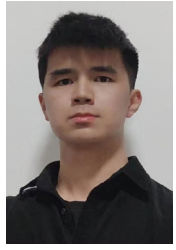

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