A Novel Transformerless Ultra Gain DC-DC Converter for Renewable Micro Energy Sources

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***Abstract*—This article proposes a novel Ultra Gain Cubic (UGC) DC-DC converter for integrating PV and Fuel cell into the grid. The proposed UGC converter is unique for its minimum component count, particularly for obtaining ultra gain when compared to existing DC-DC converters. The steady-state operation of the converter in both modes were explained and necessary equations were derived. The effect of parasitic elements on the UGC's DC-voltage gain is examined, and the stability of the UGC converter is verified using the state space averaging technique. Minimum number of components, ultra voltage gain, input and output terminals are connected to same ground, single switch, input current continuous are the key aspects of the UGC converter. A 300 W prototype with a 325 V output voltage is tested and validated using hardware results.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/8749

***Index Terms*—Ultra gain, Single switch, DC-DC converter, CCM, DCM, BCM .**

I. Introduction

Recent increase in the price of fossil fuels, and new laws restricting CO_2 emissions have raised interest in renewable energy options globally [1]. Solar and fuel cell technologies are well-known sources of renewable energy and have drawn a lot of attention. The output voltages of fuel cells and solar photovoltaics are extremely low [2]. Therefore, these low-voltage DC voltages are converted to high DC voltages (310 V - 600 V) by employing high-gain DC-DC converters, which also serve as a bridge between the source and the load. The applications of high voltage DC bus are shown in Fig. 1. Although conventional converters have the ability to boost the voltage, parasitic elements limit their gain [3]-[4].

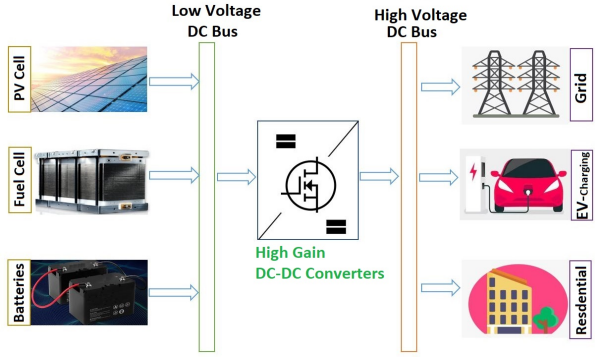

Fig. 1. High Gain DC-DC Converter: Need and Uses.

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Numerous converters have been reported by researchers with notable voltage gains, in an effort to fulfill the condition stated earlier [5]-[29]. By altering the transformer's turns ratio, isolated converters provide significant gains. Additionally, input-output isolation and safety are provided by isolated converters [6]. However, the stored leakage energy of inductors causes significant voltage spikes across the switches, necessitating extra circuitry to reduce these spikes, leading to an increased total cost [7]. Therefore, non-isolated DC-DC converters are better suited for attaining high voltage. The following set of major contributions highlights the importance of non-isolated converters. In [8], a modified SEPIC converter with a gain of $\frac{1+d}{(1-d)}$ is described, which requires two switches. In contrast, [9] achieves the same gain as [8], but with the extra benefit of just requiring one switch. A transformer-less step-up converter with a gain of $\frac{2}{(1-d)}$ is described in [10], which is superior to both [8] and [9]. On the other hand, it too requires two switches for operation, just like [8]. Remarkably, all three designs [8], [9], and [10] use only eight components, despite their differences.

[11] presents an enhanced SEPIC converter with a gain of $\frac{1+3d}{(1-d)}$, yet it suffer from common ground issues. In contrast [12] introduces a switched capacitor topology using regenerative network, offering a gain of $\frac{2-d}{(1-d)^2}$.

Both [11] and [12] use ten components, but [12] achieves a higher gain than [11] and incorporates a common ground feature. Nonetheless, its gain increase is moderate, and it still necessitates the use of two switches.

The topologies discussed from [8] to [12] are lower component count and cost-effective. Common ground problems, limited gain increase, and the need for multiple switches are some of the problems they face.

A switched capacitor (SC) boost converter is reported in [13]. Unfortunately, its efficiency is reduced by significant transient capacitor currents and it requires more number of capacitors.

Using coupled inductors is another method of enhancing voltage gain. However, leakage energy causes semiconductor devices to experience huge spikes in voltage and current and necessitates accurate inductors [14]. ZVS and ZCS techniques [15] can be used to reduce voltage spikes in coupled circuits. However, it requires additional components, making the overall system bulky and expensive.

The three level boost converter with less voltage stress across switches is reported in [16]. However, its gain is same as conventional boost.

According to the one mentioned in [17] has high gain at

lower duty ratios but having discontinuous input current and high input current ripple. An interleaved technique [18] can be used to reduce input current ripple, but it involves a more complex control circuit and additional components.

There have been several high voltage gain converters introduced in [19]–[20] that are based on voltage Multipliers (VM). It's possible for voltage multipliers to reduce the voltage stress across switching devices and make these converters much more voltage gain-oriented. To achieve high gains, though, more components of diodes and capacitors are needed.

The paper [21] suggests a cascaded boost converter that contains a single switch and achieves a gain that is equal to the square of a buck-boost converter. In contrast, the efficiency is lower and the gain enhancement is less. A VM -based converter has been reported in [22] that further increases voltage gain with a gain of $\frac{2+2d}{(1-d)}$. Even with seven capacitors and three inductors, the gain is not that much improved. According to the aforementioned literature, existing converters have several common problems, including low voltage gain, more number of components, bulky, common ground issues and low efficiency. Therefore, this article aims to overcome the mentioned limitations by introducing a novel switched LC network-based UGC converter.

II. Circuit Topology and Operation

For the integration of renewable energy sources into the grid, conventional boost, cuk, and flyback converters are commonly utilized. However, their gain is limited by parasitic elements, and efficiency degrades when voltage levels are higher. Therefore, the proposed UGC converter shown in Fig. 2 is a promising solution to overcome these limitations and facilitate the efficient integration of renewable energy.

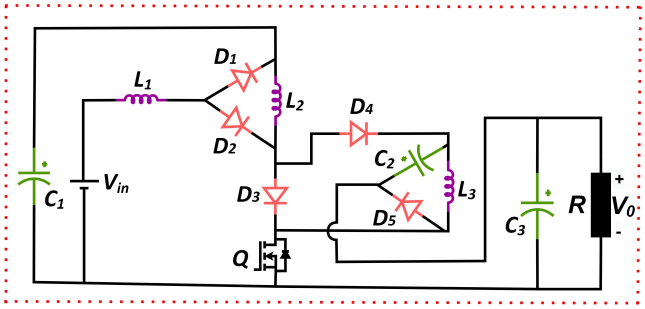

Fig. 2. The UGC converter.

The UGC converter has the following benefits over existing topologies

1. Ultra gain is achieved with minimum number of components
2. To get cubic gains, only one switch is needed.
3. The proposed converter provides a theoretical gain of 125 at d @ 0.8.
4. Without using any transformer or coupled inductors, the proposed UGC converter attaining higher gains. So high power density and overall cost is low.
5. Input current continuous, high efficiency (>90%), input and output are connected to same ground, are some additional advantages of the UGC converter.

The operating modes and waveforms in CCM and DCM were described, and the necessary equations were derived.

A. Continuous Conduction Mode

Mode-I [t_0 - t_1]:- As shown in Fig. 3, inductors L_1 ,L_2 and L_3 begin charging linearly when switch Q is in the ON state. V_{in} charges inductor L_1, capacitor C_1 charges inductor L_2, and energy stored in filter capacitor C_3 charges both inductor L_3 and capacitor C_2.

The theoretical waveforms of mode-I are presented in Fig. 5. The subsequent equations were derived using KVL and KCL.

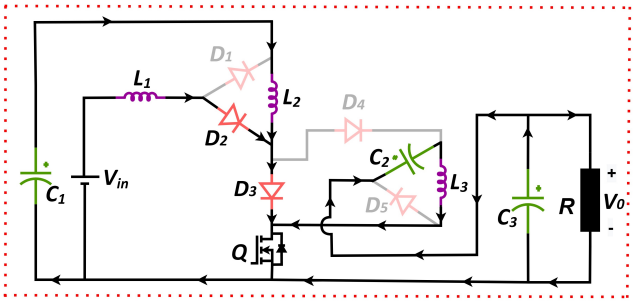

Fig. 3. Mode-I circuit diagram.

$$V_{L_1} - V_{in} = 0,\ V_{L_2} - V_{C_1} = 0 \& V_{L_3} - V_0 + V_{C2} = 0 \quad (1)$$

and

$$i_{C1(ON)} = -i_{L2}, i_{C2(ON)} = i_{L3},\ i_{C3(ON)} = -i_{L3} - i_0 \quad (2)$$

The above equations show that the circuit is operating as an ideal model, with the parasitic voltage drops of passive components and the ON-state resistance drops of switches and diodes being neglected. However, the model with these losses will be clearly discussed in the upcoming section.

Mode-II [t_1 - t_2]:- Upon turning off switch Q, the stored energy of inductor L_1 is released into capacitor C_1, whereas inductor L_3 releases its stored energy into capacitor C_2. Additionally, to filter capacitor C_3 and load, inductors L_1, L_2, and C_2 are discharged in conjunction with source voltage which is shown in Fig. 4.

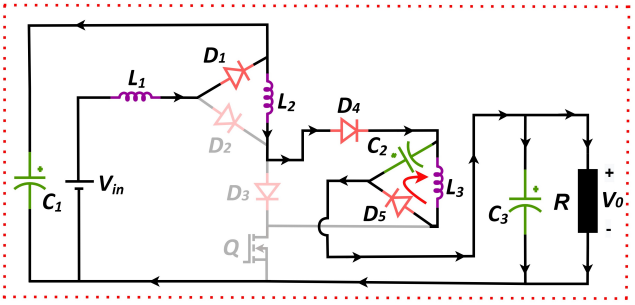

Fig. 4. Mode-II operation.

$$V_{L1} - V_{in} + V_{C1} = 0,\ V_{L2} - V_{C1} - V_{C2} + V_0 = 0, V_{L3} + V_{C2} = 0 \quad (3)$$

and

$$i_{C1(OFF)} = i_{L1} - i_{L2}, i_{C2(OFF)} = i_{L3} - i_{L2}, i_{C3(OFF)} = i_0 - i_{L2} \quad (4)$$

The voltage gain of the UGC converter in CCM (G_{VCCM}) is derived by applying the Volt-Sec balance equation for inductors, and it is obtained as

$$G_{VCCM} = \frac{1}{(1-d)^3} \quad (5)$$

By using Charge-Sec balance equation for capacitors C_1,C_2 and C_3, the current gain of UGC converter in CCM (G_{ICCM}) is obtained as

$$G_{ICCM} = (1-d)^3 \quad (6)$$

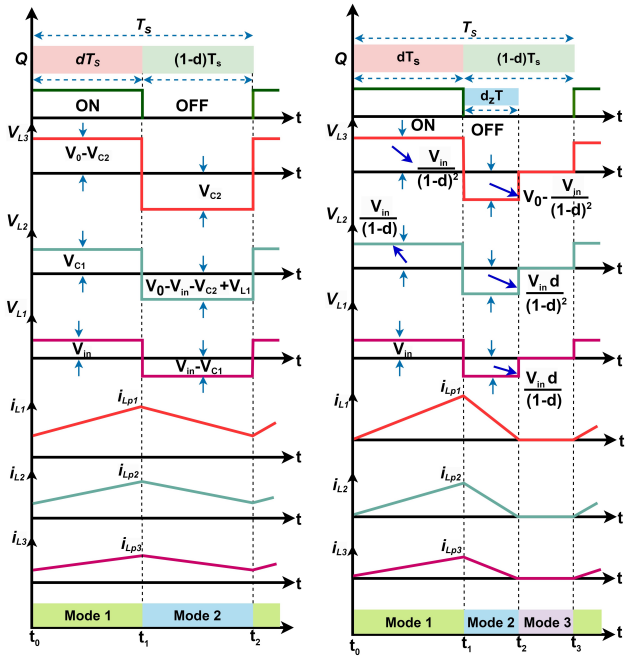

Fig. 5. Analytical waveforms in CCM and DCM modes.

B. Discontinuous Conduction Mode

The operating modes and corresponding theoretical waveforms in DCM are presented in Fig. 5.

Mode-I [t_0 - t_1]:- In terms of operation, this mode works similarly to Mode-I CCM. The peak value of inductor current L_3 is given by

$$i_{L_3} = \left(\frac{V_{in}}{(1-d)^2}\right) \times \frac{dT}{L_3} \quad (7)$$

Mode-II [t_1 - t_2]:- In this stage, the inductor current L_3 begins to decrease and eventually drops to zero at $t = t_x$. Apart from this, the remaining working operation and current paths same as Mode-II in CCM.

$$i_{L_3} = (V_0 d) \times \frac{d_z T}{L_3} \quad (8)$$

where d_z is unknown duty ratio which can be calculated by equating (7) and (8).

$$d_z = \left(\frac{V_{in} \times d}{V_0(1-d)^2}\right) \quad (9)$$

Mode III [t_2 - t_3]: As switch Q is turned OFF, inductor current L_3 becomes zero at moment t = t_3. The average output filter

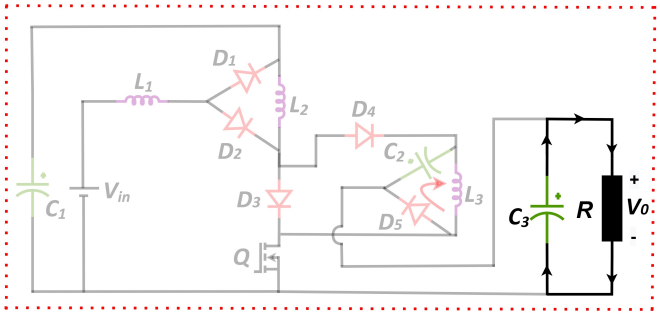

Fig. 6. Mode-III circuit diagram.

capacitor current shown in Fig. 6 is expressed as,

$$I_{C0} = \frac{1}{2} d_z I_{Lp3} - i_0 = 0 \quad (10)$$

Substitute (7),(9) in (10). After simplification, the voltage gain in DCM (k_{DCM}) is derived as

$$k_{DCM} = \frac{1}{(1+2d-d^2)} \left[\sqrt{\frac{d}{2\tau}}\right] \quad (11)$$

where,

$$\tau = \frac{L_3.f_s}{R}$$

C. Boundary conditions Mode

Under BCM mode, At particular instant of time inductor current shifts from continuous conduction mode to discontinuous conduction mode.

Both CCM and DCM's voltage gains are equal at this moment.

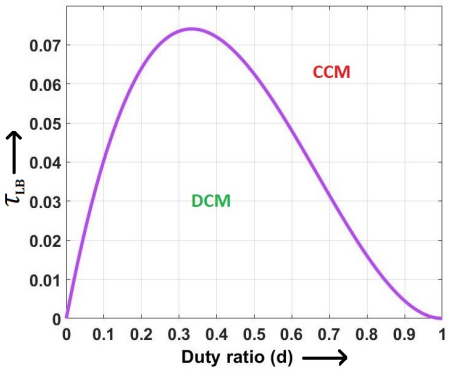

Fig. 7. CCM And DCM boundary plot.

So, by equating (5), (11) the boundary duty constant (τ_{LB}) of inductor L_3 is obatined as

$$\tau_{LB} = \frac{d.(1-d)^2}{2} \quad (12)$$

The relation between boundary duty constant and duty ratio is plotted in Fig. 7.

The critical output resistance (R_{crit}) of the UGC converter is expressed in terms of switching frequency (f_s) and duty ratio (d) using (12), and it is obtained as

$$R_{crit} = \frac{2.f_s.L_3}{(1-d)^2.d} \tag{13}$$

D. Parameter Design Converter

i. Inductor Design;- The value of the inductor is depends upon the switching frequency (f_s), allowable maximum inductor current ripples, duty cycle (d), and the supply voltage (V_{in}) . For best estimation, the ripple current Δi_L of the inductor should be chosen to be between 20% and 40% of the average inductor current. The selection of inductors for the UGC converter is based on the consideration of a maximum ripple current of 35% across the inductor.

$$\begin{cases} L_1 \geq \dfrac{d.V_{in}}{\Delta i_{L1}.f_s} \\ L_2 \geq \dfrac{d.V_{in}}{\Delta i_{L2}.(1-d).f_s} \\ L_3 \geq \dfrac{d.V_{in}}{\Delta i_{L3}.(1-d)^2.f_s} \end{cases} \tag{14}$$

ii. Capacitor Design:- The essential factor to consider when selecting capacitors is the acceptable voltage ripple. It is notable that the filter capacitor C_3 and intermediate capacitors C_1 & C_2 have a maximum permitted voltage ripple of 1% and 2% of their average values, respectively. The specifications to choose a size of capacitor are as follows:

$$\begin{cases} C_1 \geq \dfrac{d.i_0}{(1-d)^2.\Delta V_{C1}.f_s} \\ C_2 \geq \dfrac{d.i_0}{(1-d).\Delta V_{C2}.f_s} \\ C_3 \geq \dfrac{d.i_0}{\Delta V_{C3}.f_s} \end{cases} \tag{15}$$

iii.Voltage stress and Current stress :- The voltage and current stresses of switch and diodes are obtained as

$$\begin{aligned} \frac{V_Q}{V_{in}} &= \frac{1}{(1-d)^3}\,;\; I_Q = \frac{\sqrt{d}.(d^2+3(1-d))\,i_0}{(1+d(-3+3d+d^2))}; \\ \frac{V_{D1}}{V_{in}} &= \frac{-1}{(1-d)}\,;\; I_{D1} = \frac{i_0}{\sqrt{(1-2d+d^2)(1-d)^3}} \\ \frac{V_{D2}}{V_{in}} &= \frac{-d}{(1+d(d-2))}\,;\; I_{D2} = \frac{\sqrt{d}i_0}{(1+d(-3+3d+d^2))}; \\ \frac{V_{D3}}{V_{in}} &= \frac{-d}{(1+d(-3+3d+d^2))}\,;\; I_{D3} = \frac{\sqrt{d}.(2-d)i_0}{(1-d)^3} \end{aligned} \tag{16}$$

(17)

$$\begin{aligned} \frac{V_{D4}}{V_{in}} &= \frac{-1}{(1-2d+d^2)}\,;\; I_{D4} = \frac{i_0}{\sqrt{(1-d)^3}} \\ \frac{V_{D5}}{V_{in}} &= \frac{-1}{(1+d^3+d(-3+3d))}\,;\; I_{D5} = \frac{i_0}{\sqrt{(1-d)}} \end{aligned} \tag{18}$$

E. UGC Converter with Non-idealities

The voltage gain obtained in (5) represents an ideal voltage gain when all parasitic elements are considered to be negligible. In practical scenario, parasitic elements may have the significant effect on the output voltage. The UGC converter with paracitic elements taken into consideration is as shown in Fig. 8 and the output voltage with Non-idealities presented in (24) & Fig. 9.

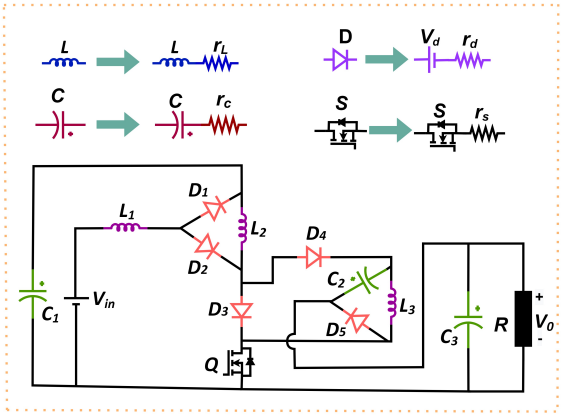

Fig. 8. UGC converter with non-idealties.

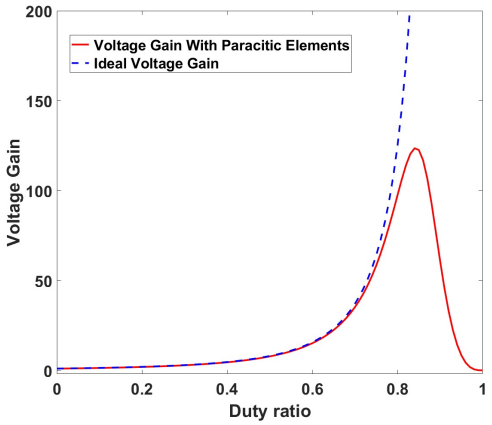

Fig. 9. Ideal and practical voltage gain of proposed UGC converter vs duty ratio plot.

F. Small Signal Modelling of UGC Converter

By using state space average technique, the proposed nonlinear switching converter has to be converted to linearised model and it is perturbed around operating point to get constant duty.

The state space equations written by considering inductor currents $i_{L01}, i_{L02}, i_{L03}$ and capacitor voltages $u_{C01}, u_{C02}, u_{C03}$ as state variables. The input voltage is $u_S(t)$, while the voltage across the load resistance R is output $u_0(t)$. The converter is assumed to be operated in CCM.

In Continuous Conduction Mode (CCM), the converter operates in two modes: Mode-I, where the switch is turned ON, and Mode-II, when it is turned off. The converter's state can be represented by its state space matrices, as shown in (19)

and (20), as well as the corresponding state average matrix, which is illustrated in (21).

The load resistance R and duty ratio are specified as 352 Ω and 0.5804, respectively. The control to output voltage transfer function is obtained in (23).

$$TF = \frac{\widehat{v_o}(s)}{\hat{d}} \tag{22}$$

$$TF = \frac{Z_5 s^5 + Z_4 s^4 + Z_3 s^3 + Z_2 s^2 + Z_1 s^1 + Z_0 s^0}{P_6 s^6 + P_5 s^5 + P_4 s^4 + P_3 s^3 + P_2 s^2 + P_1 s^1 + P_0 s^0} \tag{23}$$

As per the specifications provided in TABLE I, the poles and zeros of the transfer function can be computed as follows: $P_{1,2} = (1.0e03)(-0.0003 \pm 4.5341i)$, $P_{3,4} = (1.0e03)(-0.0005 \pm 2.8378i)$, $P_{5,6} = (1.0e03)(-0.0103 \pm 0.1806i)$, $Z_{1,2} = (1.0e04)(-0.0128 \pm 0.3536i)$, $Z_3 = (1.0e04)(-1.6867)$, $Z_4 = (1.0e04)(-0.1202)$, $Z_5 = (1.0e04)(0.0666)$

The location of poles and zeros ensure that the proposed UGC is stable. Like conventional boost converter, the UGC converter also has one zero in right half plane, which indicates that UGC a stable but non minimum phase system.

$$\begin{bmatrix} \frac{di_{L_{01}}(t)}{dt} \\ \frac{di_{L_{02}}(t)}{dt} \\ \frac{di_{L_{03}}(t)}{dt} \\ \frac{du_{C_{01}}(t)}{dt} \\ \frac{du_{C_{02}}(t)}{dt} \\ \frac{du_{C_{03}}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L_3} & \frac{1}{L_3} \\ 0 & -\frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_3} & 0 & 0 & -\frac{1}{C_3(R)} \end{bmatrix} \begin{bmatrix} i_{L_{01}}(t) \\ i_{L_{02}}(t) \\ i_{L_{03}}(t) \\ u_{C_{01}}(t) \\ u_{C_{02}}(t) \\ u_{C_{03}}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_S(t)$$

$$u_0(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L_{01}}(t) & i_{L_{02}}(t) & i_{L_{03}}(t) & u_{C_{01}}(t) & u_{C_{02}}(t) & u_{C_{03}}(t) \end{bmatrix}^T \tag{19}$$

$$\begin{bmatrix} \frac{di_{L_{01}}(t)}{dt} \\ \frac{di_{L_{02}}(t)}{dt} \\ \frac{di_{L_{03}}(t)}{dt} \\ \frac{du_{C_{01}}(t)}{dt} \\ \frac{du_{C_{02}}(t)}{dt} \\ \frac{du_{C_{03}}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & 0 & 0 & -\frac{1}{L_3} & 0 \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_2} & \frac{1}{C_2} & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & -\frac{1}{C_3(R)} \end{bmatrix} \begin{bmatrix} i_{L_{01}}(t) \\ i_{L_{02}}(t) \\ i_{L_{03}}(t) \\ u_{C_{01}}(t) \\ u_{C_{02}}(t) \\ u_{C_{03}}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_S(t)$$

$$u_0(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L_{01}}(t) & i_{L_{02}}(t) & i_{L_{03}}(t) & u_{C_{01}}(t) & u_{C_{02}}(t) & u_{C_{03}}(t) \end{bmatrix}^T \tag{20}$$

$$\begin{bmatrix} \frac{di_{L_{01}}(t)}{dt} \\ \frac{di_{L_{02}}(t)}{dt} \\ \frac{di_{L_{03}}(t)}{dt} \\ \frac{du_{C_{01}}(t)}{dt} \\ \frac{du_{C_{02}}(t)}{dt} \\ \frac{du_{C_{03}}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{d-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & \frac{1-d}{L_2} & \frac{d-1}{L_2} \\ 0 & 0 & 0 & 0 & -\frac{1}{L_3} & \frac{d}{L_3} \\ \frac{1-d}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{d-1}{C_2} & \frac{1}{C_2} & 0 & 0 & 0 \\ 0 & \frac{1-d}{C_3} & -\frac{d}{C_3} & 0 & 0 & -\frac{1}{C_3(R)} \end{bmatrix} \begin{bmatrix} i_{L_{01}}(t) \\ i_{L_{02}}(t) \\ i_{L_{03}}(t) \\ u_{C_{01}}(t) \\ u_{C_{02}}(t) \\ u_{C_{03}}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_S(t)$$

$$u_0(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L_{01}}(t) & i_{L_{02}}(t) & i_{L_{03}}(t) & u_{C_{01}}(t) & u_{C_{02}}(t) & u_{C_{03}}(t) \end{bmatrix}^T \tag{21}$$

III. Experimental Results

A 300-W laboratory hardware setup with a 325 V output and a 24 V input for the UGC converter has been constructed in accordance with the design displayed in Table I. The converter's Steady-State (SS) waveforms were recorded at V_{in}= 24 V and a duty cycle (d) of 0.59, resulting in an output voltage of 325 V which is shown in Fig. 10(a). The experimental waveforms of voltages across the inductors V_{L1}, V_{L2} and V_{L3}, along with their corresponding currents i_{L1}, i_{L2} and i_{L3} are displayed in Fig. 10(b) & Fig. 11.

The voltage across each capacitor C_1, C_2 and C_3 in Fig. 12 and Fig. 13(a) is 57.1 V, 187 V , and 324 V, respectively. The switching stresses for all diodes are as follows: V_{D1} is approximately 57.3 V, V_{D2} is approximately 71.2 V, V_{D3} is approximately 188 V, V_{D4} is approximately 136.2 V, and V_{D5} is approximately 324 V. These values may be found in Fig. 12 and Fig. 13(a). The experimental results in Fig.13

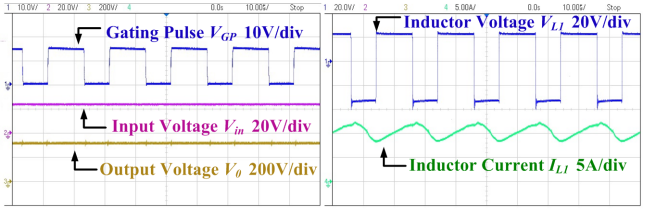

Fig. 10. Experimental results of (a) Gating pulse (V_{GP}), input voltage (V_{in}) and output voltage (V_0) (b) Inductor voltage (V_{L1}) and inductor current (I_{L1}).

show that the voltage stress between the switch Q and diode D_5 is approximately 324 V. Fig. 14(a) illustrates that the load current changes from 100% to 60% and finally to 80% with respect to the desirable output voltage, whereas Fig. 14(b) displays a three-step variations in the duty ratio.

$$V_0 = \frac{V_S - (1-d)V_{D1} - dV_{D2} - (2d-d^2)V_{D3} - (1-d)^2V_{D4} - (1-d)^5V_{D5}}{(1-d)^3 + a\frac{1}{(1-d)^3} + b\frac{1}{(1-d)^2} + c\frac{1}{(1-d)}} \tag{24}$$

$$a = \frac{1}{R} * \left\{r_{L1} + (d^3 + 3(d-d^2) * r_S + (1-d) * r_{D1} + d * r_{D2} + (2d-d^2) * r_{D3}\right\} \tag{25}$$

$$b = \frac{1}{R} * \left\{(1-d) * r_{L2} + (d^3 + 3d(1-d)) * r_S + (2d-d^2) * r_{D3} + (1-d)^2 * r_{D4}\right\} \tag{26}$$

$$c = \frac{1}{R} * \left\{(1+d^2-2d) * r_{L3} + (d^3 + 3d(1-d)) * r_S + (1-d)^3 * r_{D5}\right\} \tag{27}$$

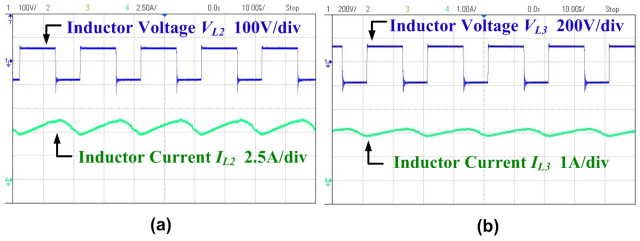

Fig. 11. Experimental results of (a) Inductor voltage (V_{L2}) and inductor current (I_{L2}) (b) Inductor voltage (V_{L3}) and inductor current (I_{L3}).

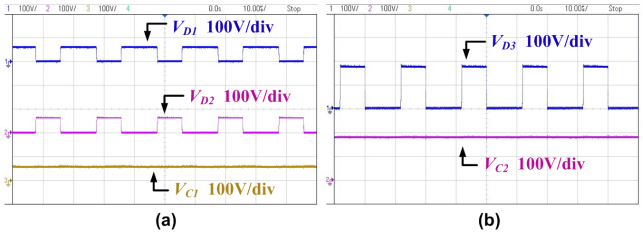

Fig. 12. Experimental results of (a) Voltage across diodes (V_{D1}, V_{D2}) and capacitor voltage (V_{C1}) (b) Voltage across diode (V_{D3}) and capacitor voltage (V_{C2}).

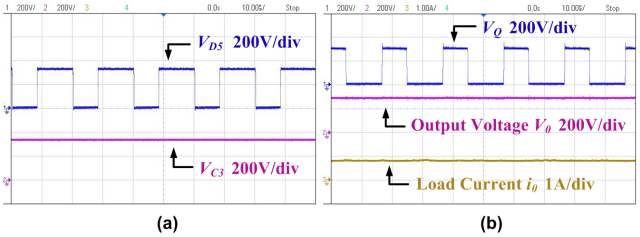

Fig. 13. Experimental results of (a) Voltage across diode (V_{D5}) and capacitor voltage (V_{C3}) (b) Switch voltage stress (V_Q), output voltage (V_0) and load current (i_0).

The maximum achievable efficiency in the experiment is recorded as 94.1%.

A. Performance Comparison of UGC Converter

In order to verify the UGC converter superiority over recent converters, a comparison analysis was done and shown in Fig. 15. A comparison study of proposed ultra gain converter with the existing converters in terms of output voltage gain, number of semi conductor devices, and number of storage elements and total count is presented in Table II. The UGC converter has one switch and five diodes, while the reported converters [23], [26], [27], [28], and [29] also contain one switch. However, the use of fourteen diodes in [24], seven diodes in [28], and six diodes in [29]. There are more number inductors and capacitors utilized in [24]. Compared to the UGC, the converters reported in [24], [27], and [28] use higher number of components and achieve lower voltage gain. The converter stated in [25] have the same voltage gain as the UGC , but requires three switches. In contrast to the converters described in [23], [24], [26], [28], and [29], the proposed converter provides a common ground feature.

Table III highlights the various converter losses associated with the inductor, switch, and snubber. Table III is formulated using the following values: L= 100 uH, C_s= 4.7 uF, f_s= 50 kHz, and i_0= 1A. For a 325 V output voltage, the duty ratios of the several converters were calculated. The UGC converter's duty ratio was 0.5804, while the ones reported in [26], [27], and [29] were 0.64, 0.67, and 0.74 respectively. In terms of performance comparison, the UGC converter has less losses than the ones reported in [26], [27] and [29].

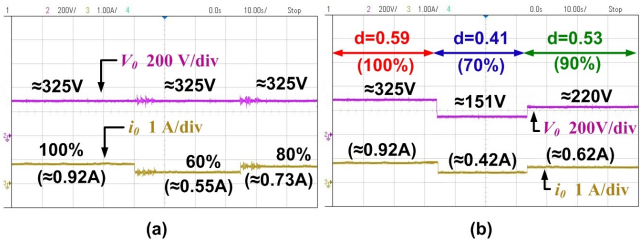

Fig. 14. (a) Dynamic variation of load current (i_0) when the load changes from 352 Ω to 586 Ω, and then to 440 Ω (b) Dynamic variation of output voltage (V_0) and load current (i_0) when duty ratio changes from 100% to 70% , and then to 90%.

TABLE I
SPECIFICATIONS OF UGC CONVERTER

Input Voltage V_{in}	24 V
Rated Power P_{out}	300 W
L_1, L_2, L_3	0.33 mH, 0.42 mH and 0.72 mH
Switching frequency f_s	50 kHz
C_1, C_2, C_3	22 uF, 47 uF, 110 uF
Mosfet Q	IRFP460
Power diodes D_1,D_2	MUR820
Power diodes D_3, D_4 and D_5	MUR860
Output Voltage V_0	325 V

TABLE II
COMPARATIVE ANALYSIS OF UGC CONVERTER WITH EXISTING TOPOLOGIES

Topology	[23]	[24]	[25]	[26]	[27]	[28]	[29]	Proposed UGC
switches	1	6	3	1	1	1	1	1
Diodes	4	14	3	3	5	7	6	5
Inductors	1	6	3	3	4	2	2	3
Capacitors	4	8	3	5	6	4	3	3
Total count	10	34	12	12	16	14	12	12
Voltage Gain	$\frac{3-d}{(1-d)}$	$\frac{3+d}{(1-d)}$	$\frac{1}{(1-d)^3}$	$\frac{d}{(1-d)^3}$	$\frac{1+2d-2d^2}{(1-d)^2}$	$\frac{3+d}{(1-d)}$	$\frac{2+2d}{(1-d)}$	$\frac{1}{(1-d)^3}$
CCM Gain d @ 0.8	11	19	125	100	33	19	18	125
Common Ground	No	No	Yes	No	Yes	No	No	Yes

TABLE III
PERFORMANCE WISE COMPARISON OF UGC CONVERTER

References	[26], 2023	[27], 2023	[29], 2021	Proposed UGC
Dutyratio Required	V_{in}=24 V d=0.63869	V_{in}=24 V d=0.62914	V_{in}=24 V d=0.7426	V_{in}=24 V d=0.5804
Output voltage	$24 \cdot \frac{d}{(1-d)^3}$ =325 V	$24 \cdot \frac{1+2d-d^2}{(1-d)^2}$ =325V	$24 \cdot \frac{2+2d}{(1-d)}$ =325V	$24 \cdot \frac{1}{(1-d)^3}$ =325V
Current through inductor L_1	$\frac{V_s}{L} \cdot dT_s$ = 3.065A	$\frac{V_s}{L} \cdot dT_s$ = 3.015A	$\frac{V_s}{L} \cdot dT_s$ = 3.565A	$\frac{V_s}{L} \cdot dT_s$ = 2.785A
Inductor Loss L_1	$\frac{(d.i_o)^2}{(1-d)^6} \cdot r_L$ =183.35 $\cdot r_L$	$i_o \left[\begin{matrix} 8d-4d^2- \\ \left(\frac{1}{d-1}\right)+ \\ \left(\frac{1}{(d-1)^2}\right)+1 \end{matrix} \right]^2$ $= 206.01 \times r_L$	$\frac{(4.i_o)^2}{(1-d)^2} \cdot r_L$ =241 $\cdot r_L$	$\frac{(i_o)^2}{(1-d)^6} \cdot r_L$ =183 $\cdot r_L$
Switch conduction Losses	$\frac{di_o{}^2}{(1-d)^6} \cdot r_{ds}$ = 117 $\cdot r_{ds}$	$i_o^2 d^2 \left[\begin{matrix} 6d-8d^2+ \\ \frac{(d-2)(2d-3)}{(d-1)^2} \end{matrix} \right]^2 r_{ds}$ $= 127.7 \cdot r_{ds}$	$\frac{16di_0{}^2}{(1-d)^2} r_{ds}$ = 179 $\cdot r_{ds}$	$\left(\frac{i_0}{(1-d)^3}\right)^2 dr_L$ = 106 $\cdot r_{ds}$

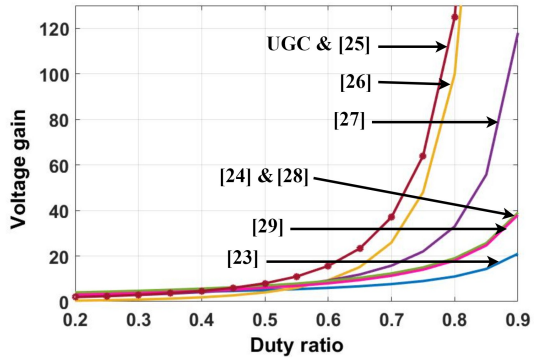

Fig. 15. Comparative DC voltage gain of UGC converter with existing topologies.

IV. CONCLUSION

In this paper, a novel UGC converter is proposed. The proposed converter was explained in CCM and DCM and condition for BCM also derived. A comparison with the latest literature converters highlights the benefits of the UGC converter further. The UGC converter was developed to have an output power of 300 W and an output voltage of 325 V. However, the voltage stress across the switch Q and diode D_5 is the same to that of the output voltage, which is a disadvantage. The experimental results validate that high voltage gain was obtained without using VM, coupled circuits and/or transformers. The UGC converter is an excellent choice for many applications such as Electric Vehicles, Smart lighting, Medical devices, Military applications, Renewable energy integration etc.

V. APPENDIX A

A. Calculation of Ideal Voltage Gain in CCM

The volt-sec balance relation for inductor L_1 is

$$V_{L1}(dT) + V_{L1}(1-d)T = 0 \tag{28}$$

from (1) & (3)
Voltage across inductor L_1 during switch ON (dT) period is V_{in} and voltage across inductor L_1 during switch OFF ((1-d)T) period is (V_{in}-V_{C1}). By substituting these values in (28), gives

$$V_{in}(dT) + (V_{in} - V_{C1})(1-d)T = 0 \tag{29}$$

by simplifying (29),

$$V_{C1} = \frac{V_{in}}{(1-d)} \tag{30}$$

similarly, the volt-sec balance relation for inductor L_2 & L_3 (using (1) & (3)) are obtained as follows

$$V_{C1}(dT) + (V_{C1} + V_{C2} - V_0)(1-d)T = 0 \tag{31}$$

$$(V_0 - V_{C2})(dT) + (-V_{C2})(1-d)T = 0 \tag{32}$$

simplifying (32), yields

$$V_0.d = V_{C2} \tag{33}$$

Substituting (30) and (33) into (31) gives the ideal voltage gain G_{VCCM} of the UGC converter in CCM.

$$G_{VCCM} = \frac{V_0}{V_{in}} = \frac{1}{(1-d)^3} \tag{34}$$

B. Calculation of Ideal Current Gain in CCM

The ideal current gain can be calculated by using charge-sec balance relation or using power balance relation. In an ideal converter, input power and output power are equal, which is written as

$$V_{in}.i_{in} = V_0.i_0 \tag{35}$$

rewriting (35) as

$$\frac{i_0}{i_{in}} = \frac{V_{in}}{V_0} \tag{36}$$

The ideal current gain G_{ICCM} of the UGC converter in CCM is obtained by using (34) in (36)

$$G_{ICCM} = \frac{i_0}{i_{in}} = (1-d)^3 \tag{37}$$

VI. Appendix B

A. Inductor Design

During Mode-I , the voltage across inductor L_1 is

$$V_{L1} = L_1 \frac{di_{L_1}}{dt} = V_{in} \tag{38}$$

i.e.,

$$V_{L1} = L_1 \frac{\Delta i_{L_1}}{dT} = V_{in} \tag{39}$$

Therefore , The inductor L_1 value is computed as

$$L_1 = \frac{V_{in}.d}{\Delta i_{L_1}.f_s} \tag{40}$$

similarly, the inductor values L_2 and L_3 are written as

$$L_2 = \frac{V_{L2}}{\Delta i_{L_2}} dT = \frac{V_{C1}}{\Delta i_{L_2}} dT = \frac{d.V_{in}}{\Delta i_{L2}.(1-d).f_s} \tag{41}$$

$$L_3 = \frac{V_{L3}}{\Delta i_{L_3}} dT = \frac{(V_0 - V_{C2})dT}{\Delta i_{L_3}} = \frac{d.V_{in}}{\Delta i_{L3}.(1-d)^2.f_s} \tag{42}$$

B. Capacitor Design

During Mode-I , the current through capacitor C_1 is

$$i_{C1(ON)} = C_1 \frac{dV_{C_1}}{dt} = i_{L2} \tag{43}$$

i.e.,

$$i_{C1(ON)} = C_1 \frac{\Delta V_{C_1}}{dT} = i_{L2} \tag{44}$$

Therefore , the value of capacitor C_1 is calculated as

$$C_1 = \frac{i_{L2}}{\Delta V_{C_1}} dT = \frac{d.i_0}{(1-d)^2.\Delta V_{C1}.f_s} \tag{45}$$

similarly, the values of capacitors C_2 and C_3 are obtained as

$$C_2 = \frac{i_{L3}}{\Delta V_{C_2}} dT = \frac{d.i_0}{(1-d).\Delta V_{C2}.f_s} \tag{46}$$

$$C_3 = \frac{i_0}{\Delta V_{C_3}} dT = \frac{d.i_0}{\Delta V_{C3}.f_s} \tag{47}$$

C. Diode Voltage Stress

During CCM Mode-I , diodes D_1, D_4 and D_5 are not conducting. By applying KVL to Mode-I circuit, the following equations were obtained.

$$V_{D1} = V_{in} - V_{L1} - V_{C1} \tag{48}$$

$$V_{D5} = -V_{C2} - V_{L3} \tag{49}$$

$$V_{D4} = V_{in} - V_{L1} + V_{C2} - V_0 \tag{50}$$

Using (1), (30) and (33) to solve (48), (49), and (50) yields

$$V_{D1} = \frac{-V_{in}}{(1-d)} \tag{51}$$

$$V_{D4} = \frac{-V_{in}}{(1-2d+d^2)} \tag{51}$$

$$V_{D5} = \frac{-V_{in}}{(1+d^3+d(-3+3d))} \tag{52}$$

Similarly, during CCM Mode II, the following KVL equations were obtained for the diodes D_2, D_3.

$$V_{D2} = V_{in} - V_{L1} + V_{C2} - V_0 \tag{53}$$

$$V_{D3} = -V_{L3} \tag{54}$$

Using (3), (30) and (33) to solve (53) and (54) gives,

$$V_{D2} = \frac{-V_{in}.d}{(1+d(d-2))} \tag{55}$$

$$V_{D3} = \frac{-V_{in}.d}{(1+d(-3+3d+d^2)} \tag{56}$$

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