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Establishing On-Wafer Calibration Standards for the 16-Term Error Model: Application to Silicon High-Frequency Transistor Characterization

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ABSTRACT This work focuses on a novel methodology to establish on-wafer calibration standards for the 16-Term Error Calibration Technique. It combines TRL-calibrated data with EM simulation to precisely generate S-parameters of standards. Applied to the advanced BiCMOS 55 nm technology, with a layout maintaining consistent coupling between standards, the 16 error-terms calibration results in significant improvements from 40GHz onward compared to standard calibration (SOLT or TRL) techniques. Notably, it corrects probe couplings, eliminates discontinuities between frequency bands, and ensures the accuracy of S-parameter measurements. Unlike traditional SOLT and TRL methods, this new approach attributes measured quantities solely to intrinsic transistor behavior.

INDEX TERMS RF probes, on-wafer measurement, S-parameters, mmW, f_{MAX} determination, SiGe HBT, RF inductors, RF MOSFET, TRL calibration, SOLT calibration, 16 error-terms calibration.

I. INTRODUCTION

Intense competition is taking place between the various semiconductor foundries as they strive to provide increasingly efficient technologies to meet the growing demand for millimeter-wave applications. In a specific BiCMOS technology context, the SiGe HBT transistor holds a central position, offering an excellent balance between cost and performance. To boost transistor performance, process engineers continually shrink device dimensions and reduce both extrinsic and intrinsic capacitances. These elements are in the order of few fF making them extremely prone to measurement errors. Meanwhile, advancements in on-wafer probes have lagged behind the rapid evolution in the semiconductor industry, leading to a commensurate increase of parasitic interference over time. Indeed, commercial RF probes do not guide perfectly the EM field towards the device and are coupling with the substrate or are coupling together generating crosstalk. This is the reason why f_{MAX} value (frequency where the maximum power gain is equal to 1) becomes extremely difficult to determine as it is mentioned in [1]. In [2], it was demonstrated that the f_{MAX} measurement is sensitive to probe couplings and nor the off-wafer SOLT, nor the on-wafer TRL calibration is able to correct them completely whatever the probe topology that was used, thus new efforts must be deployed for accurate and reliable on-wafer S-parameter measurements.

While the SOLT calibration limitation was highlighted in different works [3], [4], the on-wafer TRL calibration has been highly recommended especially for metrology [5]. Indeed, this method is self-consistent and does not require input parameters except dimensions of the different lines and a pad-load test structure to extract the line characteristic impedance [6], [7]. The TRL method is also able to properly account for probe-substrate coupling when calibration is possible directly on the wafer, but only when crosstalk is completely negligible.

Its main constraint is the inability to consider crosstalk. In specific studies in the field of measurement technology, this can be circumvented by a large distance between the probes, such as in [5], where an inter-pad distance of about 350 μm is used. On the other hand, advanced Si technologies have a high cost per square millimeter requiring an increase in the density of the test structures used for device characterization and compact modelling.

During the last years, different attempts have been proposed to account for probe leakage using improved 10 to 12 error terms models [8], [9], [10], [11]: Unfortunately, demonstration of the capability of these methods is often applied to attenuators, but their efficiency is not verified on advanced high-frequency transistors measured on the wafer.

Going back in the past, in 1991, Butler etal. introduced a 16-term error model (16T) [12] following pioneering work from Speciale in 1977 [13]. Out of the 16 error terms available, eight are specifically designated for modeling the couplings from port 1 to port 2. This configuration proves to be highly effective, especially in scenarios where significant crosstalk errors are prevalent, such as in on-wafer measurements. However, despite the evident advantage of this approach, the utilization of all 16 error terms for calibrating high-frequency transistor measurements, as observed in the literature, remains relatively sparse. [14], [15], [16]. For example, [14], [15] employed 16T with on-wafer calibrations for transistor characterization on a 130 nm MOSFET device. Although the calibration standards were modeled using lumped elements, the procedure resulted in quantifiable improvements compared to standard methods. In [17], [18], the optimal set of test-structures for 16T-calibration including aspects as reciprocity and symmetry has been investigated. However, it is important to note that ideal behavior was assumed for the test structures.

In 2014, Williams et al. [16] combined 16T with the TRL. The procedure involves two steps: i) Utilizing the TRL calibration algorithm to find the basic error terms describing the VNA; ii) Employing the orthogonal distance regression algorithm to solve for the interior crosstalk terms of the 16-term calibration model. While the introduction of the work [16] highlights the impact of crosstalk on high-frequency transistor figure of merit (FOM) measurements and the need for consistent measurements across different frequency bands implying the use of two different probe geometries [19], [20], the primary focus of the study pertains to recommending optimal designs for coplanar waveguide (CPW) access lines and evaluating the algorithm's capability to mitigate crosstalk in the presence of parasitic propagation modes. The case of the microstrip line used in the complex back-end of the line (BEOL) of silicon technologies remains unaddressed.

Another way to effectively utilize the 16-term error model, is to have appropriate standards and more importantly, an accurate S-parameters description of these standards [21]. At lower frequencies, these calibration standards can be treated as ideal components; however, this changes at higher frequencies. high frequency. The access lines, the vias descent, and EM couplings begin to affect the S parameters. Consequently, these calibration standards can no longer be considered as ideal lumped components, significantly impacting calibration accuracy.

In this context, we elaborated a methodology to obtain a reliable description of the calibration standards for the 16-term error calibration. An EM-simulation-based approach for obtaining calibration standards has previously been utilized by [22] to derive the characteristic impedance for TRL calibration. In our work, we rely on meticulously adjusted electromagnetic (EM) simulation data that describe the 16-term error term calibration standards using on-wafer TRL calibrated line standards. All the calibration structures are implemented directly on the wafer, ensuring consistent error terms between the calibration step and the measurement of the device under test (DUT).

The paper is organized as follows: I) the layout of the test structure is presented; II) the calculation of 16 terms calibration standards using TRL calibration and EM simulation is thoroughly explained; III) measurement setup and procedure are described; and finally, IV) results are analyzed.

II. LAYOUT DESIGN

The fabricated test structures are dedicated to both on-wafer TRL and 16T. These structures are implemented on the BiCMOS 55 nm technology from STMicroelectronics having 8 levels of metal (see Fig. 1). They comprise a set of microstrip lines using top-metal M8 for the design of the line and the lowest metal level M1 for the ground plane. These lines vary in length from 558.9 μm to 64.35 μm. A set of test-structures including a reflect, pad-short, pad-open, open-M8 and short-M8 are also implemented. These structures are symmetric between port 1 and port 2. The die also contains specific asymmetric structures recommended for the 16T procedure such as short-load and load-short configurations. Indeed, the 16T calibration approach requires at least 4 standards to resolve the 16 equations using the SVD Singular Value Decomposition (SVD) algorithm, and asymmetric structures are required for a more robust solution of the SVD algorithm. In this work, we use 5 standards meaning that the system of equation during SVD calculation is overdetermined.

Regarding the layout arrangement, there is a sufficient spacing between the structures, and a staggered positioning of the test structures is implemented to reduce the influence of adjacent structures. The aim of this work is to measure very small crosstalk-related quantities, which must not be disturbed by coupling to neighboring structures. Indeed, different research labs [23], [24], [25] [26] and [27] have shown that measurement results can be influenced by the adjacent structures, resulting in erroneous S-parameters. Therefore, in our specific case, the spacing between DUTs is large (Δx = 207 μm, Δy = 133 μm) mitigating the influence of neighboring structures [27].

More importantly, a continuous ground plane was used between structures which suppresses the penetration of the EM wave into the substrate [28]. Hence, the probe coupling

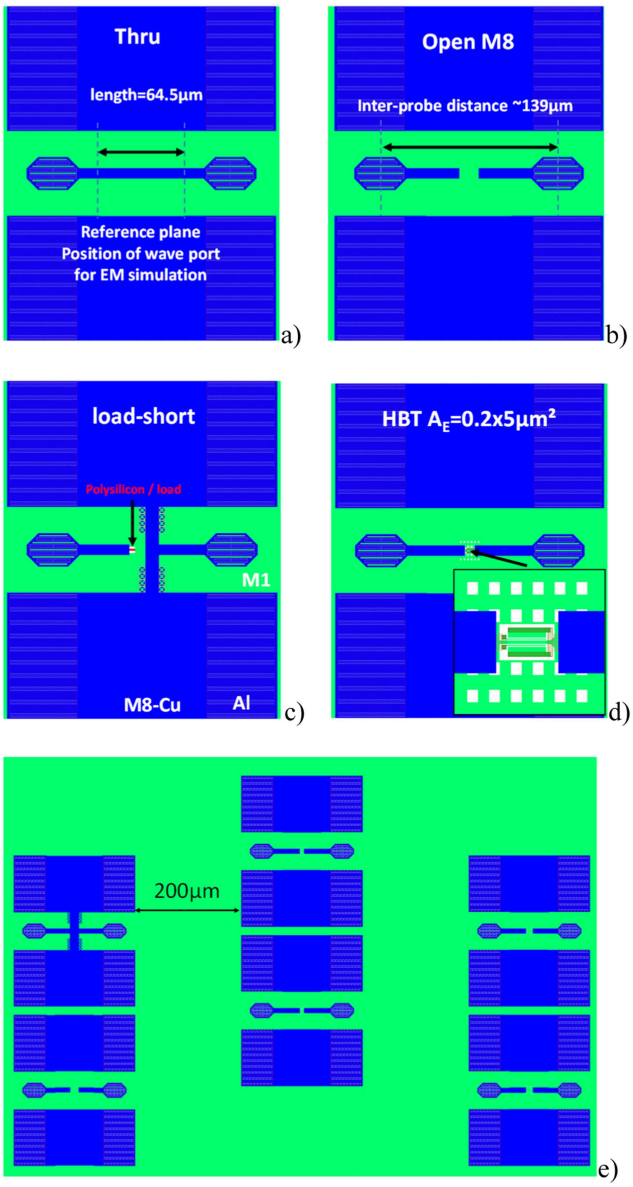

FIGURE 1. Layout of the principal test-structures highlighting distance between probes (dummies have been simplified for clarity); (a) Thru, (b) Open-M8, (c) the load-short structure is also illustrative for the load-load or short-short structure using the symmetry, (d) HBT, (e) floorplan view of some of the structures highlighting the arrangement.

is not influenced by the coupling with the substrate as it was the case in [16], but is instead confined to the air coupling. Therefore, the probe crosstalk and the probe-to-substrate coupling remain consistent across all structures which has to be guaranteed as initial condition.

III. DEFINITION OF 16T STANDARDS USING BOTH TRL CALIBRATION AND EM SIMULATION

Given that the proposed 16T approach relies on a precise knowledge of the standards obtained from EM-simulation, the key component is meticulous adjustment of the EM simulator

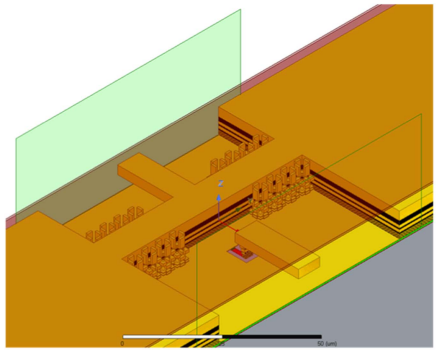

FIGURE 2. Electro-Magnetic simulation structure used to define the standards: 3D view of the load-short structure.

to generate accurate S-parameters for the standards. The required material parameters include the complex permittivity of the dielectrics stack of the BEOL, the conductivity of the top and bottom metal layers, the conductivity of the 50-ohm resistor layer as well as the resistivity of the via material.

The design rule manual, combined with the layout, provides a comprehensive understanding and definition of the structures intended for use as standard. This information includes the conductivity of each layer, ranging from top metal to the polysilicon layer which is used to create the 50 Ohm load (see Fig. 2). This information can be validated by I-V measurement of the test-structures such as the lines, to extract parameters like the top metal conductivity or the resistance of the pad-load. Unfortunately, the complexity of the back end of the line (BEOL) hinders the simulation of the complete set of test structures without simplification. To address this, the intricate BEOL structure is replaced with an equivalent dielectric. The equivalent dielectric parameters are derived from line measurements obtained from the TRL calibration, along with the obtained propagation coefficient of the line. The dielectric loss of the equivalent dielectric is determined by the real part of the propagation coefficient, which is correlated to both conductive and dielectric losses.

Conductive loss primarily depends on the top metal conductivity, which can be obtained from the design rule manual or through I-V measurement. By knowing the total loss from the TRL measurement via the real part of the propagation constant, the dielectric loss can be determined. The validity of this tuning step is verified on the thru, as shown in Fig. 3, where the EM simulation result is compared with the TRL-measured thru. For accurate EM simulation, the via resistance value and the material resistivity parameter of the polysilicon layer used as the load are essential. The former can be obtained from RF measurement of the transistor short, while the latter can be validated from RF measurement of the load calibrated from TRL.

IV. MEASUREMENT SETUP AND PROCEDURE

Concerning the measurement setup, an E8361A Vector Network Analyzer (VNA) from Agilent was used capable of

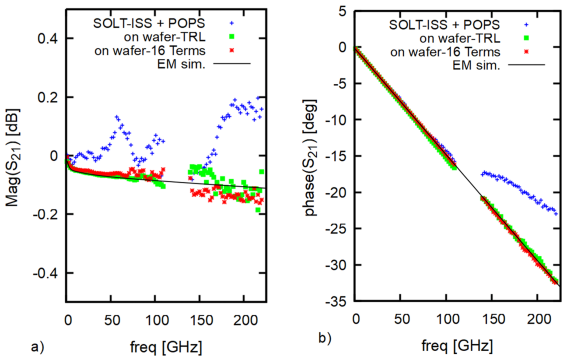

FIGURE 3. (a) Magnitude and (b) phase of S21 of the thru versus frequency. Comparison of the different calibration method (SOLT-ISS + PO-PS de-embedding, on wafer TRL, 16 terms, EM simulation). (6 calibration standards used for 16-terms method).

operating up to 110 GHz. Extenders (N5260-60003) were employed for frequencies above 67 GHz. The intermediate frequency bandwidth (IF) was set to 10 Hz and the power level was adjusted to approximately-32 dBm for frequencies up to 67 GHz. For frequencies above 67 GHz, the power was maintained below −30 dBm, achieved through the use of mechanical attenuators. This power level was selected to ensure the linear operation of the transistor. Then, two types of probes were employed depending of the frequency band: FormFactor Infinity XT 110 probes having a 50 μm pitch and FormFactor Infinity 140-220 GHz probes with 100 μm pitch. For off-wafer calibration, these probes are used in combination with the CS138356 and CS138357 alumina calibrations kit, depending on the probe pitch. Three calibrations are performed concurrently: SOLT-ISS, on wafer TRL, on wafer 16-term calibration.

Raw measurements are conducted on each calibration structure and test-structure, which can be off-wafer when applying ISS SOLT or on-wafer for TRL and 16T. The first step involves measuring the off-wafer calibration standards for the SOLT method: a short, a load, a thru and an open on alumina, which are raw measured on CS138356 or CS138357 depending on the frequency band. The second step concerns on-wafer structures having the same inter-pad distance, signifying the same inter-probe distance: raw measurements are conducted for the thru, open, short, load, short-load, load-short, and transistor along with their associated open and short de-embedding structures. Finally, raw measurements are conducted of the on-wafer line test-structures. In this step, the inter-probe distance needs adjustment due to varying line lengths of the test structures. As the crosstalk error terms are directly linked to the positioning of the inter-probe distance, this measurement phase is conducted at the conclusion to maintain consistency, ensuring identical inter-probe distances for the measurements of all other test structures. This measurement procedure is repeated on the two different bands, 1–110 GHz and 140–220 GHz. Hence, when comparing SOLT, TRL, and 16T methods, the input data are exactly the same ensuring a fair comparison.

Regarding the SOLT, the 12 error terms are computed using the raw measurement of the off-wafer alumina standards in conjunction with the parameters of the standards given by the calibration-kit manufacturer. The reference plane is set at the probe tips, i.e., at the transition from the probe-tips to the pads.

For on-wafer TRL calibration, two separate transmission lines are utilized to cover the entire frequency range band: the primary line, with a length of 558.9 μm, operates up to 80 GHz, whereas a shorter line measuring 297 μm covers the frequency range from 80 GHz to 220 GHz. These lines are paired with a thru standard measuring 64.35 μm. A short reflector is utilized for TRL calibration, and an impedance correction is applied using a load structure. The calibration planes of the on-wafer TRL calibration have been shifted back on both sides of the thru (see Fig. 1(a)) using the propagation constant computed by the TRL algorithm.

Thru, open, short, load, short-load are the five on-wafer standards selected for calculating the 16 error terms of the 16T model. To ensure a consistent comparison, the reference plane of the 16-term calibration method is aligned with that of the TRL calibration. This is achieved by positioning the ports during the EM simulation of the structure at exactly the same location.

Since the reference plane positions differ between the SOLT and TRL/16T calibrations, adjusting the reference plane of the SOLT requires applying a pad-open/pad-short de-embedding.

V. RESULTS

A. STANDARDS

To ensure the accuracy of the 16T standards, one can initially use the thru standard and compare its accuracy with other calibration procedures, especially with on-wafer TRL, which is self-consistent (see Fig. 3). This comparison reveals that the 16-term calibration closely aligns with the TRL calibration for both the magnitude and phase of S_{21}. The discrepancy is less than 0.025 dB at 60 GHz.

Additionally, it can be noted that the phase of S_{21} after SOLT-ISS, following pad-open and pad-short de-embedding, exhibits similar results to TRL at lower frequencies. However, discrepancies begin to emerge as the frequency exceeds 90 GHz. Concerning the magnitude of S_{21}, a fluctuating error of less than 0.2 dB is observed from 40 GHz to 220 GHz for SOLT-ISS. This confirms the limitation of the SOLT-ISS for measuring accurately a transmission line at high frequency.

It is of interest to analyze the results for the symmetric load structure (see Fig. 4). Note that this structure is not a pure load; it encompasses the access line, the via descent and the 50-Ohm resistor. Therefore, a very small cross-talk exists due to the coupling between the two access lines. The TRL and the SOLT-ISS methods, which inherently lack the capability to accurately estimate the coupling from port 1 to port 2, exhibit a coupling approximately 10 dB higher than that obtained through the 16T. Additionally, discontinuities are observed at the transition of frequency bands for both the SOLT-ISS

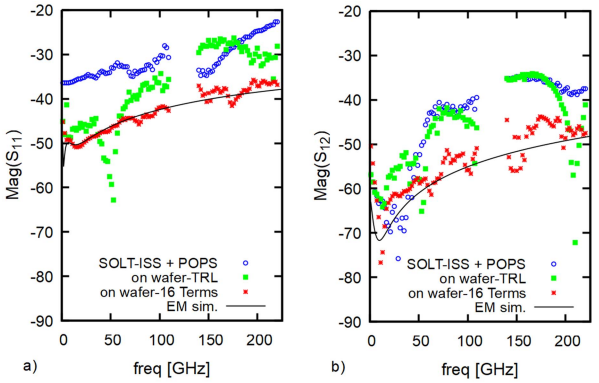

FIGURE 4. (a) Magnitude of S_{11} and (b) of S_{12} of the load-load structure versus frequency; Comparison of the different calibration method (SOLT-ISS, on wafer TRL, on wafer 16 terms, EM simulation). (6 calibration standards used for 16-terms method).

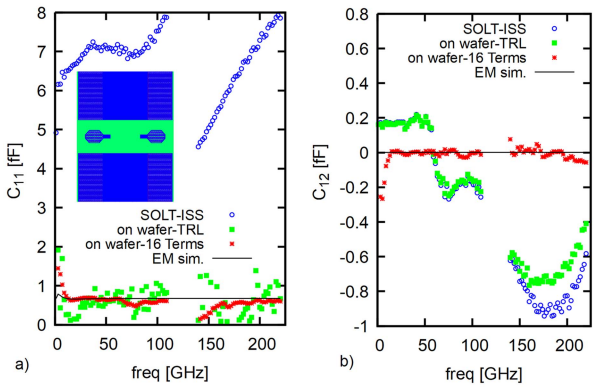

FIGURE 5. (a) C_{11} and (b) C_{12} capacitance of the pad-open structure versus frequency; Comparison of the different calibration method (SOLT-ISS, on wafer TRL, on wafer 16 terms, EM simulation).

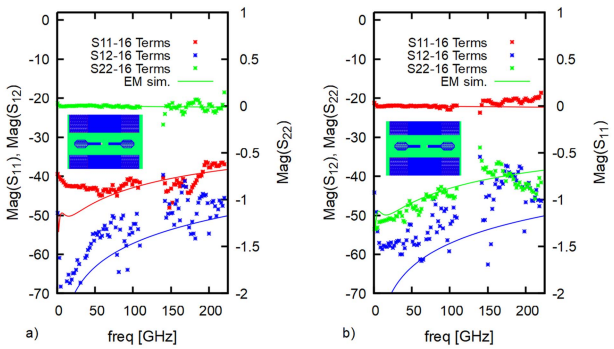

FIGURE 6. Magnitude of S parameters of the a) load-open and b) the open-load structure versus frequency.

and TRL, contrasting with the 16T, which remains consistent with EM simulation and shows no such discontinuities. In this calibration method, discontinuities are effectively mitigated.

The magnitude of S_{12} is only slightly higher than the prediction by the EM simulation. Two possible explanations arise: I) The minor imperfections in the 16 terms calibration may stem from the VNA's limited accuracy, constrained by its dynamic range. For instance, the E8361 VNA exhibits a best dynamic range of 96 dB in the 67 GHz band at maximum power, decreasing to about 69 dB at −32 dBm. Moreover, one should also consider the uncertainty sources such as instrumentation drift and probe contact repeatability. II) Another explanation could be that error terms associated with crosstalk may be subtly influenced by the intrinsic structure under measurement, as discussed in [21].

B. VERIFICATION OF CALIBRATION CONSISTENCY

The standard way to verify the consistency is to analyze standards which are not used in the calibration procedure such as the pad-open, the open-load and load-open structures.

The crosstalk capacitance of the pad-open (similar to Fig. 1(b) with access line cut at reference plane defined in Fig. 1(a)) is good indicator to analyze the crosstalk since the microstrip line is cut just after the pad minimizing the capacitance due to the 65 μm distance between each pad. The extracted capacitances obtained from the well-known π-model, $C_{11} = imag(Y_{11} + Y_{12})/(2\pi freq)$, $C_{12} = -imag(Y_{12})/(2\pi freq)$, $C_{22} = imag(Y_{22} + Y_{12})/(2\pi freq)$. are depicted on Fig. 5. Concerning C_{12} in Fig. 5(b), we notice nearly identical behavior following SOLT-ISS and TRL calibration. However, this behavior is non-physical and does not represent the inherent pad-open structure. This behavior arises from a combination of probe-to-probe coupling below 50 GHz, together with probe-to-substrate coupling above 50 GHz. Indeed, the EM simulation predicts a quasi-null C_{12} corresponding to a magnitude of S_{12} below −80 dB across the entire frequency bands. The 16-term calibration model aligns well with the EM simulation as expected.

Second, the open-load and load-open structure are calibrated using the 16-terms error model and the result is compared to the EM simulation, see Fig. 6. We can first observe that the S_{ii} parameters are well measured on the reflect side with an error of less than 0.15 dB up to 220 GHz. On the load side, the S_{ii} are lower than −35 dB and a fairly good match is observed with the EM simulation. Indeed, the noisy behavior can be attributed to the very low signal amplitude (<-65 dBm). Finally, when considering the crosstalk term S_{ij}, there is a notable correlation between measurement and EM simulation, despite the transmitted signal being very low (∼-80 dBm) which approaches the dynamic range of the VNA.

C. TRANSISTORS

For the transistor located beneath the BEOL, eliminating all BEOL-related parasitic requires employing an appropriate de-embedding procedure. In the case of on-wafer TRL and on-wafer 16-term calibration data, a transistor-short/transistor-open (TSTO) de-embedding procedure is utilized. The primary parasitic contributor, the inductive component from the access line, is initially removed. Conversely, for off-wafer SOLT-ISS calibration, where the reference line is positioned after the probe tips, the main contributor is the capacitive component consisting of the pad, access line, via descent, and

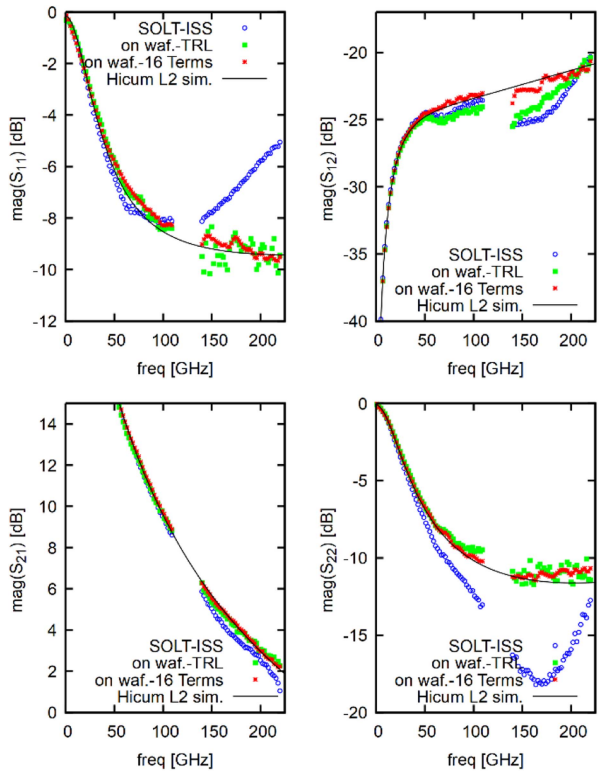

FIGURE 7. Measurement of magnitude of S parameters versus frequency of the transistor (A_E=0.09∗5 μm^2) at V_{BE}=0.9 V and V_{CB}=0V.

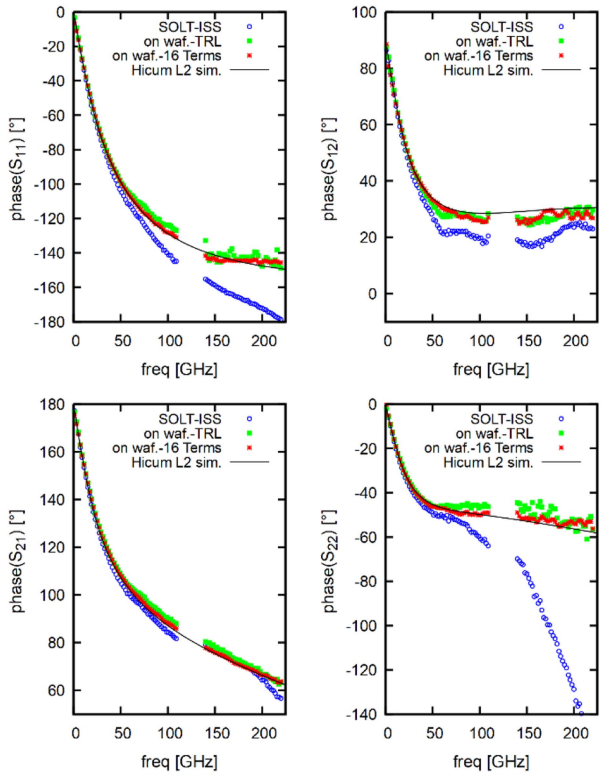

FIGURE 8. Measurement of phase of S parameters versus frequency of the transistor (A_E=0.09∗5 μm^2) at V_{BE}=0.9 V and V_{CB}=0V.

fingers. In this scenario, a transistor-open and transistor-short (TOTS) de-embedding procedure is applied. In all cases, the new reference plane is positioned at the interface between metal 1 and the contact. This de-embedding process effectively eliminates the contribution of M1 fingers as well. In Figs. 7–9, the compact model simulation data are added for comparison. These data are added as an illustrative purpose and show an expected trend of the intrinsic transistor. The transistor is biased at V_{BE}=0.9V and at V_{CB}=0V to achieve high f_T and f_{MAX}. The magnitude and phase of S-parameters are plotted on Figs. 7 and 8 comparing the three different calibration methods. Up to 40 GHz, all the three methods yield similar results, but a divergence is noticeable beyond this frequency. Among the four S-parameters, the magnitude of S_{12} curve is of particular interest since it is correlated to the crosstalk. SOLT-ISS+TO/TS and on wafer TRL+TS/TO starts to deviate at 70 GHz and a significant discontinuity is observed between the two bands corresponding to the change of probe topology.

Conversely, in the case of the 16-terms+TS/TO data, the observed trend aligns with the expectations from the compact model. Also, the continuity between the two bands is obtained confirming that the probe influence has been eliminated from the measurement. Indeed, while S_{12} is the most sensitive parameter, it is noteworthy that the 16-term method also proves valuable for accurately measuring the magnitude and, particularly, the phase of the S_{11} and S_{22} parameters. Finally, while

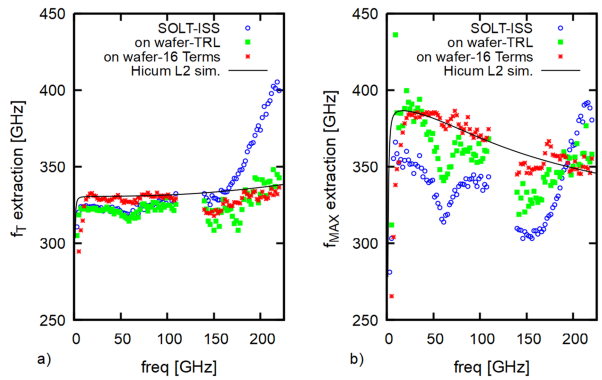

FIGURE 9. Determination of (a) f_T (defined as H21∗freq), (b) f_{MAX} (defined as $U^{1/2}$∗freq) versus frequency of the transistor (A_E=0.09∗5 μm^2) at V_{BE}=0.9 V and V_{CB}=0V.

S_{21} is the most robust parameter to measure, one can observe that when the frequency increases and the magnitude of S_{21} drops below 10 dB, the accuracy of measurement obtained from TRL and SOLT-ISS diminishes. Concerning the S_{22} parameter, it is notably affected, exhibiting significant discontinuities at 140 GHz for the SOLT-ISS in terms of magnitude. Moreover, there also is a completely incorrect trend in the upper band when considering the phase. Thus, once more, the 16-terms method demonstrates a significant enhancement in performance whereas the TRL gives acceptable results except for S_{12} parameter.

The subsequent crucial step for foundries concerns the extraction of main RF FOM, i.e., the transit frequency f_T and maximum oscillation frequency f_{MAX}. These FOMs are extracted from Fig. 9. The f_T is the most straightforward FOM to determine. Typically, this FOM is usually extracted by assuming a constant current gain (H_{21}) bandwidth product. One can observe that both SOLT-ISS and on wafer TRL yield comparable results and exhibit an unexpected trend at 60 GHz characterized by sudden drop, attributed to the probe coupling. However, with the 16-term calibration method, this trend disappears, and the extracted f_T value is about 5 to 10 GHz higher. In the second band, while the three methods are over-imposed up to 160 GHz, the SOLT-ISS method starts to diverge significantly and the resulting data can no longer be attributed solely to the intrinsic transistor.

Concerning the f_{MAX}, it can be obtained in the same way as f_T, but by considering the square root of Mason's gain instead of H_{21}. This FOM is notoriously difficult to measure [1]. When employing the conventional SOLT-ISS or the on-wafer TRL method, a similar pattern is observed which does not reflect the intrinsic transistor. Specifically, there is a sudden drop at 60 GHz, followed by a discontinuity between the frequency bands, and finally, the extracted value rises from 140 to 220 GHz. These discrepancies are attributed to uncorrected probe-to-probe and probe-to-substrate coupling and do not represent the intrinsic behavior of the transistor. However, these effects are completely corrected employing the 16-term calibration procedure.

Finally, the trend observed with the 16-term method aligns with that predicted by the compact model. The decreasing slope of f_{MAX} is notably associated with the substrate effect, which introduces a secondary pole in the power gain. This trend was similarly observed in TCAD work by [29].

VI. CONCLUSION

A methodology has been devised for establishing the on-wafer standards for the 16-term calibration procedure. This approach combines TRL calibrated data with the EM simulation to precisely generate the S parameters of the 16T standards. Careful attention has been given to the design of these on-wafer standards to maintain unchanged coupling between them. These standards have been implemented in an advanced BiCMOS 55 nm technology. The new calibration methodology provides a significant improvement starting from 40 GHz. In fact, the method significantly improves accuracy by correcting probe couplings. In particular, it eliminates discontinuities between frequency, affirming the consistency of the S-parameter measurement. Transistor measurements calibrated with the SOLT and TRL methods exhibit unexpected results on various parameters such as C_{BC}, S_{12}, S_{22}, and f_{MAX}, which cannot be solely attributed to the intrinsic transistor. The on-wafer TRL proves to be reliable for measuring certain parameters but demonstrates significant limitations when measuring FOMs which are correlated to crosstalk or return to ground. Particularly, the TRL method lacks accuracy in assessing the f_{MAX} FOM above 40 GHz despite employing state-of-the-art probes with reduced crosstalk and a diminished pitch of 50 μm in this study. Finally, the enhanced accuracy attained through the 16-term calibration method comes at the expense of additional effort compared to employing on-wafer TRL or SOLT-ISS method. The latter requires significant preparation time for EM simulations.

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