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The Impact of a Taper Impedance Transformation on the TRL De-Embedding Error

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ABSTRACT This work originates from the realization that, in a transformed impedance thru-reflect-line (TRL) calibration, the sensitivity to random measurement errors is affected by impedance discrepancies between the impedance transformer and the device-under-test (DUT). Through a thorough exploration that includes theoretical analysis, simulations and TRL measurements, this study establishes that the accuracy of de-embedding operations on a transformed impedance medium is intricately tied to the difference between the Thevenin impedance seen from the DUT-side of the launcher and the DUT impedance. A noteworthy finding is that minimizing this difference enhances the resilience of the de-embedding process against random measurement errors, being advantageous for precision modeling techniques, and demonstrating the importance of considering those concepts when designing an access structure to a DUT.

INDEX TERMS Calibration, de-embedding, measurement error, taper, TRL calibration.

I. INTRODUCTION

In the modern scheme of RF/microwave electronics, computer-aided design (CAD) techniques severely rely on accurate models, with measurements being fundamental for most modeling techniques [1], [2]. Precision in measurements translates into more accurate models and fewer design iterations. This is particularly crucial for complex components, as the RF transistor, which demands sophisticated equivalent-circuit models [3], [4], [5].

For RF measurements, a launcher is required to transport the excitation signal to the device-under-test (DUT). De-embedding these launchers from the measurements is a common practice with calibrations like thru-reflect-line (TRL) [6], [7], [8]. However, practical limitations in manufacturing standards introduce uncertainties. Printed circuits may have errors, and transitions between different transmission media may not be consistent across measurements. For example, the placement of connectors [9], [10] or RF probes [11] on the board may not be perfectly accurate [12], [13], or these transitions may vary between measurements. In either case, these imprecisions generate unexpected differences between the launchers of the various calibration standards [14], which will then translate to measurement errors [15], [16], [17], [18], [19], [20], [21].

While these errors may not be significant in many cases, they pose challenges for certain devices. For example, high-power transistors are known for being particularly difficult to measure, mostly due to the low impedances associated with them [2]. To increase the power handling of the transistor, without changing the technology, the area of the device needs to be increased by placing several small devices in parallel [22], [23]. This can lead to very wide devices and, more

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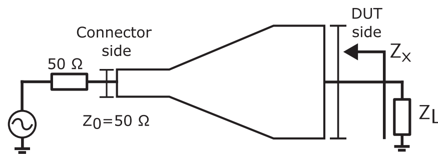

FIGURE 1. Representation of a tapered launcher used to measure a certain DUT.

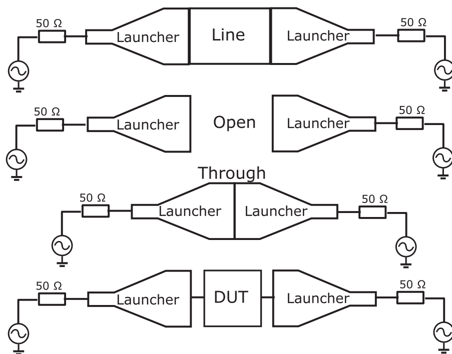

FIGURE 2. Representation of a TRL calibration kit for an arbitrary DUT-side width.

importantly, very low impedances, whose measurement can be severely influenced by uncertainties in the calibration standards, as demonstrated in the next section. Fig. 1 presents a representation of a tapered launcher commonly used to measure wide devices, as shown in [24], [25], in which the connector width must be converted into a width similar to the DUT's width, generating different characteristic impedances at each end.

The TRL algorithm, as shown in [6], [26], can effectively be used for these wide devices as long as the characteristic impedance of the line standard is known. Fig. 2 illustrates a common TRL kit configuration where a uniform transmission line with a lower characteristic impedance serves as the TRL line standard. This configuration, with a consistent tapered launcher, moves the reference plane to the middle of the through standard. The taper serves as an impedance transformer between the measurement system impedance (usually 50 Ω) and the DUT [27].

This study demonstrates that, in the presence of the described random errors, the accuracy of de-embedding the launcher hinges on the relationship between the impedances of the DUT (Z_L in Fig. 1) and the Thevenin impedance seen into the taper, from the DUT-side port, when the source port is terminated with the system reference impedance Z_s (typically 50 Ω) (Z_x in Fig. 1). Simulations and measurements on connectorized microstrip printed circuit boards (PCBs) reveal that approximating the absolute value of both impedances reduces the error sensitivity. As an example, a launcher that guarantees $Z_x = 50$ Ω was used to access two different capacitance values (1 and 10 pF), but an error was added to emulate a connector placement uncertainty. This error, whose major effect is expected to be a phase shift, was thus electrically modeled by an ideal transmission line of $Z_0 = 50.2$ Ω and delay of 0.4 ps (1.15° at 8 GHz). As illustrated in Fig. 3, a higher relative

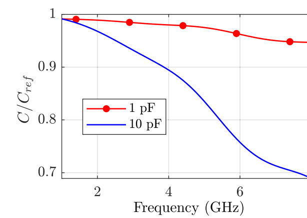

FIGURE 3. Simulation example of the relative capacitance error obtained from the de-embedding of a taper generating $Z_x \approx 50$ Ω with a small transition error.

error is observed for the larger capacitance. As we show in this paper, this measurement error difference, from the same originating imprecision, can be traced to the relationship between Z_x and Z_L. Admitting a generalized Z_x, if the reflection coefficient, $\Gamma_L = (Z_L - Z_x^*)/(Z_L + Z_x)$ is closer to zero, the measurement has lower uncertainty. However, since Z_x is typically close to real, we also show that $Z_x = |Z_L|$ is a good compromise to reduce the measurement uncertainty. The main objective of this study is to establish a theoretical framework for refining launcher design in these scenarios. Additionally, it seeks to identify unfavorable measuring scenarios, as well as to provide modeling error estimates. This information can be used to determine whether different measuring strategies should be pursued.

The main novelty behind this work lies in the development of a formal theoretical framework that delineates the relationship between the Thevenin impedance at the DUT-side and the DUT's impedance. This framework is a tool for RF engineers to predict unfavorable measurement conditions and to optimize launcher design for the DUT, without the need for time-consuming Monte-Carlo analysis [28]. While experienced RF engineers may have empirically reached similar conclusions, this study offers a systematic explanation of these phenomena and provides theoretical tools that could drive the development of innovative measurement solutions, e.g., selecting the frequency range with lower uncertainty for extracting an equivalent circuit model.

This paper is organized as follows: Section II first presents a theoretical analysis of a general de-embedding process of a tapered launcher; then, the impact of Z_x on the error sensitivity is deduced; and finally, simulation examples of measurement uncertainty for different types of DUT are shown. Section III will be dedicated to the practical validation of the developed concepts; and Section IV concludes the paper.

II. THEORY AND SIMULATION EXAMPLES

The main goal of this section is to mathematically prove that the output impedance seen from the DUT-side of the launcher will impact measurement accuracy, and, therefore, it can be optimized to decrease the sensitivity to measurement error. Besides that, this analysis can be used to predict the error sensitivity under certain conditions.

Throughout this analysis, we assume a well-understood DUT interface, treating any impact of the DUT's connection to the taper as a known and integrated part of the DUT. Additionally, a low-loss substrate for the access structure is always

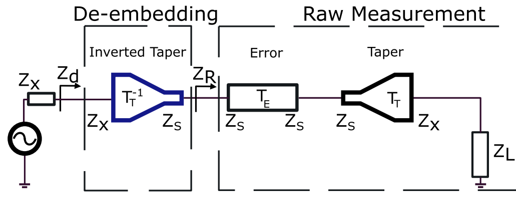

FIGURE 4. Block diagram of the conceptual de-embedding system. The raw measurement is composed of the actual one-port DUT (represented by Z_L) followed by the taper and a certain connector-side uncertainty. In this figure, the normalization impedances of the S-parameter blocks are also represented below their respective ports.

assumed, so that the characteristic impedances can always be considered real.

A. THEORETICAL ANALYSIS WITH AN IDEAL TRANSFORMER

In this subsection, we undertake a theoretical analysis focusing on the de-embedding process of an ideal taper. The concept involves a lossless ideal taper operating as an impedance transformer between two real impedances [29], [30], incorporating an electrical length (ϕ). The S-parameter matrix for this ideal taper is described as:

$$\boldsymbol{S_T} = \begin{bmatrix} 0 & e^{-j\phi} \\ e^{-j\phi} & 0 \end{bmatrix}_{Z_s, Z_x^*} \tag{1}$$

The subscript (Z_s, Z_x^*) determines the normalization impedance at port 1 (connector-side) and port 2 (DUT-side), respectively, where Z_s represents the measurement system's impedance (usually 50 Ω). The complex conjugate is denoted by the operator *. Also, as this is a representation of an ideal taper, $Z_s, Z_x \in \Re$, and $Z_x^* = Z_x$. For this reason, in this subsection, the normalization impedance will be considered to be Z_x. At this point, a few considerations should be made:

- A preliminary analysis is done considering a single one-port device, and thus only one launcher.
- The launcher will be a conceptual tapered line that converts Z_s, at the connector side, to Z_x, at the load side.
- The taper works as an impedance transformer and it is represented by (1) considering real-valued Z_s and Z_x, where ϕ stands for the electrical length of the taper.
- A conceptual error block ($\boldsymbol{T_E}$) is introduced into the theoretical model for the raw measurement of Z_L (Z_R), as depicted in Fig. 4. The taper ($\boldsymbol{T_T}$) is assumed to be extracted without error, hence $\boldsymbol{T_T^{-1}}$ is de-embedding the taper's effect to obtain the corrected Z_d.

The error impeding the exact (i.e., error-free) de-embedding of the taper from the raw measurement data is represented in Fig. 4 by an error block, $\boldsymbol{T_E}$, whose S-Parameters are:

$$\boldsymbol{S_E} = \begin{bmatrix} \delta_{S_{11}} & \sigma e^{j\theta} \\ \sigma e^{j\theta} & \delta_{S_{22}} \end{bmatrix}_{Z_s, Z_s} \tag{2}$$

This formulation assumes a small mismatch ($\delta_{S_{11}}$ and $\delta_{S_{22}}$), losses in the connector (σ) and a phase error (θ) caused by the misplacement of the connector, for example. The losses and the mismatch are expected to be very small in a well-designed measurement system. Actually, in these conditions, the phase error should also be relatively small.

Converting the S-parameter matrices of the taper and the error block to T-parameters results in:

$$\boldsymbol{T_T} = \begin{bmatrix} e^{j\phi} & 0 \\ 0 & e^{-j\phi} \end{bmatrix}_{Z_s, Z_x} \tag{3}$$

$$\boldsymbol{T_E} = \begin{bmatrix} \sigma^{-1} e^{-j\theta} & -\delta_{S_{22}} \sigma^{-1} e^{-j\theta} \\ \delta_{S_{11}} \sigma^{-1} e^{-j\theta} & e^{-j\theta} \frac{-e^{2j\theta}\sigma^2 + \delta_{S_{11}}\delta_{S_{22}}}{\sigma} \end{bmatrix}_{Z_s, Z_s} \tag{4}$$

With these T-parameters, $\boldsymbol{T_P} = \boldsymbol{T_T^{-1}} \boldsymbol{T_E} \boldsymbol{T_T}$ can be obtained, with $\boldsymbol{T_P}$ being the T-parameters after the de-embedding process. Note that $\boldsymbol{T_T^{-1}} \boldsymbol{T_E} \boldsymbol{T_T}$ is normalized to Z_x [31]. The conversion of this expression to S-parameters is expressed by:

$$\boldsymbol{S_P} = \begin{bmatrix} \delta_{S_{11}} e^{2j\phi} & \sigma e^{j\theta} \\ \sigma e^{j\theta} & \delta_{S_{22}} e^{-2j\phi} \end{bmatrix}_{Z_x, Z_x} \tag{5}$$

So, this means that the measured reflection coefficient after de-embedding can be described by:

$$\Gamma_d = \delta_{S_{11}} e^{2j\phi} + \frac{\sigma^2 e^{j2\theta} \Gamma_L}{1 - \delta_{S_{22}} e^{-2j\phi} \Gamma_L} \tag{6}$$

considering:

$$\Gamma_L = \frac{Z_L - Z_x}{Z_L + Z_x} \tag{7}$$

and

$$\Gamma_d = \frac{Z_d - Z_x}{Z_d + Z_x} \tag{8}$$

From (6) an impedance parameter error can be obtained by converting the reflection coefficient to an impedance. To simplify the equation Taylor expansions around $\delta_{S_{11}}$ and $\delta_{S_{22}}$ can be used. To further simplify the calculations, we can also consider $\sigma = e^{\alpha}$, so that $\sigma e^{j\theta} = e^{\alpha + j\theta} = e^{\gamma}$ (where γ represents the propagation constant of the error block). This step consists purely of a variable transformation to simplify the equation since σ is a real number expressing the error block losses. Note that if no error is assumed (i.e. σ equal to one, and $\delta_{S_{11}}$, $\delta_{S_{22}}$ and ϕ equal to zero) $\Gamma_d = \Gamma_L$ as expected. A more detailed demonstration of these steps can be seen in Appendix A. The final impedance error expression can be given by:

$$\begin{aligned} Z_{Err} = Z_d - Z_L &= \frac{Z_x^2 - Z_L^2}{Z_L - Z_x \coth(\gamma)} \\ &+ \frac{2e^{2j\phi} \delta_{S_{11}} (Z_L + Z_x)^2 Z_x}{(Z_L + Z_x - e^{2\gamma}(Z_L - Z_x))^2} \\ &+ e^{2\gamma} \frac{2e^{-2j\phi} \delta_{S_{22}} (Z_L - Z_x)^2 Z_x}{(Z_L + Z_x - e^{2\gamma}(Z_L - Z_x))^2} \end{aligned} \tag{9}$$

Although this error expression may seem complex to analyze, we can look into its three individual terms. The second and third terms of the expression are dependent on the mismatch of the coaxial-to-microstrip connector ($\delta_{S_{11}}$ and $\delta_{S_{22}}$). If an appropriate connector is used, the mismatch will be very small, so the impact of both terms will not be that important (for most

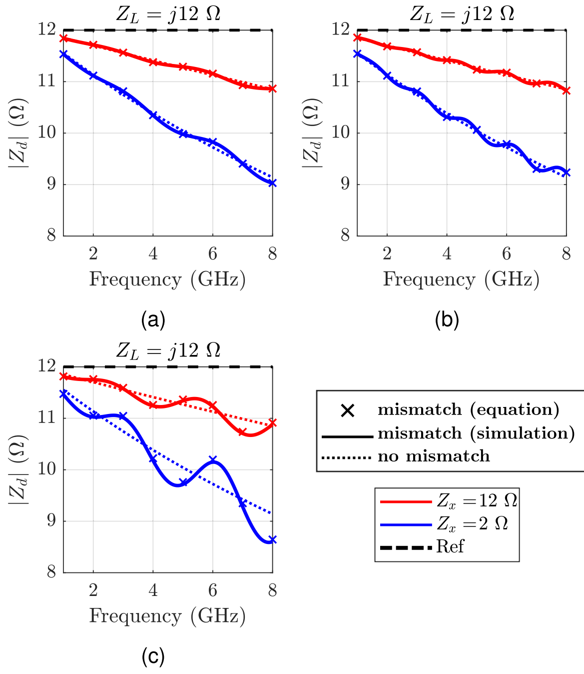

FIGURE 5. **Predicted de-embedding error comparison for a complex Z_L for mismatched and matched errors with delay error of 1 ps and: (a) $Z_0 = 53\ \Omega$ and taper delay of 158 ps; (b) $Z_0 = 53\ \Omega$ and taper delay of 316 ps; (c) $Z_0 = 65\ \Omega$ and taper delay of 158 ps.**

measurement conditions). Also, note that these terms are the only ones dependent on the taper's electrical length (ϕ). All of this means that, for most practical cases, the first term can be expected to be dominant for the overall accuracy of the measurement.

To illustrate the dominance of the first term of (9), several tests were conducted by modeling the error block as a short transmission line with a delay of 1 ps and variable Z_0. As seen in Fig. 5, the first term determines the average error of the measurement, while the other terms describe a wave-like pattern with a wavelength dependent on the length of the taper, and the amplitude determined by the mismatch ($\delta_{S_{11}}$ and $\delta_{S_{22}}$). Note that these cases represent a considerable mismatch modeled by 3 Ω and 15 Ω (i.e. $Z_0 = 53\ \Omega$ and $Z_0 = 65\ \Omega$, respectively). Also, in most cases, the losses in the transitions are low enough to be considered negligible. This was verified in the measurement system used in the practical validation of this work. These findings suggest that the phase error, represented by the first term of (9), is likely to have a greater influence compared to other error terms. Although the mismatch error typically has a minor impact, it can cause deviations that exhibit a wave-like pattern. However, these deviations may be mitigated to a large extent by calculating an average. In contrast, phase errors are more challenging to eliminate effectively.

This suggests that, for simplicity in the analysis, it is reasonable to consider a matched lossless line as the error block. In this condition, $\delta_{S11} = \delta_{S22} = 0$ and $\gamma = j\theta$, so that $\coth(j\theta) = -j\cot(\theta)$. Thus, (9) can be simplified into:

$$Z_{Err} = Z_d - Z_L = \frac{Z_x^2 - Z_L^2}{jZ_x \cot(\theta) + Z_L} \tag{10}$$

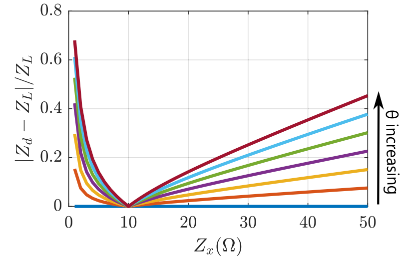

FIGURE 6. **De-embedding error at 10 GHz, considering 0 ps to 1.5 ps error delays, for $Z_L = 10\ \Omega$.**

The admittance error, (11), can be deduced to be:

$$Y_{Err} = Y_d - Y_L = \frac{Y_x^2 - Y_L^2}{jY_x \cot(\theta) + Y_L} \tag{11}$$

where, similarly to the previous case, Y_d and Y_L are the de-embedded and the DUT admittances, respectively, and Y_x is the inverse of Z_x.

B. ILLUSTRATIVE SIMULATIONS

By analyzing (10), it is possible to determine how the measured impedance error behaves in different scenarios. It can be verified that the error expression is affected by three variables: the load impedance (Z_L); the phase error of the measurement (θ); and the output impedance of the taper at the DUT-side (Z_x). For an ideal taper built on a low-loss substrate, Z_x can be considered real, as $Z_x = Z_{0_{DUTside}}$.

An interesting realization is that, by optimizing Z_x, the measurement error can be minimized. A general minima for the expression is not trivial, but we can analyze the error behavior for different types of measurement loads, and deduce a reasonable solution from there.

1) RESISTIVE LOADS

In scenarios where the load (Z_L) is purely real, the analysis of de-embedding errors becomes relatively straightforward. The unique condition for a zero error occurs when Z_x equals Z_L. This condition highlights an interesting case where the error is minimized, and the remaining mismatch-related error dominates, creating an oscillation around the actual load.

To exemplify this analysis for more complex cases, we explore the absolute error $|Z_{Err}| = |Z_d - Z_L|$. This approach allows us to assess the error variation with Z_x and identify a reasonable approximation to the minimum error. For real loads, the minimum absolute error, $\min(|Z_{Err}(Z_x)|)$, can be easily calculated and it is obtained for:

$$Z_x = Z_L,\ if\ Z_L \in \Re > 0 \tag{12}$$

In Fig. 6, we observe the evolution of the error across different Z_x values while maintaining a fixed $Z_L = 10\ \Omega$. The analysis also considers varying delay values θ in the range of 0 ps to 1.5 ps, corresponding to lengths from 0 mm to 0.3 mm for a substrate with $\varepsilon_R = 2.2$. The frequency of interest is set at 10 GHz.

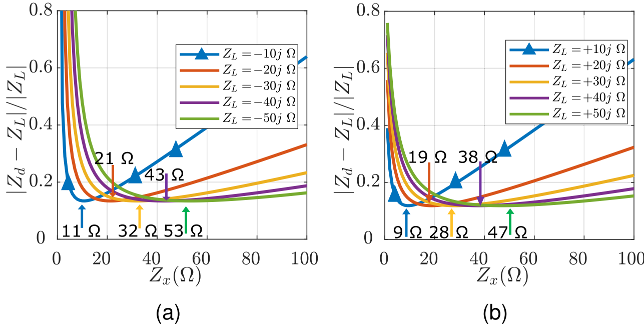

FIGURE 7. De-embedding error at 10 GHz, considering 1 ps error delay, for multiple imaginary loads: (a) Capacitive; (b) Inductive. The arrows indicate for which Z_x the minimum error occurs.

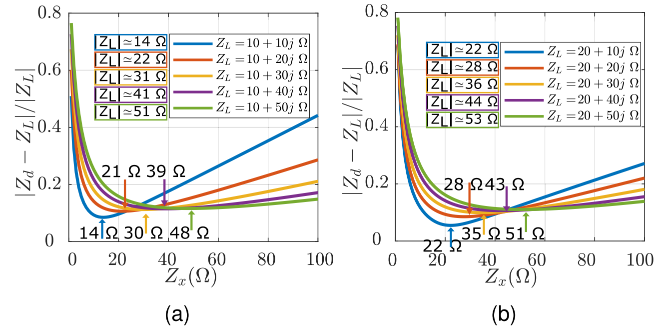

FIGURE 9. De-embedding error at 10 GHz, considering 1 ps error delay, for multiple complex loads: (a) Capacitive; (b) Inductive. The arrows indicate for which Z_x the minimum error occurs.

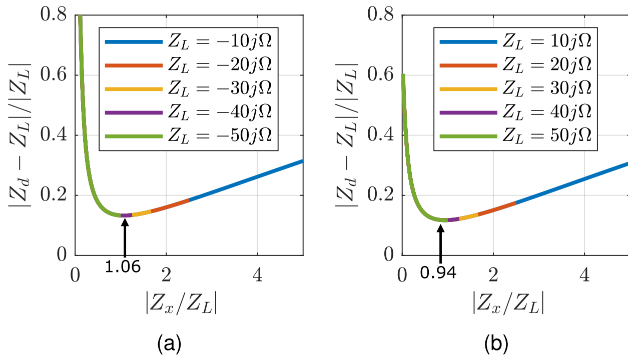

FIGURE 8. De-embedding error at 10 GHz, considering 1 ps error delay, for multiple imaginary loads: (a) Capacitive; (b) Inductive. Note that, in this plot, the abscissas are normalized to Z_L.

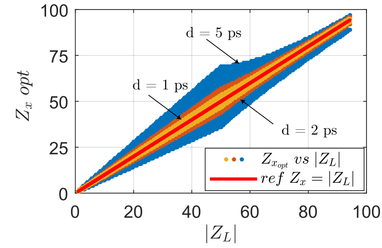

FIGURE 10. Optimal Z_x vs $|Z_L|$ ranging $\Re(Z_L) = [0:70]\ \Omega$ and $\Im(Z_L) = [-50:50]\ \Omega$ and with a $d = 5$ ps (blue), $d = 2$ ps (orange) and $d = 1$ ps (yellow) error lines.

2) PURELY IMAGINARY LOADS

For purely imaginary loads, two minimum values can be obtained for $|Z_{Err}(Z_x)|$ for:

$$Z_x = -\Im(Z_L)\frac{\sin(\theta) - 1}{\cos(\theta)} \tag{13}$$

$$Z_x = -\Im(Z_L)\frac{\sin(\theta) + 1}{\cos(\theta)} \tag{14}$$

where $\Im()$ represents the imaginary part of its argument.

Although there are two solutions to the equation, for a certain imaginary load, only one solution is valid:

- for capacitive loads, $\Im(Z_L) < 0$, (13) leads to positive Z_x;
- for inductive loads, $\Im(Z_L) > 0$, (14) leads to positive Z_x.

For small θ, a good rule-of-thumb solution is $Z_x = |Z_L|$. This can be seen in Fig. 7, where in all cases the minima are always close to $|Z_L|$. This rule-of-thumb becomes even more evident if we normalize the xx axis to Z_L, obtaining Fig. 8 by using the same data as Fig. 7.

These examples demonstrate that the error is also minimized similarly to the real Z_L case. However, a key distinction is that the error minima is not zero for purely imaginary loads. Also, by looking at the triangle-marked lines of Fig. 7, it is noticeable that to measure low impedances, the optimal realizable Z_x range becomes very narrow. This highlights the critical relevance of these findings in scenarios involving low-impedance measurements.

3) COMPLEX LOADS

The minimum of the error expression for complex loads, could not be analytically determined. So, a numerical approach was taken.

Fig. 9 depicts the relative error for various Z_x values with selected complex loads, emphasizing that the error minimum occurs around $Z_x \sim |Z_L|$. This rule-of-thumb solution is further validated by Fig. 10, where different colored dots represent optimal Z_x values for various error delays. While extremely high error delays (as in the blue dots) may deviate from the rule, practical scenarios with reasonable error levels consistently demonstrate that the error is minimized close to $Z_x = |Z_L|$ (indicated by the red line). Note that $d = 5$ ps corresponds to around 1 mm in an $\varepsilon_R = 2.2$ substrate.

C. NON-IDEAL IMPEDANCE TRANSFORMER

In practical scenarios, the assumption of an ideal impedance transformer may not hold true. In theory, physically longer tapers will perform a better impedance conversion. However, in practice the taper's physical length is limited, leading to small electrical lengths, particularly at lower frequencies [29]. So, we consider the taper to be imperfect if it is not sufficiently long to achieve the ideal impedance transformation. In these cases, Z_x may be a complex impedance, even for a lossless taper.

To represent the non-ideal lossless taper transformer with a limited physical length (1) can be used, considering now a complex-valued Z_x. However, the demonstration in Section II-A exclusively addresses a real-valued Z_x, whereas, for a short taper, it is imperative to account for the distinction between Z_x and Z_x^*. This definition ensures that the DUT-side port is normalized to the complex conjugate of Z_x and produces an anti-diagonal matrix. A detailed explanation for this description of the short taper is found in Appendix B.

This distinction could introduce a challenge in cascading power-wave S-parameters directly when their reference impedance is not real [32], [33]. Fortunately, the complexity is localized to the interface between the taper and the load (Z_L). So, it remains feasible to cascade the matrices using $\boldsymbol{T_P} = \boldsymbol{T_T}^{-1}\boldsymbol{T_E}\boldsymbol{T_T}$.

However, caution is required when evaluating the resulting S-parameter matrix $\boldsymbol{S_P}$. The inversion of $\boldsymbol{T_T}$ into $\boldsymbol{T_T}^{-1}$ leads to the normalization of the first terminal to Z_x. Consequently, $\boldsymbol{S_P}$, as defined previously by (5), is normalized to (Z_x, Z_x^*). As a result, the de-embedded reflection coefficient is expressed as follows:

$$\Gamma_d|_{Z_x} = S_{p_{11}} + \frac{S_{p_{21}}S_{p_{12}}\Gamma_L|_{Z_x}}{1 - S_{p_{22}}\Gamma_L|_{Z_x}} \tag{15}$$

where both Γ_d and Γ_L are referenced to Z_x, demonstrated in the equation by the notation $|_{Z_x}$. In the case of a simple phase error, the error expression is modified:

$$Z_{Err} = Z_d - Z_L = \frac{|Z_x|^2 - Z_L^2 - 2jZ_L\Im(Z_x)}{Z_L + j[\Re(Z_x)\cot(\theta) + \Im(Z_x)]} \tag{16}$$

Note that $\Re$ and $\Im$, respectively represent the real and imaginary parts of their argument.

It is noteworthy that the error is zero if $Z_L = Z_x^*$. While conceptually there could be a Z_x that creates zero error, in practical scenarios, Z_x is expected to take a limited range of values. The analysis is restricted to a taper transformer, considering a Z_x within a certain VSWR normalized to Z_0 at the DUT-side. Results of Fig. 11 are presented for an imperfect taper that induces a Z_x varying impedance as shown in Fig. 11(c) . The plots illustrate the de-embedding error comparison for a complex Z_L under simulated mismatched and matched errors with a delay error of 1 ps, mismatch modeled by 5 Ω, and taper delay of 474 ps. An important note is that, in these plots, the mismatched results were obtained from simulations, while the matched ones were obtained by (16). The results affirm that the analysis is robust, providing insights even in non-ideal conditions, as they align with previous observations.

D. TRL CALIBRATIONS

This subsection employs simulated TRL kits to de-embed both single-port and dual-port devices. Also, a more realistic and elaborated error will be considered to verify the validity of the previous simplifications.

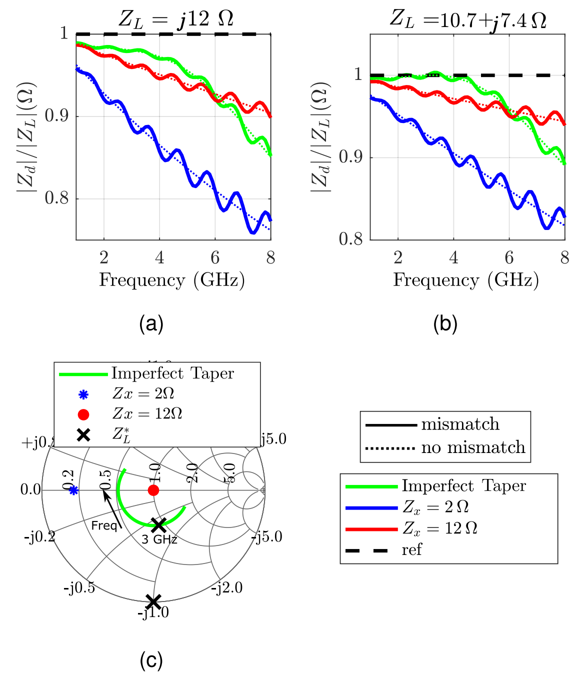

FIGURE 11. Predicted de-embedding error comparison for a complex Z_L for mismatched and matched errors with delay error of 1 ps, mismatch of 5Ω and taper delay of 474 ps: (a) $Z_L = j12\ \Omega$; (b) $Z_L = 10.7 + j7.4\ \Omega$. In (c) the evaluated Z_x and complex conjugate of Z_L are displayed with a reference impedance of 12 Ω. The previously ideal tapers were also added for comparison with the imperfect taper.

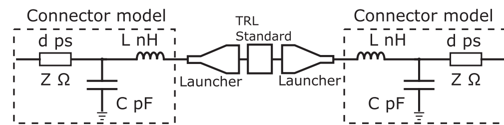

FIGURE 12. Diagram of the error model added to each TRL standard.

1) REALISTIC SIMULATION SET-UP

The methodology consists of employing two TRL kits on an electromagnetic (EM) simulator (we used Keysight ADS's Momentum), composed of the through, open and two lines (5.5 mm and 14 mm) standards, as in Fig. 2. The kits were designed using the same substrate (Rogers 4350b with 0.508 mm thickness). The difference between them is the approximate Z_x : 50 Ω and 12 Ω; both kits present $Z_0 = 50$ Ω at the connector side. For simplicity, they are referred to as 50 Ω and 12 Ω kits throughout this work.

To generate the measurement error due to the lack of connector repeatability between measurements, the circuit shown in Fig. 12 is added to each port of each standard. This circuit is built by an LC circuit to represent the coaxial-to-microstrip transition and a transmission line to represent the added electrical length. In the following tests, slightly different parameters for that circuit are used for each standard and DUT to represent the error added to each measured board.

To recreate a realistic variation of these parameters, a 50 Ω TRL kit similar to the one in Fig. 2 was measured

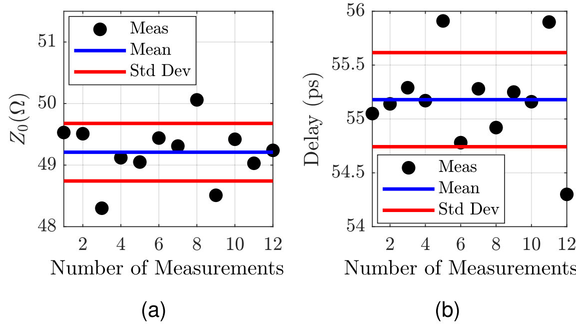

FIGURE 13. Extracted parameters for the connector error model obtained from measurements: (a) Characteristic Impedance; (b) Delay.

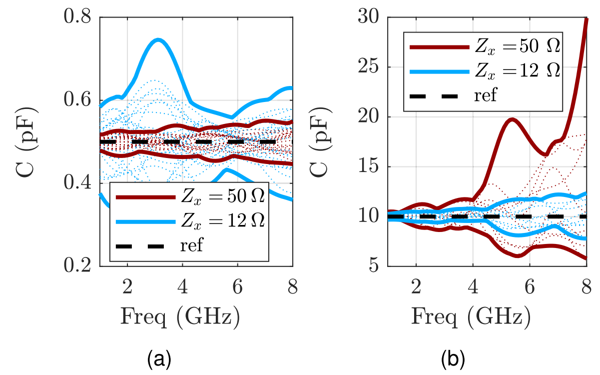

FIGURE 14. Simulation results for two different TRL kits subjected to the same error model and used to measure two capacitances: (a) 0.5 pF; (b) 10 pF.

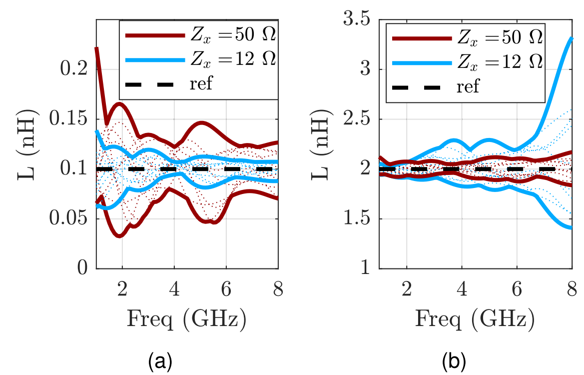

FIGURE 15. Simulation results for two different TRL kits subjected to the same error model and used to measure two inductances: (a) 0.1 nH; (b) 2 nH.

twice with removable coaxial-to-microstrip connectors. After applying a SOLT calibration to set the reference plane at the coaxial cable to connector interface, it is possible to compare the S-parameters of the EM simulations without connectors to the measurements (which include the connectors). From this comparison, the parameter sets of 12 connector models were extracted via equivalent-circuit optimization. For this optimization, the adopted connector model topology is the one shown in Fig. 12. The optimization target is the mean squared error (MSE) in the S-Parameters. After optimization, the achieved MSE level is lower than −30 dB, showing that the selected model is sufficient to account for the connector transition within the measurement range. The extracted parameters were not used for the calibrations in this subsection. Instead, they were used to obtain average and variance values to produce a realistic range for the Monte-Carlo tests. In this procedure, the average values were: $\mu_C = 0.08$ pF, $\mu_L = 0.14$ nH, $\mu_Z = 49.2\ \Omega$, and $\mu_d = 54.9$ ps. The error was introduced by varying the Z_0 and d of each transmission line following a normal distribution with the standard deviations $\sigma_Z = 0.47\ \Omega$, $\sigma_d = 0.43$ ps, as demonstrated in Fig. 13.

2) TRL CALIBRATION OF SINGLE-PORT DEVICES

With the previously extracted variance for the connector model parameters, a Monte Carlo simulation was performed for the process of accessing the DUT through a TRL calibration. This Monte-Carlo Simulation was applied to access different known DUTs. The calibration procedure is iterated 10 times, generating 10 TRL kits with different parameter values following a normal distribution with the presented standard deviations and S-parameters for all TRL standards. To ensure a fair comparison between the 12 Ω and the 50 Ω kits, the error box is exactly the same for both in each iteration.

By following this methodology, 10 sets of S-parameters for the input and output launchers are obtained. These can be used to de-embed known DUTs embedded with error-less launchers. If Z_x played no role in the accuracy of the measurements, the error in the de-embedded device would be consistent for both kits.

Fig. 14 displays the de-embedded results when two capacitance values (0.5 pF and 10 pF) are to be measured. The dotted lines represent the 10 iterations, while the full lines depict their envelope (maximum error). Despite having the exact same connector variation in all iterations, the extracted capacitances are different. These values were calculated from the de-embedded Y-parameters as follows:

$$C = \Re\left\{\frac{Y_d}{j\omega}\right\} \tag{17}$$

For the smaller capacitance, the 50 Ω kit is less sensitive to errors, as the DUT's impedance is higher. For the 10 pF capacitance the reverse occurs. Similar observations can be made using ideal inductors as DUTs (0.1 nH and 2 nH). Fig. 15 demonstrates that the 50 Ω kit benefits the extraction of the larger inductance due to its larger impedance, while the 12 Ω kit benefits the smaller inductance. The inductance values were obtained by:

$$L = \Re\left\{\frac{1}{j\omega Y_d}\right\} \tag{18}$$

These results demonstrate the influence of Z_x on the sensitivity of the error in a TRL calibration. Performing the same procedure 1000 times allows the estimation of the probability

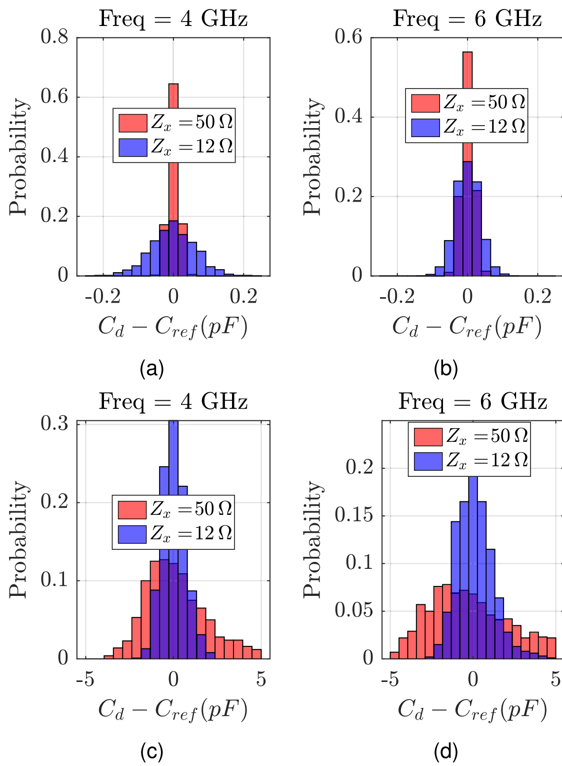

FIGURE 16. Probability distribution functions for the error of 1000 de-embedded capacitances for a certain frequency: (a) C = 0.5 pF at 4 GHz; (b) C = 0.5 pF at 6 GHz; (c) C = 10 pF at 4 GHz; (d) C = 10 pF at 6 GHz.

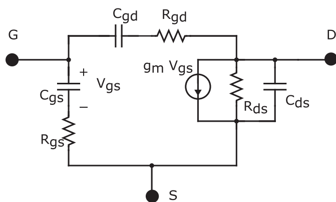

FIGURE 17. Circuit schematic of the intrinsic model of a transistor.

distribution for each capacitance value. Fig. 16 shows consistent average values with the DUT, while the standard deviation varies significantly, depending on the frequency and the Z_x generated by the launcher.

3) TRL CALIBRATION OF A TRANSISTOR

The previously described kits are now employed for de-embedding simplified small-signal transistor models, offering insight into the implications of the presented concepts in a proper TRL calibration with a 2-port DUT. While the earlier theory was developed for a single-port measurement, a parallel analysis is conducted for a two-port measurement. The relation of Z_x to the Z-parameters of the DUT is shown to have a similar form as in the single-port case, as demonstrated in Appendix C.

A common topology for the intrinsic structure of the transistor is depicted in Fig. 17. In this subsection, two biases are

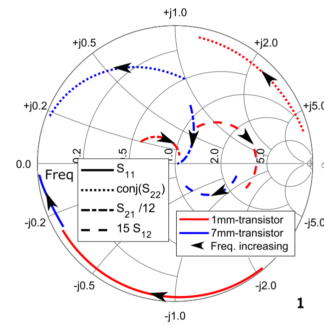

FIGURE 18. Simulated intrinsic S_{11}, S_{21}, S_{12} and complex conjugate of S_{22} parameters for a 1mm-wide transistor and a 7mm-wide transistor in a $[V_{gs} = V_t; V_{ds} = V_{DD}]$ bias and measured from 1 to 8 GHz.

considered: $[V_{gs} = -5\,V; V_{ds} = 0\,V]$; and $[V_{gs} = V_t; V_{ds} = V_{DD}$ (within the saturation region)]; with $V_t = -3\,V$, assuming a normally-on device (for instance, a GaN HEMT). The objective is to extract three sets of capacitances (C_{gs}, C_{ds}, C_{gd}) for each bias following the equations [34] below:

$$C_{gs} = \frac{1}{\omega \Im\{\frac{1}{Y_{d_{11}} + Y_{d_{12}}}\}} \tag{19a}$$

$$C_{gd} = \frac{1}{\omega \Im\{\frac{1}{Y_{d_{12}}}\}} \tag{19b}$$

$$C_{ds} = \frac{\Im\{Y_{d_{12}} + Y_{d_{22}}\}}{\omega} \tag{19c}$$

In realistic scenarios, extrinsic elements such as manifolds and packaging elements would be expected, but they only cause impedance transformations to the DUT. To streamline the analysis, we simplify it by considering only the intrinsic elements of the device. A scalable intrinsic model is employed, allowing adjustment of its parameters to fit a certain physical size. The devices are conceptualized as composed of unit-cells with two 0.325 mm-wide gate fingers. The medium-power device comprises 8 unit-cells, while the high-power device consists of 53. Moving forward, we refer to the devices by their pad widths: 1 mm for the medium-power and 7 mm for the high-power devices. Fig. 18 presents the S-parameters for both transistors, where the S_{22} of the devices is represented by its complex conjugate in the Smith chart. It is noteworthy that the larger transistor naturally exhibits lower impedances.

Fig. 19 reveals a significant impact, with considerable frequency-dependent variations of the capacitance values. As in the previous cases, despite having the same connector error applied to both sets of simulations, its effects are more pronounced in the larger transistor (the one with the lowest impedances).

To validate the previously described relation between the measured impedance and Z_x, a kit resembling the previous 7 mm design but utilizing a thinner substrate (Rogers 4350b, 0.101 mm) is designed. This maintains launcher geometry while decreasing Z_x to around 2 Ω. Fig. 20 demonstrates that

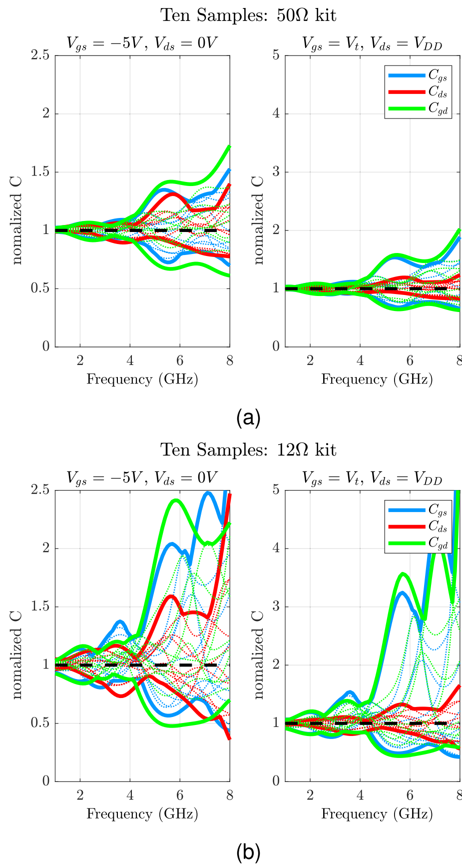

FIGURE 19. Simulation results of the extraction of the capacitances of small-signal models of transistors: (a) 1 mm-wide transistor with a 50 Ω TRL kit; (b) 7 mm-wide transistor with a 12 Ω TRL kit.

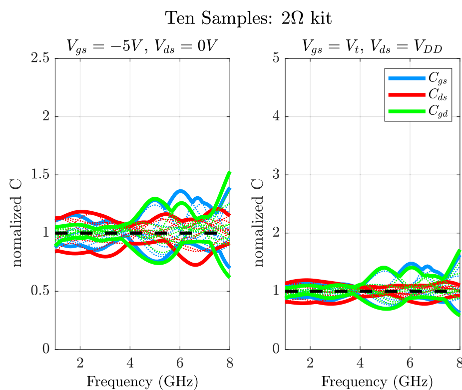

FIGURE 20. Simulation results of the extraction of the capacitances of small-signal model for a 7 mm-wide transistor, but now with a 2 Ω TRL kit. Please note the lower error now obtained when compared to the results of Fig. 19(b), in which the same DUT was used.

the measurement with the 2 Ω kit is less sensitive to error, underscoring the substantial impact of the explored concepts on the measurement of complex devices, such as transistors.

In certain scenarios, the proposed theory can provide guidance on determining the optimal Z_x that minimizes overall error within a specific bandwidth, assuming the RF engineer possesses an approximation of the variation of Z_L. Rather than optimizing Z_x for a particular frequency, it could be adjusted to ensure that error remains reasonable across the bandwidth of interest. However, we should acknowledge that some situations can occur where the optimal Z_x is not practical (limitations caused by the DUT's geometry and dynamic nature, for example). In those cases, the effectiveness of this solution could, in fact, be less pronounced. However, the theoretical analysis presented throughout this Section can help the RF engineer predict those cases and take other additional actions to prevent excessive measurement error, e.g. taking an average of multiple DUT measurements to reduce random errors. This formalism can also help in modeling problems of measured devices: examining uncertainty predictions across frequency helps prioritize measurements in low-uncertainty regions, enhancing the accuracy of the extraction process.

Besides these considerations, this work could also motivate a deeper look into a two-port DUT with different impedances at each port. This investigation could involve assessing the potential benefits of designing a DUT board with distinct launchers at each port, optimized for their respective Z_L values. One possible approach is to use two separate TRL kits, with each kit acquiring the error box for a different port of the DUT board, as demonstrated in [35].

Our analysis shows the benefits of designing the launchers to match Z_x to a complex Z_L by optimizing their width and length or even designing a matching network. However, this optimization can be challenging, so we generally recommend using real-valued tapers for consistency in the measurements. Longer tapers are beneficial to ensure stable impedance transformation at lower frequencies, but the trade-off between losses and matching should also be considered.

III. EXPERIMENTAL VALIDATION

For practical validation, two TRL kits intended to present different Z_x values were built to measure known EM structures (i.e., known impedance profiles).

A. BUILDING THE TRL KITS

The kits were built, aiming for distinct characteristic impedances (and, by consequence, presented Z_x) to analyze their sensitivity to the lack of connector repeatability. The kits used different substrate thicknesses to help achieve different Z_x without recurring to overly problematic widths. The chosen compromise balanced a significant Z_x difference with minimal impact from DUT-to-taper transitions, assessed through electromagnetic simulations.

The launchers consisted of a 7 mm taper with a 0.508 mm substrate for $Z_x = 12\ \Omega$, using a Klopfenstein taper [36], and a 1.4 mm taper with a 0.762 mm substrate for $Z_x = 54\ \Omega$, utilizing a shorter linear taper. Fig. 21 illustrates the launchers, and Fig. 22 shows the measured S_{22} normalized to the expected Z_x. Each TRL kit includes an open circuit, two lines (14 mm and 5.5 mm), and a zero-length through. The layouts used in the measurements are depicted in Fig. 23. A picture of the fabricated TRL kits can be seen in Fig. 24. For both kits, the

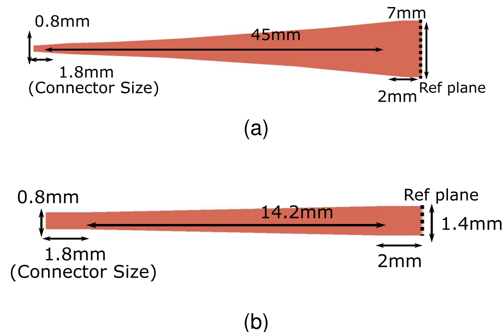

FIGURE 21. Launchers used in the practical measurements: (a) 12 Ω kit; (b) 54 Ω kit.

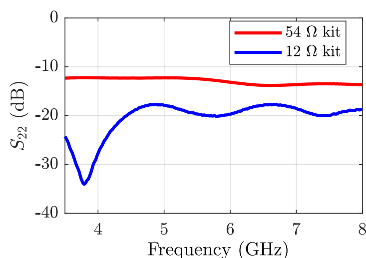

FIGURE 22. Measured S_{22} of the fabricated connectorized TRL launchers normalized to their respective projected impedance, Z_x.

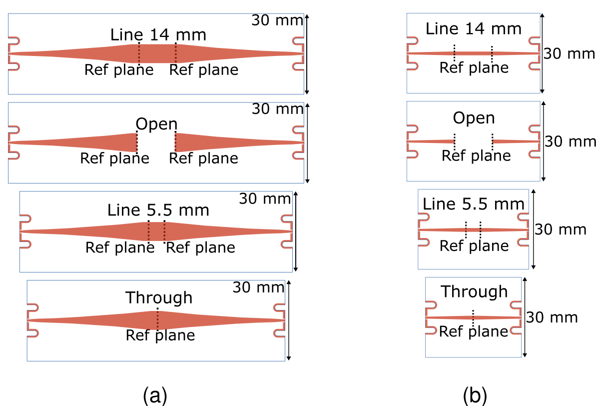

FIGURE 23. Layouts of the measured TRL kits: (a) 12 Ω kit; (b) 54 Ω kit.

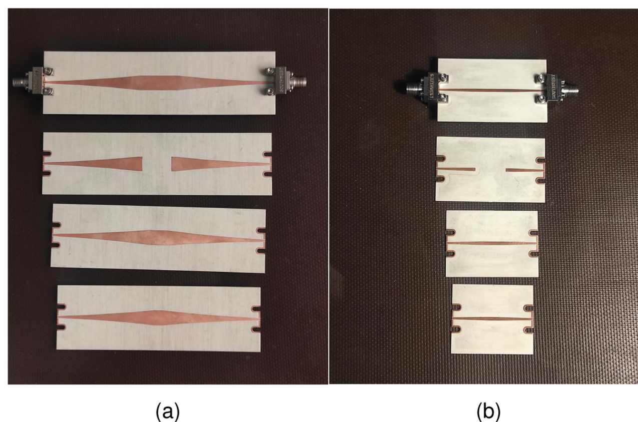

FIGURE 24. Picture of the fabricated TRL kits: (a) 12 Ω kit; (b) 54 Ω kit.

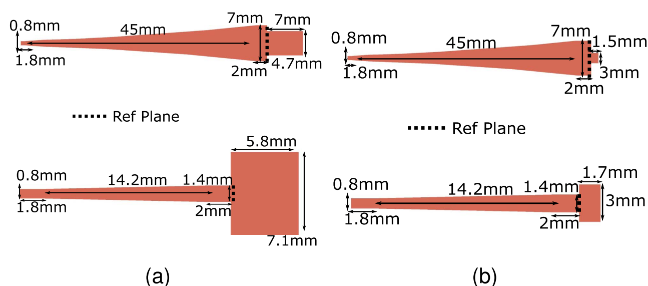

FIGURE 25. DUTs used in the practical measurements and their respective launchers: (a) low impedance stubs; (b) high impedance stubs.

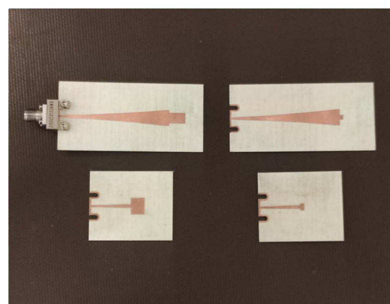

FIGURE 26. Picture of the fabricated DUT boards.

reference impedance of the TRL was estimated through simulations and measurements to guarantee a proper impedance conversion to 50 Ω.

B. BUILDING THE DUTS

To ensure a known DUT, simple structures were built using microstrip lines. The simplicity of these structures facilitates the usage of EM simulations to ascertain the added parasitic effects introduced by the discontinuity in the reference plane. Although these effects are not calibrated by the TRL method, they can be removed via EM simulation, also using Keysight's ADS. The applied procedure is described in Appendix D. The measurements compared in the following include the de-embedding of the step transition. So, in this study, the DUTs consist of open-ended stubs designed to maintain the same load impedance (Z_L) for both launchers across a wide frequency band.

Two sets of stubs were created to highlight the differences between the TRL kits: a low-impedance stub for the 12 Ω kit and a high-impedance stub for the 54 Ω kit. The stubs depicted in Fig. 25 were designed with the same characteristic impedance (Z_0): 17 Ω for the low-impedance stubs and 33 Ω for the high-impedance stubs. A picture of the produced DUT boards is shown in Fig. 26. Fig. 27 shows the reflection coefficients of these stubs, simulated from 3.5 GHz to 8 GHz (Smith chart normalized to 50 Ω).

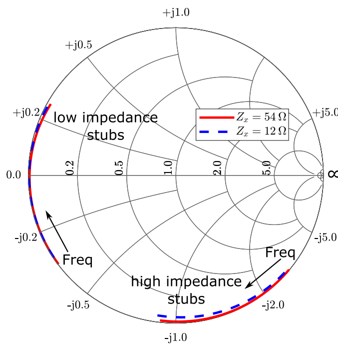

FIGURE 27. Reflection coefficients of the designed stubs simulated from 3.5 GHz to 8 GHz (Smith chart normalized to 50 Ω).

TABLE 1. Reference Delays of the Measured Stubs

	$Z_x = 54\ \Omega$	$Z_x = 12\ \Omega$
low Z_L	38 ps	44 ps
high Z_L	12 ps	10 ps

C. MEASURING THE DUTS

Each DUT was measured 10 times using its respective TRL kit, and the impedance results can be seen in Fig. 28. Additionally, 2000 iterations of the expected results using the developed error model were performed, to extract the error boundary, and demonstrate that the measured error falls within the predictions made during this work. As predicted, the measurement error is lower if Z_x is closer to $|Z_L|$.

To better visualize the impact of these measurement errors when extracting certain properties of a DUT, we determined the phase delay from the measured impedances. For an open-ended stub, Z_L is given by:

$$Z_L = Z_0 \coth(\gamma_{stub} L) \tag{20}$$

With Z_0 being the characteristic impedance of the stub, L its length, and γ_{stub} the propagation constant, which can be described by $\gamma_{stub} = \alpha_{stub} + j\beta_{stub}$ (i.e. the sum of the attenuation constant and the phase constant).

As Z_0 is known, obtaining $\gamma_{stub} L$ is a straightforward process. However, we must also consider the impact of the transition between the launchers and the stubs, as they have different line widths. For this, as previously stated, EM simulations were used to de-embed the impact of this transition.

Following this procedure, and considering that, for these stubs, the attenuation constant is very small, we can calculate the delay as $d = \beta_{stub} L/\omega$. Expected delays for the stubs are presented in Table 1.

The calculated delay can be subtracted from the reference one, resulting in the plots seen in Fig. 29. We can see that Fig. 29(a) clearly demonstrates that the 12 Ω kit is better suited to measure the low impedance stub, while in Fig. 29(b) the reverse is true. The results align with the conclusions drawn from the theoretical development: the accuracy of the measurement improves when Z_x is closer to $|Z_L|$.

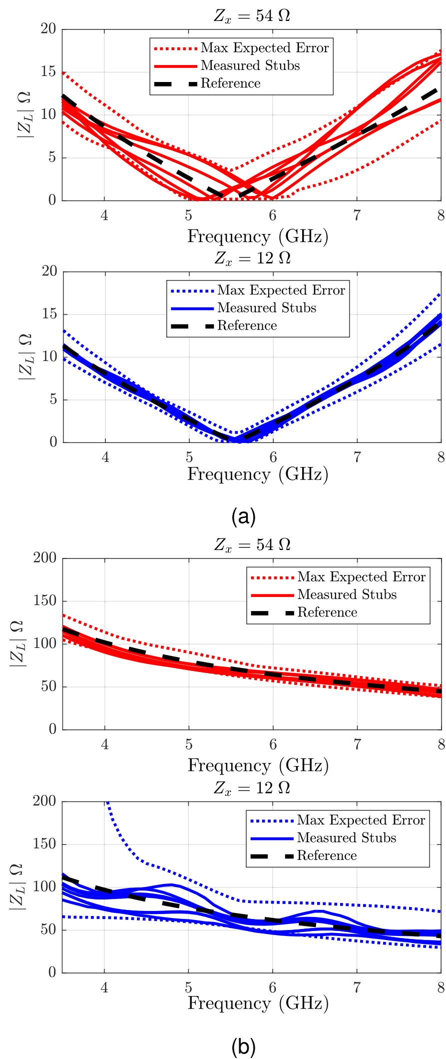

FIGURE 28. Measured impedances of the: (a) low impedance stubs; (b) high impedance stubs; at the TRL reference plane.

These results demonstrate that the kits indeed produce different outcomes consistent with our predictions. More importantly, measurement errors significantly impact the extraction of the DUT properties, which can hinder the modeling process.

IV. CONCLUSION

This work demonstrated the impact of the output impedance seen from the DUT-side of the launchers in TRL calibrations on the calibrated result sensitivity to random measurement errors. Utilizing theory, simulations, and measurements, this work illustrates that refining the launcher impedance to closely match the absolute value of the DUT impedance enhances the quality of TRL calibrations.

Additionally, a theoretical model is introduced to anticipate the impact of connector errors in such measurements. The approach presented here offers a systematic way to analyze and attempt to mitigate the impact of measurement errors, being

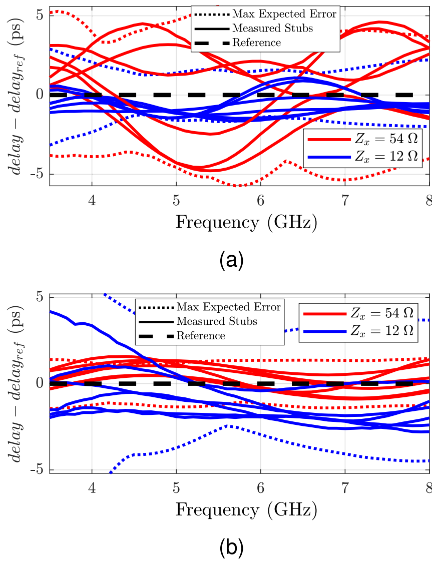

FIGURE 29. Delay error of the measured stubs and their expected error for: (a) low impedance stubs; (b) high impedance stubs.

particularly interesting for devices with very low or very high impedances, as calibration kits are not generally developed for these extreme cases. Although this work demonstrates the utility of these concepts, in some practical cases, either due to a wide frequency-dependent variation of the DUT's impedance or due to physical constraints set by the DUT, an optimal launcher may not be feasible. Nonetheless, in those cases, this theoretical formalism still serves as a guide to partially minimize this problem or to take a different approach to help improve the quality of the measurements (e.g. the use of more stable transitions or multiple measurements of the same DUT) or to prioritize frequency regions with less uncertainty in the modeling of measured components.

Another limitation of the present work is related to the measurement of two-port devices. While briefly explored in Section II-D-3, the theoretical principles governing these measurements align with those of single-port cases. However, there remains potential for further development and exploration in future studies. A common challenge arises when the impedance of the DUT differs between its two ports. In such cases, the creation of a de-embedding technique tailored for different launchers could present an intriguing approach worth pursuing.

APPENDIX A
IMPEDANCE ERROR DEMONSTRATION

This appendix demonstrates the derivation of (9) from (6). The first step is to consider (8). Then, combining with (6), we get:

$$Z_d = Z_x \frac{1 + \delta_{S_{11}} e^{2j\phi} + \frac{e^{2\gamma}\Gamma_L}{1-\delta_{S_{22}} e^{-2j\phi}\Gamma_L}}{1 - \delta_{S_{11}} e^{2j\phi} - \frac{e^{2\gamma}\Gamma_L}{1-\delta_{S_{22}} e^{-2j\phi}\Gamma_L}} \tag{21}$$

This expression is too complicated to effectively develop into an impedance error that can be easily analyzed. To simplify this expression, a first-order Taylor expansion is performed, assuming small mismatches, $\delta_{S_{11}}$ and $\delta_{S_{22}}$ (a reasonable assumption in a well-designed measurement system). This results in (22), which divides the expression into three terms: one dependent on neither values; another only dependent on $\delta_{S_{11}}$; and a third one only dependent on $\delta_{S_{22}}$.

$$Z_d = Z_x \left(\frac{1 + e^{2\gamma}\Gamma_L}{1 - e^{2\gamma}\Gamma_L} + \frac{\delta_{S_{11}} 2e^{2j\phi}}{(\Gamma_L e^{2\gamma} - 1)^2} + \frac{\delta_{S_{22}} 2e^{-2j\phi} e^{2\gamma}\Gamma_L^2}{(\Gamma_L e^{2\gamma} - 1)^2} \right) \tag{22}$$

This expression is further simplified by breaking down its three terms separately, following the notation: $Z_d = Z_d^{(1)} + Z_d^{(2)} + Z_d^{(3)}$. Starting with the first term, $Z_d^{(1)}$, since $e^{2\gamma} = \cosh(2\gamma) + \sinh(2\gamma)$ and (7), resulting in:

$$Z_d^{(1)} - Z_L = \frac{\sinh(\gamma)(Z_L^2 - Z_x^2)}{Z_x \cosh(\gamma) - Z_L \sinh(\gamma)} = \frac{Z_L^2 - Z_x^2}{Z_x \coth(\gamma) - Z_L} \tag{23}$$

that appears in (9).

The other two terms provide simpler expressions if the exponential notation is maintained. By developing Γ_L an in the first term, we get:

$$Z_d^{(2)} = \frac{2e^{2j\phi}\delta_{S_{11}}(Z_L + Z_x)^2 Z_x}{(Z_L + Z_x - e^{2\gamma}(Z_L - Z_x))^2} \tag{24}$$

$$Z_d^{(3)} = e^{2\gamma} \frac{2e^{-2j\phi}\delta_{S_{22}}(Z_L - Z_x)^2 Z_x}{(Z_L + Z_x - e^{2\gamma}(Z_L - Z_x))^2} \tag{25}$$

The overall impedance error is a sum of (23), (24) and (25), resulting in (9). Note that this is an approximation suitable for scenarios with small mismatches, common in practical applications.

APPENDIX B
IMPERFECT TAPER DEMONSTRATION

This appendix aims to provide a mathematical demonstration for (1), which is intended to state the S-parameters of a non-ideal lossless taper in a simple manner that can then be used for further mathematical demonstrations. Considering Z_x, the output impedance seen into the taper from the DUT-side when the connector-side is terminated with the system impedance, then, using power waves definition [37], we get:

$$\boldsymbol{S_T} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & 0 \end{bmatrix}_{Z_s, Z_x^*} \tag{26}$$

assuming a real Z_s (the impedance of the measurement system). We can consider $S_{22} = 0$ by definition of the power-waves S-parameters, since the matrix is normalized to the complex conjugate of the output impedance in that port, the port is conjugate matched. Knowing that the taper is reciprocal

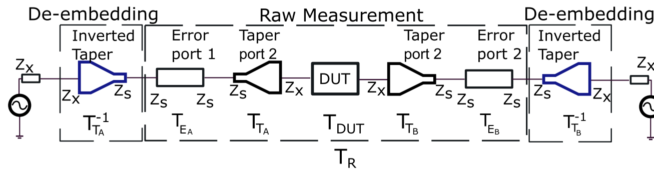

FIGURE 30. Block diagram of the conceptual de-embedding of a 2-port raw measurement (T_R).

and lossless [29], we can obtain the following equation system that provides us with the basis for (1):

$$\begin{cases} |S_{11}|^2 + |S_{21}|^2 = 1 \\ |S_{22}|^2 + |S_{12}|^2 = 1 \\ S_{12} = S_{21} \\ S_{22} = 0 \end{cases} = \begin{cases} S_{12} = S_{21} \\ |S_{21}| = 1 \\ S_{11} = 0 \\ S_{22} = 0 \end{cases} \tag{27}$$

Considering that the taper has the electrical length of ϕ, then $S_{21} = S_{12} = e^{-j\phi}$, resulting in the mentioned S-parameter description for the imperfect taper.

APPENDIX C
TWO-PORT ERROR DEMONSTRATION

This appendix aims to detail the development of the error analysis to a two-port DUT. As this increases the complexity of the analysis, the following demonstration assumes a few simplifications from the start: the launchers are the same in both ports and, consequently, their Z_x; the error appears in both ports in the connector-side of the measurement; the error block can be described by a lossless Z_s Ω line, i.e., only a delay error is considered.

With this established, we can consider a two-port system as in Fig. 30. This system resembles the one presented in Fig. 4, but now representing the operation:

$$\begin{aligned} \boldsymbol{T_D} &= \boldsymbol{T_{T_A}}^{-1}\boldsymbol{T_R}\boldsymbol{T_{T_B}}^{-1} \\ &= \boldsymbol{T_{T_A}}^{-1}\boldsymbol{T_{E_A}}\boldsymbol{T_{T_A}}\boldsymbol{T_{DUT}}\boldsymbol{T_{T_B}}\boldsymbol{T_{E_B}}\boldsymbol{T_{T_B}}^{-1} \end{aligned} \tag{28}$$

where $\boldsymbol{T_R}$ is the T-parameter matrix representation of the 2-port raw measurement, and $\boldsymbol{T_{T_A}} = \boldsymbol{T_{T_B}} = \boldsymbol{T_T}$, given by the S-to T-parameters transformation of:

$$\boldsymbol{S_T} = \begin{bmatrix} 0 & e^{-j\phi} \\ e^{-j\phi} & 0 \end{bmatrix}_{Z_x^*, Z_x^*} \tag{29}$$

where ϕ is the electrical length of the taper. Then, the error blocks are given by:

$$\boldsymbol{S_{E_{A,B}}} = \begin{bmatrix} 0 & e^{j\theta_{A,B}} \\ e^{j\theta_{A,B}} & 0 \end{bmatrix}_{Z_s, Z_s} \tag{30}$$

where $\theta_{A,B}$ is the electrical length of the error block of ports 1 and 2, respectively. The DUT is given a generic S-parameter matrix:

$$\boldsymbol{S_{DUT}} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}_{Z_x, Z_x} \tag{31}$$

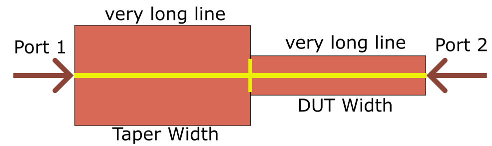

FIGURE 31. Example of the EM simulation of the DUT's transitions.

Developing (28) and converting it into S-parameters results in:

$$\boldsymbol{S_D} = \begin{bmatrix} S_{11}e^{2j\theta_A} & S_{12}e^{j\theta_A}e^{j\theta_B} \\ S_{21}e^{j\theta_A}e^{j\theta_B} & S_{22}e^{2j\theta_B} \end{bmatrix}_{Z_x, Z_x} \tag{32}$$

As demonstrated in [37], the Z-parameter matrix can then be obtained by:

$$\boldsymbol{Z_D} = (\boldsymbol{I} - \boldsymbol{S_D})^{-1}(Z_x^*\boldsymbol{I} + Z_x\boldsymbol{S_D}) \tag{33}$$

where $\boldsymbol{I}$ represents the identity matrix. To expand this expression into a Z-parameter error ($\boldsymbol{Z_D} - \boldsymbol{Z_{DUT}}$), another simplification needs to be taken: $\theta_A = \theta_B = \theta$, so that $\boldsymbol{S_D} = \boldsymbol{S_{DUT}}e^{j2\theta}$. This implies that the errors are identical in both ports. Although it is an unlikely scenario, it allows for the development of a concise Z-parameter error expression that can provide some insight into these more complex cases. So, following this consideration, for a real Z_x, (33) can be developed into:

$$\boldsymbol{Z_D} - \boldsymbol{Z_{DUT}} = (Z_x^2\boldsymbol{I} - \boldsymbol{Z_{DUT}^2})(\boldsymbol{Z_{DUT}} + j\boldsymbol{I}Z_x\cot(\theta))^{-1} \tag{34}$$

For a complex Z_x we can obtain:

$$\begin{aligned} \boldsymbol{Z_D} - \boldsymbol{Z_{DUT}} &= (|Z_x|^2\boldsymbol{I} - \boldsymbol{Z_{DUT}^2} - 2j\Im\{Z_x\}\boldsymbol{Z_L}) \\ &(\boldsymbol{Z_{DUT}} + j\boldsymbol{I}[\Re\{Z_x\}\cot(2\theta) + \Im\{Z_x\}])^{-1} \end{aligned} \tag{35}$$

Note that, despite their matrix formulation these expressions share a similar form with the ones obtained for the single-port DUT ((34) is similar to (10), and (35) is similar to (16)). This implies that the conclusions taken for the single-port case are also applicable to a two-port measurement.

APPENDIX D
MEASUREMENT TRANSITION PREDICTION

The TRL method is incapable of de-embedding transmission line discontinuities like the ones presented in Fig. 25. This implies that the result of the TRL method contains the response of the DUT and those discontinuity effects. However, the DUTs designed in this work are simple, and the discontinuity can be accurately predicted using an EM simulator.

In this case, simulations similar to those shown in Fig. 31 were performed in the microwave Momentum simulator of Keysight's ADS. The response of these simulations was de-embedded from the measured results to obtain the DUT's response. To observe the effectiveness of this method, we can look at Fig. 28, where the TRL-obtained measured results are compared to the EM simulation of the DUT with the added transitions described in this appendix.

Notably, the predictions align remarkably well with the actual measurements for cases where Z_x and Z_L exhibit

proximity. Throughout all scenarios, the measured results consistently fall within the anticipated error margins under these conditions. With this method, it is possible to overcome the TRL's limitations in this specific test case.

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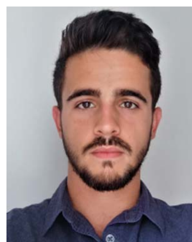

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