# Low-Voltage CMOS Capacitor-Less LDOs: Bulk-Driven Versus Gate-Driven Comparative Study

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***Abstract*— This paper explores the feasibility of a capacitor-less (CL) low-dropout (LDO) regulator to operate efficiently in a low-voltage environment. The CL-LDO scheme selected is based on a unity-gain feedback configuration around the error amplifier (EA), so that the inclusion of high-value on-chip resistors is avoided and different key parameters, such as the power supply rejection or the noise, are optimized. A comparative analysis has been carried out over the same LDO structure including a bulk-driven and a gate-driven EA, respectively. The pass branch of the voltage regulator is provided with pseudo-class-AB operation, in order to lead to a very small quiescent current in the standby operation mode, whereas a very large current can be delivered to the load when required. Both regulators were designed and fabricated in 180 nm CMOS technology to operate with a maximum supply voltage of 1.8 V. The extensive experimental characterization showed that the bulk-driven LDO can achieve a significantly lower minimum supply voltage, i.e., 0.6 V, as compared to the gate-driven counterpart, 1 V, under the same reference voltage and load current conditions.**

***Index Terms*— Bulk-driven MOS, capacitor-less LDO, low-power, low-voltage, voltage regulator.**

## I. Introduction

NOWADAYS micro-energy harvesting is a suitable solution to supply a low-power autonomous system [1]. The block diagram of a battery-less system-on-chip, illustrated in Fig. 1, comprises a harvester, a power management unit (PMU), and the load. In general, the energy harvested from the environment, typically in the nW to $\mu$W range in a miniaturized device [2], [3], [4], is processed using a DC-DC converter to increase the voltage and track the maximum power operation point. A low-dropout (LDO) voltage regulator can be used to control the output voltage of the PMU and deliver the current demanded by the load [5], [6], [7], [8]. The LDO may be designed in a compact manner using an integrated capacitor, resulting in a capacitor-less (CL) LDO [9], [10], [11], [12], [13], [14].

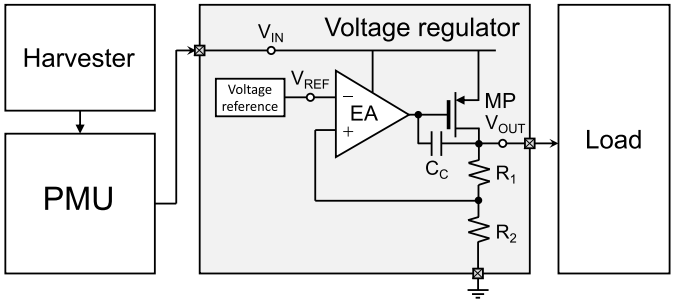


Fig. 1. Block diagram of a system-on-chip supplied by an energy harvester.

The conceptual schematic of a CL-LDO is detailed in the shadowed box in Fig. 1. It consists of a pass transistor, MP, used to modulate the load current, an error amplifier (EA) in charge of controlling MP so that the output voltage, $V_{OUT}$, is a function of a reference voltage, $V_{REF}$, and a feedback network that closes a control loop around MP and the EA. The feedback loop established in the LDO leads to the following expression valid for DC and the low frequency range:

$$V_{OUT} = V_{REF} \cdot \frac{A_{EA} \cdot A_p}{1 + \beta \cdot A_{EA} \cdot A_p} \approx V_{REF} \cdot \frac{1}{\beta} \quad (1)$$

where $A_{EA}$ is the DC gain of the EA, $A_p = g_{m,MP} \cdot r_{o,MP}$ is the intrinsic gain of MP, being $g_{m,MP}$ and $r_{o,MP}$ the transconductance and output resistance, respectively, and $\beta$ is the gain of the feedback network. In the desirable case in which the gains of the error amplifier and the pass transistor are very high, the output voltage relies on the reference voltage only through $\beta$. This requires that MP operates in saturation, i.e., that $V_{SD,MP} > |V_{DSat,MP}|$. At the same time, the power efficiency is optimized as the voltage drop $V_{SD,MP} = V_{IN} - V_{OUT}$ is minimized, that is, when there is a low voltage shift between the input and output voltages of the voltage regulator.

In a micro-energy harvester, power consumption must be optimized, which requires a high efficiency for the DC-DC

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converter and ultra-low-power consumption for the voltage regulator. Thus, LDOs with a very-low quiescent current, $I_Q$, and able to provide a large dynamic current have been proposed [15], [16], [17]. In these cases, ensuring the stability of the LDO for a light load current is challenging. Besides, the reduction of the LDO input voltage, $V_{IN}$, allows decreasing the number of stages of the DC-DC converter used to elevate the harvested voltage. Different solutions can be found to satisfy this requirement [15], [18], [19], [20]. The use of bulk-driven (BD) transistors at the input of an analog circuit results in an increase of the input voltage range and enables operation under lower supply voltages [21], [22], [23]. Recently, BD transistors have been incorporated to the input stage of the EA with the goal of reducing $V_{IN}$ in an LDO [24]. Indeed, the use of a BD differential pair in the EA allows setting the value of $V_{REF}$ to any level between the rails while supplying the LDO with the lowest possible voltage required to keep in saturation all the transistors in the BD differential section.

In this paper, two LDOs with identical structures are compared. Both employ a unity-gain non-inverting feedback configuration, i.e., $\beta = 1$. However, they differ in the input stages of their error amplifiers: one utilizes a conventional GD input pair, while the other one employs a BD differential pair. The main goal is to obtain an LDO with rail-to-rail programmability of the output voltage, even in the case of extremely low supply voltages. For this reason, the central focus of this proposal is on determining the input voltage and reference voltage ranges required for proper operation in each case. Additionally, the pros and cons of both implementations are evidenced by means of a theoretical study and experimental results. The rest of the manuscript is organized as follows. In Section II the structure of an LDO is described and its implementation and theoretical analyses are carried out in Section III. Experimental results are discussed in Section IV and conclusions are drawn in Section V.

## II. Low-Power Low-Voltage LDO

When designing analog circuits, it is important noting that low-power consumption and low-voltage operation are not always equivalent. Low-voltage capability may demand additional stages to meet specific requirements, which can actually increase power consumption. Next, some considerations to accomplish both low power consumption and low voltage operation when designing an LDO, applicable to quiescent current levels in the nA and a few $\mu$A range, are discussed.

### A. LDO Architecture for Low-Power Consumption

In the LDO illustrated in Fig. 1 the feedback loop around the EA is established by a resistive network implementing a voltage divider, i.e., $\beta = R_2/(R_1 + R_2)$. This structure presents important challenges in a monolithic realization. Indeed, when a very low level of $I_Q$ is desired, the values of the resistors in the feedback network have to be extremely large [17]. Indeed, this circuit section is often realized by means of active components, i.e., transistors, operating as pseudo-resistors [17]. Besides, an accurate value of $\beta$ can be achieved by properly matching the relative values of $R_1$ and $R_2$. Nevertheless, the unavoidable variations of their absolute values that take place during the fabrication process will lead to a noticeable variation of the value of $I_Q$, as the current flowing through the output branch depends on the absolute value of the feedback resistors and on the level to which $V_{OUT}$ is intended to be set.

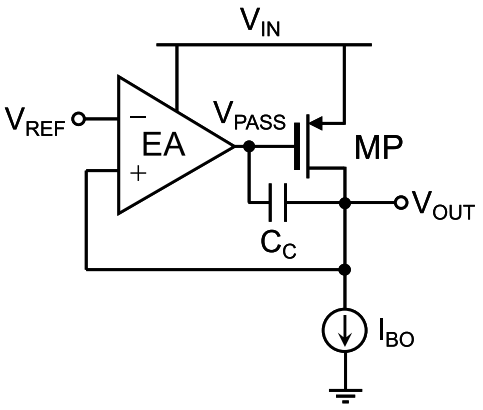


Fig. 2. LDO with unity-gain feedback network.

The dependence of the quiescent current of the LDO pass branch on the resistive feedback shown in Fig. 1 can be avoided by using the unitary feedback LDO illustrated in Fig. 2. In order to prove this potential advantage, three different feedback configurations, i.e., a unity-gain feedback, a feedback network based on polysilicon resistors, and a feedback network based on diode-connected MOS transistors, have been subjected to a corner analysis. A preliminary benefit of the unity-gain feedback structure is the reduction of the area occupation, as the feedback network is reduced to a wire, whereas the case based on polysilicon resistors leads to the most demanding area requirements. Furthermore, the simulation of the DC current flowing through the output branch of the LDO in all the corners and using the three feedback configurations mentioned provided a standard deviation over mean value ratio ($\sigma(I_Q)/\mu(I_Q)$) of nearly zero for the unitary-gain case, 108/1.023 nA/$\mu$A (10.5%) for the use of polysilicon resistors, and 3.16/2.59 $\mu$A/$\mu$A (122%) for the implementation with diode-connected MOS transistors.

Some key metrics in an LDO rely inversely on $\beta$ and they are, hence, optimized when it reaches its maximum value, i.e., for $\beta = 1$. One of these parameters is the power supply rejection (PSR), which indicates how the output voltage, $v_{out}$, is affected by an undesired signal at the input terminal, $v_{in}$, as follows [25]:

$$PSR \equiv \frac{v_{out}}{v_{in}} = \left[\frac{1 - PSR_{EA}}{\beta A_{EA}} + \frac{1}{A_p} \cdot \frac{1}{\beta A_{EA}}\right] \quad (2)$$

where $PSR_{EA}$ is the gain from the input of the LDO to the output of the error amplifier, i.e., $v_{pass}/v_{in}$. It can be inferred from (2) that the PSR is minimized by maximizing $\beta$.

On the other hand, the power spectral density of the output noise of the LDO in Fig. 1 may be expressed as [9]

$$v_{N,out}^2(f) = \frac{1}{\beta}\left[v_{N,ref}^2(f) + v_{N,EA}^2(f) + \frac{v_{N,pass}^2(f)}{A_{EA}^2(f)}\right]$$

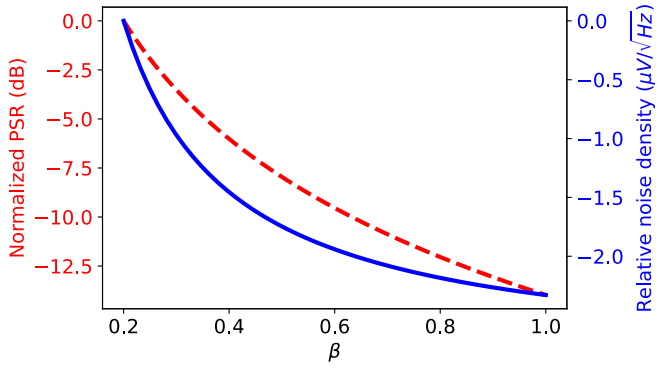


Fig. 3. Simulated response of PSR and output noise when the feedback factor, $\beta$, is swept.

$$+ v_{N,R_1}^2(f) + v_{N,R_2}^2(f)\left(\frac{R_1}{R_2}\right)^2 \tag{3}$$

where each term within the brackets comprises the thermal and flicker noise components of the voltage reference connected at terminal $V_{REF}$, the error amplifier, and the pass branch, respectively, representing the last two terms the thermal noise of the feedback resistors. The noise contribution of the EA can be neglected, as it is divided by its open-loop gain, $A_{EA}$. At this point, it is worth to indicate that the unitary feedback loop configuration for the LDO illustrated in Fig. 2 leads to a noise reduction. Indeed, on the one hand, feedback resistors are avoided, with the consequent suppression of these noise sources and, on the other hand, the noise given by expression (3) is minimized for the maximum possible value of the feedback factor, i.e., $\beta = 1$.

Electrical simulations were employed to assess the influence of the feedback factor on both the PSR and the output noise of the LDO depicted in Fig. 2. The results can be found in Fig. 3, where the values of the PSR (red dashed line) and the output noise spectral density (continuous blue line) are expressed relative to the baseline value for $\beta = 0.2$. In accordance with equations (2) and (3), both the PSR and the noise exhibit an improvement by maximizing the value of the feedback factor i.e., $\beta = 1$, which is the selected choice in our design.

Therefore, some of the constraints imposed by the feedback network in a low-power application can be overcome by connecting the EA in a non-inverting unity-gain feedback configuration, i.e., by directly shorting the noninverting input of the EA to the output terminal of the LDO, as shown in Fig. 2. In this case, no feedback network is required and the current flowing through the pass branch in absence of load current can be generated by means of an appropriate circuit section. Nevertheless, in this case the requirements imposed to the input common-mode (CM) voltage range of the EA are more stringent. Indeed, the expression in (1) becomes now $V_{OUT} = V_{REF}$ and the input CM voltage of the EA must be able to range from ground up to a voltage very close to $V_{IN}$ if a wide range for the output voltage of the LDO is desired.

### B. EA Structure for Low-Voltage Operation

The conventional input stage used in the EA of an LDO is based on a GD differential pair, and is illustrated in Fig. 4a in a PMOS version. The input CM voltage range of this differential structure can be expressed as

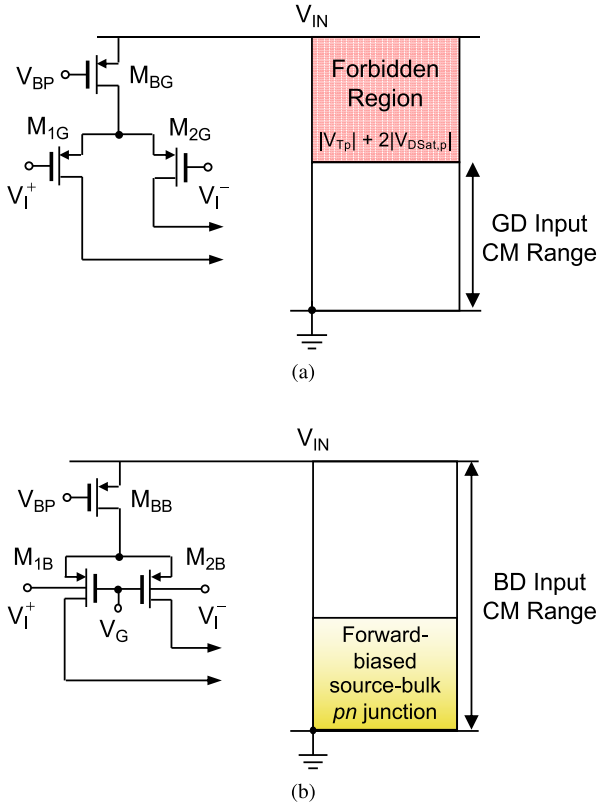


Fig. 4. PMOS differential pair: (a) gate-driven and (b) bulk-driven implementation.

$$V_{GND} \leq V_{I_{EA},CM(GD)} \leq V_{IN} - V_{SG,M1G-2G} - |V_{DSat,MBG}| \tag{4}$$

where $V_{SG,M1G-2G}$ and $V_{DSat,MBG}$ are the source-to-gate voltage of transistors M1G and M2G and the source-to-drain saturation voltage of device MBG, respectively. The operating regions of the GD differential pair are illustrated on the right-hand side of Fig. 4a, where the different voltage drops involved in the operation of the structure are represented. An important limitation of $V_{I_{EA},CM(GD)}$ close to $V_{IN}$,represented in Fig. 4a by a red box and in the order of a threshold voltage and two saturation voltages, becomes apparent from (4). This constraint prevents the operation of the LDO in the low-dropout regime, as the output voltage cannot reach a value close to $V_{IN}$ when the EA is connected in the unity-gain feedback configuration in Fig. 2.

This situation can be overcome by using the BD PMOS differential pair illustrated in Fig. 4b. In the BD transistors a DC voltage, $V_G$, is applied to the gate terminal to turn them on, whereas the input signal is processed through the bulk. There is a design trade-off associated to the gate voltage level selected for the bulk-driven MOS transistors, which involves the effective transconductance and the input current [26]. When the gates of transistors M1B and M2B are connected to the lowest voltage available, i.e., to ground, the voltage at the common-source terminal is pushed down and allows reducing

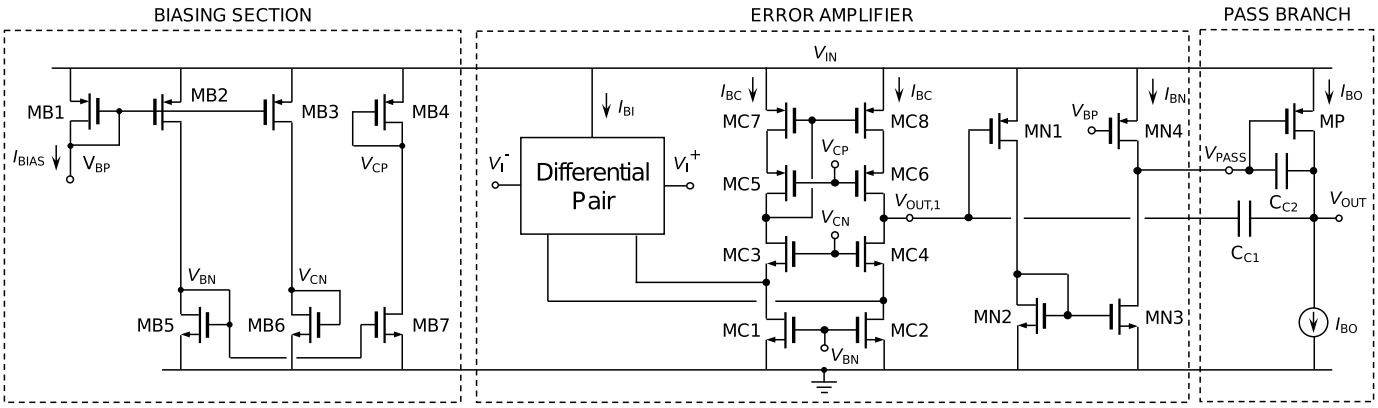


Fig. 5. Proposed low-voltage CL-LDO with generic differential pair in the error amplifier.

the bulk voltage without any risk of important forward biasing of the corresponding *pn* junction formed by the source and bulk terminals. This fact is pointed out in Fig. 4b, where the yellow box represents the region in which the bulk voltage is lower than the source voltage. This leads to a forward-bias condition that, however, does not lead to a significant current flowing through the parasitic diode [26]. Moreover, the hazard of forward operation of these parasitic diodes is reduced as the tail current of the BD differential pair is decreased, which leads to the reduction of the source-to-gate voltage of the input drivers and, consequently, of the voltage level at the common source node. In view of the operating regions on the right-hand side of Fig. 4b, the input CM voltage range of a BD differential pair can be expressed as

$$V_{GND} \leq V_{I_{EA},CM(BD)} \leq V_{IN} \tag{5}$$

The limitation arising in the GD case, equal to a threshold voltage plus two saturation voltages, is not present now, provided that the the level of $V_{IN}$ is higher than this amount.

The advantages of the BD technique for low-voltage operation described must be confronted with the inherent disadvantages of this approach. On the one hand, the bulk transconductance, $g_{mb}$ is smaller than the gate transconductance, $g_m$, in a factor approximately equal to 1/3 in the CMOS technology used and with the biasing current selected. This fact impacts on parameters such as the maximum achievable frequency range and the input referred offset voltage and noise, due to the lower intrinsic gain of a BD transistor as compared to a GD device [23]. On the other hand, BD transistors have to be placed in their own tub, reason why in an *n*-well technology the BD devices must be PMOS type. Besides, the source and bulk terminals form an intrinsic *pn* junction, which is forward biased when $V_B < V_S$. The risk of latch-up is not a major issue provided that layout rules are accomplished, but the bulk current could lead to loading effects on preceding stages and must be kept to a minimum extent. These restrictions seem to be determinant when the input voltage of the LDO is sufficiently high so as to use a GD error amplifier. Nevertheless, the use of BD transistors enables the possibility to reduce the input voltage in very constrained operating conditions, as it is the case of micro-energy harvesting applications.

## III. Proposed Low-Power Low-Voltage LDO

In this section the transistor-level implementation of a CL-LDO is detailed and particularized for the GD and BD cases and their theoretical performance is derived in order to establish an analytical comparison.

### A. Transistor-Level Implementation

The proposed LDO, illustrated in Fig. 5, is substantially formed by a two-stage EA and the output branch, which includes the pass transistor MP. The passive network formed by capacitors $C_{C1}$ and $C_{C2}$ is used for frequency compensation, whereas the biasing section, shown at the left-hand side of the circuit schematic, allows onchip generation of all the required biasing voltages and currents from an external current $I_{BIAS}$.

The error amplifier consists of a differential input block, represented as a box in Fig. 5, a folded-cascode summing stage, MC1-MC8, and a non-inverting gain stage, MN1-MN4. Two different approaches have been followed to build the input stage, i.e., the GD and the BD illustrated in Figs. 4a and 4b, respectively. The folded-cascode stage includes a PMOS current mirror, MC5-MC8, which provides a higher PSR for the LDO [9]. Furthermore, the design criterion followed to internally generate the bias voltages $V_{CN}$ and $V_{CP}$ has been to allow the LDO operating under the lowest possible input voltage. The non-inverting gain stage makes possible frequency compensation by means of nested Miller compensation and is based on a low-gain branch, transistors MN1 and MN2, and a common-source gain stage, devices MN3 and MN4.

The output section, illustrated with a higher degree of detail in Fig. 6, includes a current sink that sets the desired output current level and facilitates the discharge of the output node when a transition from heavy to light load occurs, therefore reducing the overshoot time of the regulator. Its operation is based on connecting the current source MBO7 to the output node when MP is turned off ($V_{PASS}$ high). In addition, to increase current conduction in cases where $V_{OUT}$ is very low, transistor MN is connected, which offers greater sinking capability than MBO6 due to its higher overdrive voltage.

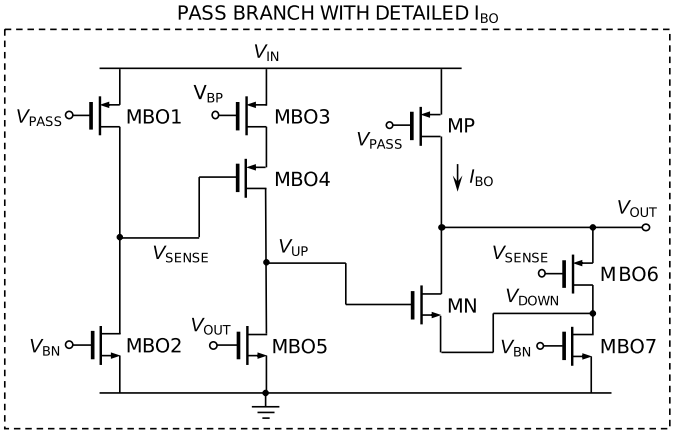


Fig. 6. Detailed circuit schematic of the LDO output branch.

### B. Performance Analysis

Considering (4) and (5), the minimum achievable value of $V_{IN}$ by an LDO with a GD and a BD EA, respectively, is

$$V_{IN,min(GD)} = V_{REF} + V_{SG,M1G-2G} + |V_{DSat,MBG}| \quad (6)$$

$$V_{IN,min(BD)} = V_{SG,M1B-2B} + |V_{DSat,MBB}| \quad (7)$$

In the BD case, $V_{REF}$ is applied to the bulk terminal of one of the input devices and, hence, it is eliminated from the critical DC path from $V_{IN}$ to ground, thus allowing to achieve a much lower minimum supply voltage even when $\beta = 1$. Contrarily, the level selected for $V_{REF}$ constrains the minimum value of the supply voltage that can be used in a GD LDO.

One of the most critical issues of a CL-LDO is the stability in the presence of very light load conditions. In this case, the current flowing through MP is only the tail current of the output stage and the corresponding pole is pushed towards low frequencies. The position of this pole must be higher than the unity gain frequency to ensure a sufficient phase margin and an appropriate transient response. The transfer function of the loop gain implicit in the LDO can be expressed as [27], [28]:

$$LG(s) = \frac{g_{m,MI}g_{m,MN3}g_{m,MP}}{g_{o1}g_{o2}g_{o3}} \cdot \frac{1}{\left(1 + s\frac{C_{C1}g_{m,MN3}g_{m,MP}}{g_{o1}g_{o2}g_{o3}}\right)} \cdot \frac{\left(1 - s\frac{C_{C2}}{g_{m,MP}} - s^2\frac{C_{C1}C_{C2}}{g_{m,MN3}g_{m,MP}}\right)}{\left[1 + s\frac{C_{C2}\left(g_{m,MP} - g_{m,MN3}\right)}{g_{m,MN3}g_{m,MP}} + s^2\frac{C_L C_{C2}}{g_{m,MN3}g_{m,MP}}\right]} \quad (8)$$

The DC gain, $A_{DC}$, dominant pole, $\omega_0$, and secondary poles and zeroes, $\omega_1$, $\omega_2$, $z_1$, and $z_2$, can be determined as

$$A_{DC} = \frac{g_{m,MI}g_{m,MN3}g_{m,MP}}{g_{o1}g_{o2}g_{o3}} \quad (9a)$$

$$\omega_0 = -\frac{g_{o1}g_{o2}g_{o3}}{C_{C1}g_{m,MN3}g_{m,MP}} \quad (9b)$$

$$\omega_1 = -\frac{g_{m,MP} - g_{m,MN3}}{C_L} \quad (9c)$$

$$\omega_2 = -\frac{g_{m,MP} - g_{m,MN3}}{C_{C2}\left(g_{m,MP} - g_{m,MN3}\right)} \quad (9d)$$

$$z_1 = \frac{g_{m,MP}}{C_{C2}} \quad (9e)$$

$$z_2 = -\frac{g_{m,MN3}}{C_{C1}} \quad (9f)$$

where parameter $g_{m,MI}$ represents the transconductance of the input devices of the GD or the BD structure and $\omega_2 \gg \omega_1$ and $z_2 \gg z_1$ has been assumed. The gain at DC and in the low frequency range is high, as it corresponds to a three-stage structure. Consequently, in the case of a BD input stage in the EA the fact of having a lower effective input transconductance is not a major issue. Indeed, simulated open loop gain values of 128 dB and 130 dB are obtained for the GD and BD case.

Regarding the frequency response, nested Miller compensation has been carried out by means of capacitors $C_{C1}$ and $C_{C2}$. The following condition is imposed to the gain-bandwidth product (GBW)

$$GBW = A_{DC} \cdot \omega_0 = \frac{g_{m,MI}}{C_{C1}} < \omega_1 \quad (10)$$

This leads to the following relationship

$$\frac{g_{m,MI}}{C_{C1}} < \frac{g_{m,MP}}{C_L} \quad (11)$$

which can be more easily achieved in the bulk-driven case since $g_{mb} < g_m$. It is worth to point out that, even though the connection of capacitor $C_{C2}$ between the gate and the drain terminals of the pass transistor can cause PSR degradation, it results essential for pole splitting and proper frequency compensation.

The PSR of an LDO usually presents a given value at DC and in the low frequency range, increasing for frequencies higher than the dominant pole of the loop gain. When $\beta = 1$, the PSR in the low frequency band is:

$$PSR = \frac{(1 - A_{oEA}) \cdot g_{o1}g_{o2}}{g_{m,MI}g_{m,MN3}} + \frac{g_{o1}g_{o2}g_{o3}}{g_{m,MI}g_{m,MN3}g_{m,MP}} \quad (12)$$

It can be inferred from (12) that the higher the value of $g_{m,MI}$, the lower the PSR, situation resulting more convenient for the GD solution. Nevertheless, the use of a BD input stage allows implementing more easily an unity-gain feedback loop configuration around the LDO, which also leads to a lower PSR as compared to the case in which $\beta < 1$, as it has been previously shown in Fig. 3.

The line sensitivity (LS), as the PSR, indicates the capability of the LDO to reject signals coming from the supply. At low frequency, the value of the line sensitivity (LS) can also be estimated from (12). Besides, the variation of the output voltage when the load current changes is usually known as load regulation (LR). The the load regulation (LR) relies on the closed-loop output resistance of the LDO, which in our case can be particularized as:

$$R_{out,cl} = \frac{R_{out}}{1 + \beta A_{EA}A_p} \approx \frac{g_{o1}g_{o2}}{g_{m,MI}g_{m,MN3}g_{m,MP}} \quad (13)$$

Increasing the value of $g_{m,MI}$ leads to a more stable output voltage against load current variations, since the output resistance is decreased and is less impacted by the load resistance. Nevertheless, it can be observed in the middle term of (13) that $R_{out,cl}$ decreases as $\beta$ increases and, as previously indicated, the operation with a maximum feedback factor value in a low supply voltage environment is more feasible when a BD input stage is used in the EA.

The line transient and the load transient response are used to determine the behavior of the output voltage against fast variations in the input voltage and the load current, respectively. Obtaining specific expressions for these metrics is a challenging task, especially taking into account that the pass transistor MP can operate in different inversion regions depending on the level of the load current. In any case, it is worth pointing out that the line transient is in general reduced when the PSR is improved, as it is related to the rejection of signals coming from the supply. Besides, the impact on the output voltage of large changes in the load current is reduced when the pass branch is provided with class-AB capability, as effective current sourcing and sinking functions are carried out by transistors MP and MN in Fig. 6.

The overall noise of the LDO is structurally reduced thanks to the unity-gain feedback configuration adopted, which is illustrated in Fig. 2. There are two reasons for this, the maximization of the feedback factor, i.e., $\beta = 1$, and the removal of the feedback resistors. Thus, the general expression in (3) can be particularized as:

$$v^2_{N,out}(f) = v^2_{N,ref}(f) + v^2_{N,EA}(f) + \frac{v^2_{N,pass}(f)}{A^2_{EA}(f)} \tag{14}$$

The noise contribution of the error amplifier, $v^2_{N,EA}(f)$, assuming that is dominated by the input transistors, can be written for the GD and the BD solution as:

$$v^2_{N,EA_{GD}}(f) = 2 \cdot \left[ \frac{K_f}{WLC_{ox}} \cdot \frac{1}{f} + 4kT\gamma \cdot \frac{1}{g_m} \right] \tag{15a}$$

$$v^2_{N,EA_{BD}}(f) = 2 \cdot \left( \frac{g_m}{g_{mb}} \right)^2 \left[ \frac{K_f}{WLC_{ox}} \cdot \frac{1}{f} + 4kT\gamma \cdot \frac{1}{g_m} \right] \tag{15b}$$

where $K_f$ is the flicker noise parameter, $k$ is the Boltzmann constant, $T$ is the temperature, and $\gamma$ is a technology parameter with value around 2/3 for long channel devices. The expressions provided in (15a) and (15b) should include additional terms in case the noise contribution of any of the transistors in the folded-cascode summing stage, MC1 to MC8, becomes comparable to that of the input transistors. The noise generated by a GD and a BD transistor is exactly the same. Nevertheless, the input-referred noise is higher in the case of the BD solution, due to the lower value of the effective bulk transconductance, $g_{mb}$, as compared to the gate transconductance, $g_m$. In addition, the gain of the EA will be generally higher in the case of the GD approach, which also leads to a further reduction of the noise of the pass branch, that is, to the third noise contribution in (14).

It is worth to point out that to reduce random offset voltage in the EA, a suitable layout edition is required. To this end, interdigitization and common-centroid techniques are often used, leading both of them to a higher effective area occupation in the case of the BD solution. Indeed, in the GD approach both input transistors of the EA can be placed in the same tub, whereas for the BD technique each input transistor of the EA must be placed in a different well. Besides, the area is further increased when the BD transistors are divided to implement the previously mentioned matching techniques. Quantitative details on the area increase of the EA due to the use of the BD technique are provided in next Section. Even though the risk of latch-up in a bulk-driven transistor is taken to a minimum extent by just accomplishing the design rules, in the case of the BD LDO the bulk-driven input transistors have been surrounded by a ring of connections to the $n$-tub implementing the substrate to further avoid this potential detrimental phenomenon.

TABLE I
SIZE OF THE DEVICES USED IN THE FABRICATED LDO PROTOTYPES

| Device | (W/L) ($\mu m/\mu m$) |
|---|---|
| M1G,M2G,MBG,M1B,M2B,MBB | 20/2 |
| MC5,MC6,MC3,MC4 | 20/2 |
| MC1,MC2,MC7,MC8,MS2,MS3,MN1,MS4 | 12/2 |
| MP | 900/1 |
| MN | 9/2 |
| MBO1,MBO2 | 0.6/2 |
| MBO4,MBO6 | 10/0.3 |
| MBO3 | 0.75/1 |
| MBO5 | 6/1 |
| MBO7 | 36/1 |

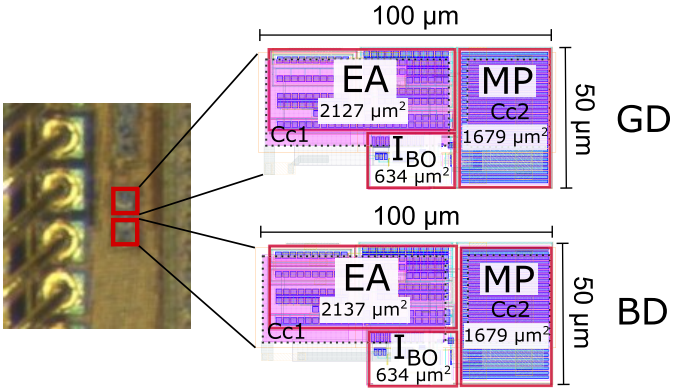


Fig. 7. Chip microphotograph and layout captures.

## IV. EXPERIMENTAL RESULTS

The LDO in Fig. 5 was designed and fabricated in standard 180 nm CMOS using only regular-$V_{th}$ transistors with nominal threshold voltages of 438 mV and −454 mV for NMOS and PMOS devices, respectively. For the sake of comparison, two silicon prototypes of the LDO, containing the gate-driven and the bulk-driven input stages in Fig. 4, were considered. In the experimental characterization, $V_{IN}$ and $V_{REF}$ adopted different values, even though the nominal operating conditions were selected to be $V_{IN} = 1$ V and $V_{REF} = 0.6$ V. Transistor dimensions can be found in Table I. The aspect ratios of all the devices have been equally sized in order to carry out a fair comparison. Nevertheless, the structures of the BD and the GD differential pair in Fig. 4 can be modified to optimize each design in view of an intended set of specifications. The biasing current of the LDO was $I_{BIAS} = 1$ $\mu$A. A microphotograph of the chip as well as the layout captures are depicted in Fig. 7. As can be seen, the use of bulk-driven transistors leads to an increase in the silicon area of the BD EA with respect to the

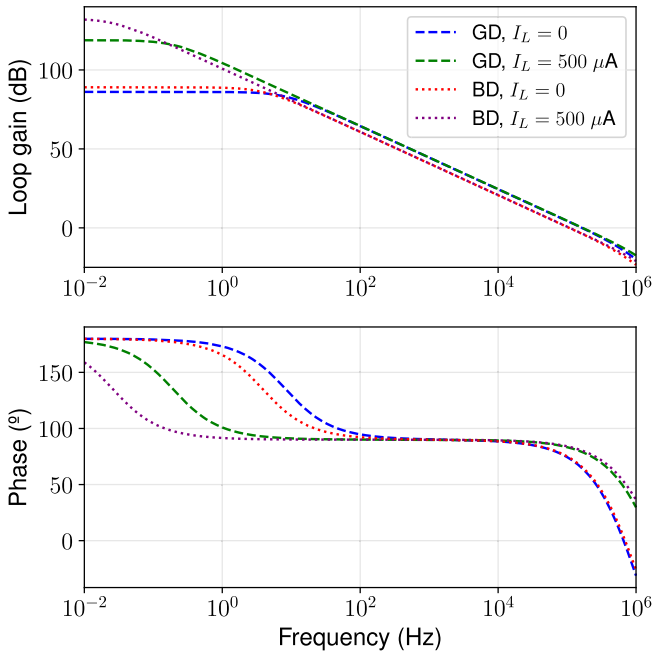


Fig. 8. Simulated frequency response of the gate driven and bulk driven error amplifier LDOs with no load and with a load current of 500 $\mu$A.

GD case which, for this particular implementation, is of only 0.47%.

The compensation capacitors $C_{C1} = 3.6$ pF and $C_{C2} = 1.8$ pF were implemented as metal-insulator-metal (MIM) devices. The simulated frequency response of the loop gain in the GD and BD LDOs is depicted in Fig. 8. This simulation was carried out in the typical mean corner and at room temperature, with a load capacitance of $C_L = 10$ pF and for $V_{IN} = 1$ V and $V_{REF} = 0.6$ V. Under these conditions when $I_L = 0$ (representing the worst stability scenario), the GD LDO achieved a phase margin of 65°, while the BD LDO achieved a phase margin of 74°. Additionally, by performing a process corner analysis while keeping $C_L = 10$ pF and $I_L = 0$, a minimum phase margin of 61° for the GD LDO and 65° for the BD LDO is ensured in the temperature range from −20°C to 80°C. The maximum value of $C_L$ that ensures a phase margin higher than 45°, across all corners and the considered temperature range, is 13 pF for the gate-driven LDO and 18 pF for the gate-driven LDO. In any case, it is not possible to ensure the load conditions in the experimental testbench of the LDO, which are most likely increased as compared to the simulated characterization, due to the unavoidable effect of the integrated circuit PADs, wire bonding, chip carrier, test PCB, and measurement setup.

The two LDOs were first characterized at DC. The input/output transfer characteristics for different values of $V_{REF}$ and with $V_{IN}$ varying from ground to 1 V are depicted in Fig. 9 for a load current $I_L = V_{OUT}/R_L$ with a load resistor taking the value $R_L = 1.5$ kΩ. It may be observed that the minimum supply from which the operation in the LDO starts is around 0.5 V in both cases. Nevertheless, the GD realization shows a hump in the response of the output voltage around the switch-on region, requiring a value of $V_{IN}$

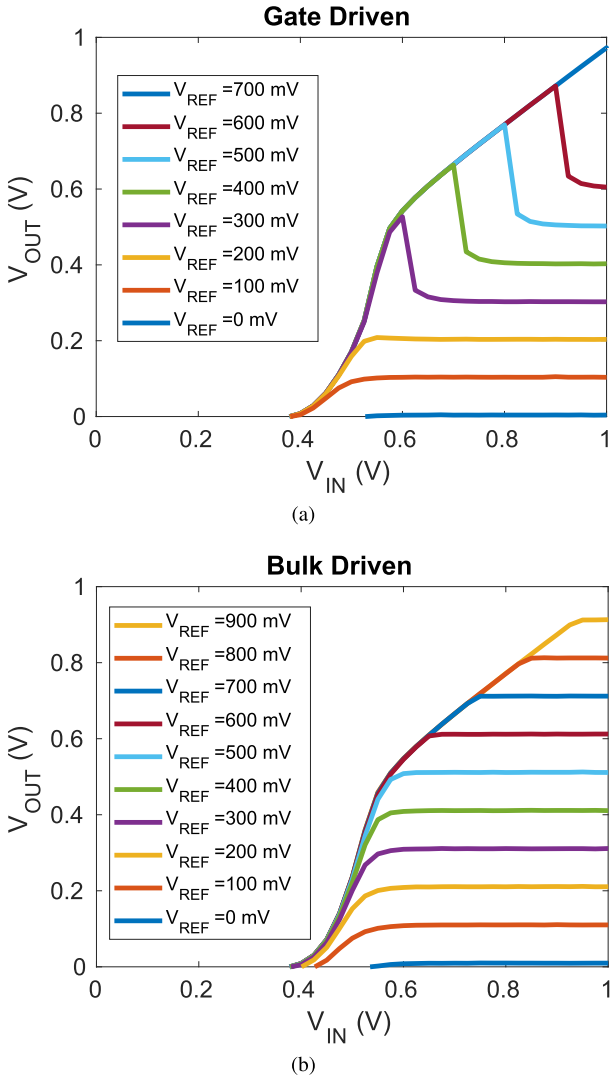


Fig. 9. Experimental output voltage $V_{OUT}$ varying the input voltage $V_{IN}$ for (a) the GD and (b) the BD LDO.

increasingly higher to operate as $V_{REF}$ is raised. Conversely, the BD approach requires a minimum value of $V_{IN}$ for proper operation that is approximately equal to the value of $V_{REF}$. The line sensitivity may be determined from the plots in Fig. 9, yielding values equal to $LS_{GD} = 10.0$ mV/V and $LS_{BD} = 0.5$ mV/V for the gate-driven and the bulk-driven solution, respectively. Besides, the output voltage of the LDO is represented in Fig. 10 as a function of the load current for different values of $V_{REF}$. As can be seen, the GD solution does not properly respond for values of $V_{REF}$ higher than 0.6 V while the BD approach offers a rail-to-rail range for $V_{REF}$. The load regulation was determined to be $LR_{GD} = 6.0$ mV/mA and $LR_{BD} = 2.9$ mV/mA for the gate-driven and the bulk-driven regulator, respectively. If $V_{IN} = 1.8$ V, maximum voltage level allowed in the selected technology, the load current $I_L$ can reach values higher than 27 mA in both cases.

Figs. 11, 12a and 12b illustrate the dynamic behavior of both LDOs. In the PSR response, depicted in Fig. 11, it can be seen that for the particular case of input voltages of

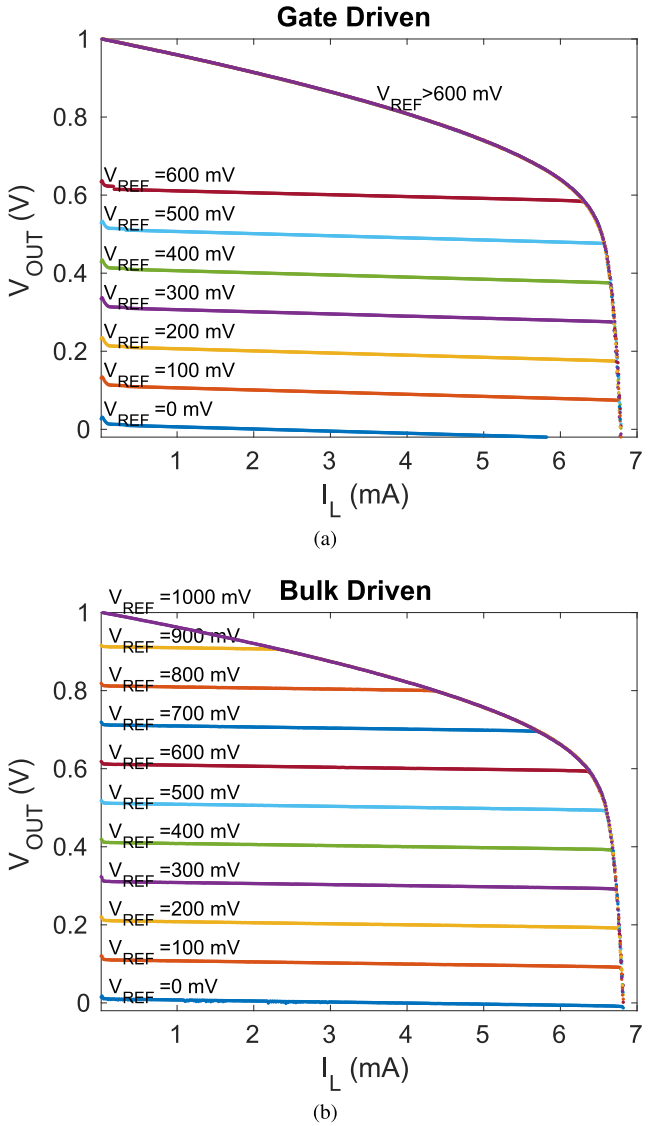


Fig. 10. Experimental output voltage $V_{OUT}$ sweeping the load current $I_L$ for (a) the GD and (b) the BD LDO.

700 mV the bulk-driven LDO operates as expected, while the gate-driven approach needs an input voltage $V_{IN} > 1$ V to offer a normal behavior. Regarding the time response, recovery time is a key metric to determine the dynamic accuracy of the LDO [29]. From the load transient responses, it can be inferred that with an input voltage $V_{IN} = 700$ mV, shown in Fig. 12a, the BD solution is able to regulate the output voltage, as expected, while the GD version is not working ($V_{OUT}$ is almost equal to $V_{IN}$ and not equal to the reference voltage $V_{REF} = 600$ mV). When the input voltage is increased to a nominal value $V_{IN} = 1$ V (Fig. 12b), both LDO implementations can properly regulate the output voltage. An extensive experimental characterization of the time response of the LDO when the load current was stepped from a minimum value of 30 nA to a maximum value ranging between 300 $\mu$A and 5 mA was carried out, obtaining in all the cases similar responses to those illustrated in Figs. 12a and 12b. The ripple noticeable at the beginning of each transition in Fig. 12b, slightly longer than 10 $\mu$s, is ascribed to the limited phase margin available, which is further reduced by the measurement setup.

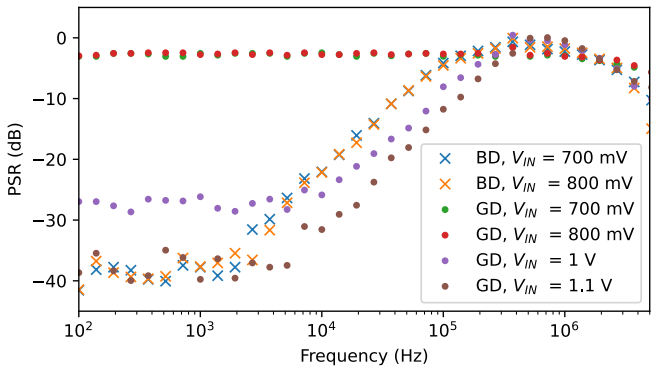


Fig. 11. PSR with a load resistor $R_L = 1.2$ kΩ.

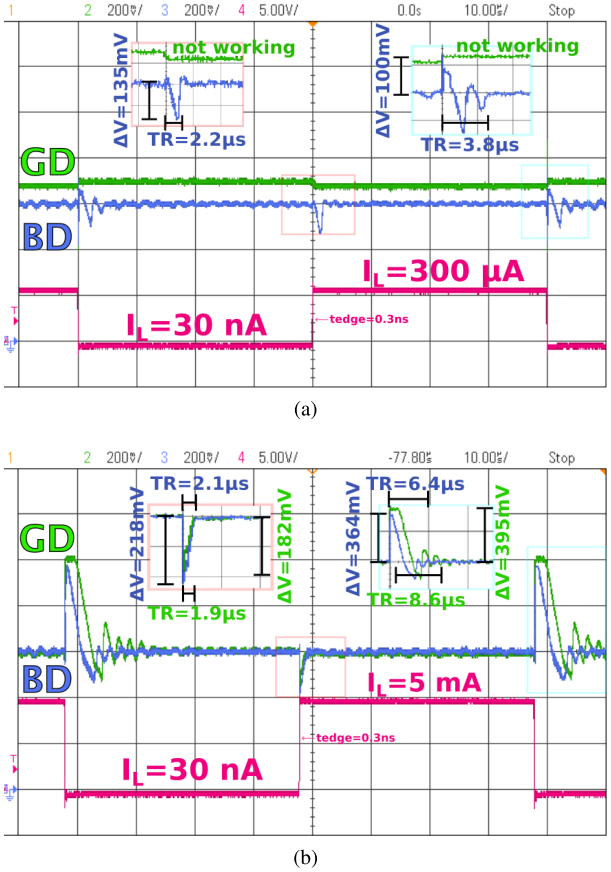


Fig. 12. Measured load transient responses when the LDOs are supplied with (a) $V_{IN} = 0.7$ V and (b) with $V_{IN} = 1$ V. Transient details are indicated by the overlaid figures. Green labels are associated with GD LDO and blue labels correspond to BD LDO.

A summary of the experimental performance of the proposed LDOs is provided in Table II, where they are compared with state-of-the-art solutions. For the sake of fairness, it is worth to emphasize here that the bulk-driven and gate-driven approaches presented have been designed to be compared in a wide variety of key metrics for an LDO, which in some cases lead the corresponding experimental performance farther than desired from the state-of-the-art. Nevertheless, in other cases, the results obtained are the best of the comparison established, as discussed next. Two different figures of merit (FoMs) have been used in order to carry out an objective comparison. On the

TABLE II
SUMMARY OF THE EXPERIMENTAL PERFORMANCE OF THE TWO LDOS DESIGNED AND COMPARISON WITH THE STATE-OF-THE-ART

| **Parameter** | **This work GD** | **This work BD** | **[18] TCAS-I'18** | **[30] TCAS-II'18** | **[32] TCAS-II'19** | **[33] Access'19** | **[15] JSSC'20** | **[31] TCASI'23** | **[34] TCASII'23** |
|---|---|---|---|---|---|---|---|---|---|
| Technology | 180 nm | 180 nm | 65 nm | 180 nm | 180 nm | 65 nm | 55 nm | 180 nm | 28 nm |
| Capacitor-less | yes | yes | yes | yes | yes | yes | no | yes | no |
| Size ($\mu m^2$) | 4440 | 4450 | 4200 | 210000 | 31000 | 7000 | 42000 | 3500 | 1000 |
| Min. $V_{IN}$ (V) | 1 | 0.6 | 1 | 1.6 | 1.2 | 1.2 | 0.8 | 0.5 | 0.6 |
| $I_Q$ (µA)@$V_{IN}$ (V) | 10@1.8 | 9.4@1.8 | 0.03 | 133 | 10.2 | 9.6 | 0.016 | 22.25@0.5<br>35.7@1.8 | 0.0135 |
| $I_{L,max}$ (mA)@$V_{IN}$ (V) | 6.5@1<br>26@1.8 | 0.75@0.6<br>27@1.8 | 10 | 50 | 100 | 70 | 10 | 2@0.5<br>200@1.8 | 10 |
| LS (mV/V) | 10 | 0.5 | - | 2.67 | 10 | 3.84 | 0.5 | 0.346 | 9.7 |
| LR (mV/mA) | 6.0 | 2.9 | 1.22 | 0.194 | 0.081 | 0.29 | 1.05 | 0.0095 | 0.8 |
| PSR@10 Hz (dB) | -40@0.5mA | -40@0.5mA | - | - | - | -67‡ @heavy load | -75@1nA<br>-43@10mA | -62@0 A<br>-47@2mA | - |
| PSR@10 kHz (dB) | -28@0.5mA | -23@0.5mA | -28@10mA | -70@50mA | - | -26‡ @heavy load | -100@1nA<br>-43@10mA | -62@0 A<br>-47@2mA | -26@5mA |
| $\Delta I$ (mA) | 5 | 5 | 10 | 31 | 99 | 70 | 10 | 40 | 10 |
| $T_R$ (µs) | 1.9 | 2.1 | 0.25 | 0.019 | 0.22 | 1.8 | 9.5† | 0.86 | 18 |
| $\Delta V$ (mV) | 182 | 218 | 487.5 | 166 | 200 | 322 | 70 | 72 | 22 |
| $k$ | 86 | 86 | 571 | 1 | 286 | - | 57 | 286 | 286 |
| $FoM_t$ (ns) | 3.8 | 3.9 | 0.00075 | 0.082 | 0.023 | 0.25 | 0.015† | 0.48 | 0.024 |
| $FoM_v$ (mV) | 31 | 35 | 0.84 | 0.71 | 5.9 | - | 0.0064 | 11 | 0.0085 |

† Estimated from the transient response.
‡ Simulation result.

one hand, a widely used FoM, defined as

$$FoM_t = T_R \frac{I_Q}{\Delta I_L} \tag{16}$$

where $T_R$ is the response time, gives an idea on how fast the LDO responds to large changes in the load current, taking also into account the value of the quiescent current. The measured values of $T_R$ were 1.9 $\mu$s and 2.1 $\mu$s for the gate-driven and the bulk-driven solution, respectively. On the other hand, the $FoM_V$ defined as

$$FoM_v = k\Delta V_{OUT} \frac{I_Q}{\Delta I_L} \tag{17}$$

takes into account the output voltage drop, $\Delta V_{OUT}$, when a sudden change in the load current, $\Delta I_L$, occurs, weighted by the quiescent current, $I_Q$, and by a term $k$ that is the ratio between the current step edge time over the fastest current edge of the comparative [30]. The values of $\Delta V_{OUT}$ measured in the fabricated LDOs were 182 mV and 218 mV for the gate-driven and the bulk-driven approach, respectively. As it can be seen in Table II, the proposed bulk-driven LDO is able to operate from one of the lowest input voltages while keeping a reduced size and line sensitivity. In fact, remarkably only [31] reports a smaller $V_{IN}$, but with a significantly higher quiescent current, which highlights the main benefit of the bulk-driven error amplifier approach in very constrained operating conditions such as micro-energy harvesting. In comparison, the gate-driven alternative shows worse line sensitivity and load regulation values but a better $FoM_v$ yet with input voltages higher than 1 V. Both the proposed GD and BD LDOs provide very reduced power consumption and silicon area.

## V. CONCLUSION

The unitary-feedback architecture offers advantages in a low-voltage low-power LDO, enhancing PSR, eliminating feedback resistors, and enabling an easier adjustment of the quiescent current of the output branch. However, employing a conventional gate-driven input pair in the error amplifier faces limitations when the output voltage is set close to the input voltage in this configuration. Introducing bulk-driven transistors in the input pair of the error amplifier in an LDO with unitary feedback factor facilitates setting the output voltage at any level in the range from ground to the input voltage, resolving this constraint efficiently. Two LDOs have been implemented on silicon using the same structure and only changing the input pair type. It has been proven experimentally that the bulk-driven input pair solution allows to reduce the supply voltage as compared to the traditional gate-driven approach due to its rail-to-rail common mode operation range.

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