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Voltage Reference and Voltage Regulator for the Cryogenic Performance Evaluation of the 22 nm FDSOI Technology

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ABSTRACT This paper presents the design and cryogenic electrical characterization of a voltage reference and a linear voltage regulator at temperatures between 6 K and 300 K. Both circuits are employed as test vehicles for the experimental performance evaluation of the 22 nm FDSOI MOS technology when used as platform for the development of cryogenic analog systems, whose role is relevant in Quantum Computing (QC) applications. Additionally, we report the impact that MOS transistor cryogenic phenomena have over these circuits and propose to take advantage of some of those phenomena in analog circuit design. In particular, we focus on the cryogenic threshold voltage (V_{th}) saturation, the transconductance (g_m) increase and the low frequency (LF) excess noise. Our experimental results indicate that the cryogenic V_{th} saturation and the g_m increase can be used as circuit design tools, while the LF excess noise is a performance handicap for cryogenic analog circuits.

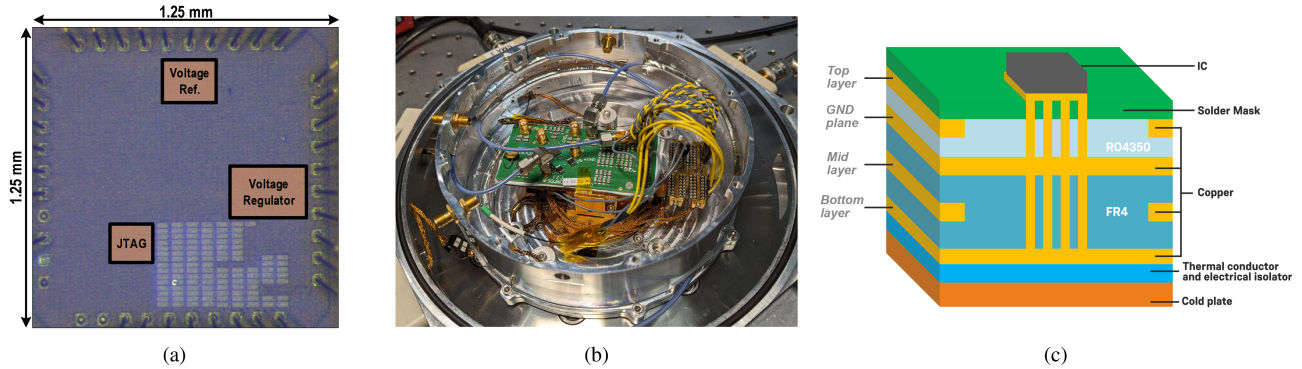
INDEX TERMS Cryogenics, fully depleted silicon-on-insulator (FDSOI), low-frequency noise, metal-oxide-semiconductor (MOS), quantum computing, voltage reference, voltage regulator.

I. INTRODUCTION

THE USE of quantum physics phenomena at cryogenic temperatures via the manipulation of a large number of qubits performed by a quantum computer promises to speed up the finding of solutions to the computational challenges faced in drug design, cryptography and logistics [1], [2]. In addition, it has been demonstrated that cryogenic integrated circuits (ICs) based on metal-oxide-semiconductor (MOS) devices will be an important part of QC systems and its scalability. Therefore, the development of analog, digital, and mixed-signal cryogenic ICs has attracted significant attention in the last years [3], [4], [5]. Moreover, cryogenic MOS ICs are a relevant part of applications such as astronomical detectors, space exploration and high-performance computing [6], [7], [8].

However, the development of cryogenic analog MOS ICs is challenging. This is because several cryogenic MOS phenomena can severely affect the performance of a circuit; e.g., the cryogenic threshold voltage (V_{th}) increase can push the supply voltage requirement of a circuit to a higher value [9]. Moreover, the simulation models from many MOS technologies are not valid for cryogenic applications. This could be due to the fact that the equation sets used by the models do not consider the cryogenic MOS phenomena or because the ICs commercial manufacturer has not developed a cryogenic process design kit. Consequently, many design teams are constrained to develop ICs without a reliable cryogenic pre-silicon verification. Under these circumstances, there arises the need for an understanding of the analog MOS circuit performance variations caused by the cryogenic phenomena.

This paper contributes to the advancement of the cryogenic analog MOS circuit design discipline by providing an experimental study on the impact that cryogenic MOS



(a) (b) (c)

FIGURE 1. (a) Micrograph of prototype chip. (b) Experimental setup: PCB with prototype chip, mounted onto the Gifford-McMahon cryocooler. (c) PCB stack used for the chip cryogenic thermalisation with electrical isolation from cold plate for ground loop noise coupling avoidance.

phenomena exert over two standard circuit blocks: a voltage reference and a linear voltage regulator. These circuits are employed as test vehicles for the experimental performance evaluation of the 22 nm fully depleted silicon-on-insulator (FDSOI) technology when used as platform for the development of cryogenic analog MOS circuits. In particular, we focus on the cryogenic MOS phenomena of V_{th} saturation, transconductance (g_m) increase and the low frequency (LF) excess noise. Therefore, the design and cryogenic electrical test of both circuits are presented in this study.

A detailed description of the methodology applied in this study is provided in Section II. In our study we investigate the cryogenic V_{th} saturation phenomenon in the NMOS transistor and demonstrate its practical use for the development of cryogenic voltage reference circuits (Section III-A). The impact of the MOS transistor g_m increase is investigated through the cryogenic electrical characterization of a voltage regulator circuit. Our measurements demonstrate that the regulator loop gain increases with temperature reduction, improving in this way the load regulation and power supply rejection performance metrics of this circuit (Section III-B). LF excess noise is a phenomenon consistently observed in MOS transistors of different technologies and can affect the noise performance of the cryogenic analog MOS circuits [10], [11]. In order to assess its impact, the LF noise generated at the outputs of our test circuits is characterized at 8 K and 300 K. As a result, an average increase of 90 % on the LF RMS voltage noise at 8 K is found for both circuits (Section III-C). A discussion concerning the experimental results obtained in this study and a comparison with the state of the art, are provided in Section III-D. Final remarks and conclusions are given in Section IV.

II. METHODOLOGY

A chip containing super-low V_{th} I/O MOS devices was used for the exploratory DC characterization of the 22 nm FDSOI technology in the 7 K – 300 K range [12]. These type of devices are selected due to their reduced V_{th} and dielectric breakdown voltage, being at room temperature around 0.4 V and 2 V respectively. The DC parameters extracted from an NMOS device ($W/L = {}^{1\,\mu\text{m}}/_{0.32\,\mu\text{m}}$) are used in this study. For the cryogenic electrical characterization, a semiconductor device analyzer (B1500A) was used in combination with a cryocooling station (attoDRY800).

With the information obtained by our exploratory 22 nm FDSOI technology characterization, a voltage reference and a linear voltage regulator configured via a JTAG digital communication interface, are designed for cryogenic operation. It must be mentioned that the JTAG interface is only used for an initial configuration of the analog circuits. These circuits are incorporated into a prototype chip, as in Figure 1 (a). The experimental setup is displayed in Figure 1 (b). Inside the cryocooling station, our prototype chips are mounted on PCBs specially designed for good thermal coupling with the cryocooler cold plate; Figure 1 (c) shows an sketch of the employed PCB stack.

Since our cryocooling station uses a modified Gifford-McMahon cold head unit (RDK-101E) employing a rotatory valve motor attached to its chassis, the coldest stage in our setup is electrically linked to the lab physical ground. As explained in [13], such a condition leads to ground loop noise coupling and hence interference in the LF noise measurements. In order to break the ground loop between the cryocooler cold plate and the prototype chip, a thermally conductive-electrically isolating layer (Gap Pad 5000S35) is used as indicated in Figure 1 (c); an alternative layer, with similar properties, can be obtained by applying GE 7031 varnish over a cigarette paper substrate [14]. Moreover, the cables thermalisation is done without an electrical short between the test circuit ground and the lab physical ground. However, the minimum PCB temperature that can be reached with this ground isolation approach is 8 K. In contrast, without these ground isolation measures the lowest PCB temperature in our setup is 6 K; a limit set by the cryocooler cooling power.

In order to measure and control the PCB temperature, a sensing silicon diode (DT-670) is attached on the PCB and monitored during the electrical tests. So as to heat the PCB and perform electrical tests at higher temperatures, a heating resistor (PWR220T-35) attached to the cryocooler cold plate is used. For the electrical test of the prototype chips, DC supply voltage sources (N67050), DMMs (34470A), an

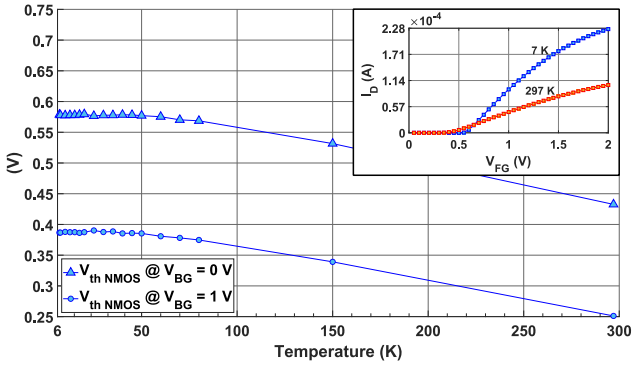


FIGURE 2. V_{th} extracted from an I/O NMOS (W / L = 1 μm / 0.32 μm) via the linear extrapolation method over temperature, for V_{BG} = 0 V and V_{BG} = 1 V. Inset displays the I_D versus V_{FG} curve for 297 K and 7 K, at V_{DS} = 0.1 V and V_{BG} = 0 V.

spectrum analyzer (R&S FSU), a signal source analyzer (E5052B), a low noise amplifier (SR560), a JTAG debugger (J-Link PRO) and a support PC, are utilized.

III. RESULTS AND DISCUSSION

A. THRESHOLD VOLTAGE SATURATION

Typically MOS transistors experience changes of their electrical characteristics when operated at different temperatures. It is also known that the V_{th} of MOS transistors increases with temperature reduction [15]. In the case of the super-low V_{th} I/O NMOS device of the 22 nm FDSOI technology, Figure 2 shows the extracted V_{th} values over temperature via the linear extrapolation method [16]. As expected, the device V_{th} increases with temperature reduction; from 430 mV at 297 K, up to 578 mV at 60 K. However, it can be noticed that the V_{th} saturation phenomenon starts at 60 K. This phenomenon also occurs when the back gate of the device is set to 1 V, with a V_{th} saturation of 387 mV. It is noteworthy that V_{th} tuning via the back-gate terminal is a characteristic offered by FDSOI MOS devices [17]. The cryogenic V_{th} increase and saturation is attributed to the ionization energy increase and the charger carriers freeze-out [18]. Furthermore, [19] argues that the cryogenic V_{th} behavior is due to the temperature dependence of the bulk Fermi potential and the density of interface traps. Besides, the V_{th} saturation has been reported for other technologies, including a commercial 28 nm bulk CMOS technology [19]. While the cryogenic V_{th} saturation of 22 nm FDSOI technology is reported in [20], to the best of the authors knowledge, it has not being intentionally used in the design of cryogenic analog circuits.

The circuit shown in Figure 3 exploits the cryogenic V_{th} saturation as a feature for the generation of a reference voltage. The circuit is composed of beta-multiplier and self-bias V_{FGS} current sources, that together bias a diode connected NMOS device to yield the reference voltage (V_{Ref}). Assuming the transistors in Figure 3 operate in saturation, the self-bias V_{FGS} and beta-multiplier circuits will generate the currents I_{B1} and I_{B2}, as in (1) and (2) [21], [22].

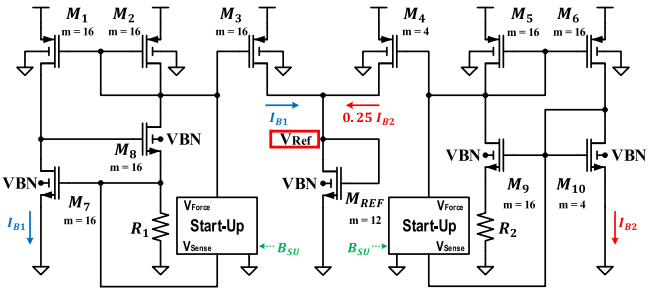


FIGURE 3. Voltage reference based on cryogenic V_{th} saturation.

These currents are copied and supplied to M_{REF} via M_3 and M_4. Consequently, V_{Ref} can be approximated by means of (3).

$$I_{B1} = \frac{V_{GS7}}{R_1} = \frac{V_{th} + V_{ov7}}{R_1} \approx \frac{V_{th}}{R_1} \tag{1}$$

$$I_{B2} \approx \frac{L}{2 \cdot R_2^2 \cdot \mu C_{ox} \cdot W} \tag{2}$$

$$V_{Ref} \approx \sqrt{\frac{(I_{B1} + 0.25 \cdot I_{B2}) \cdot 2 \cdot L}{\mu C_{ox} \cdot W}} + V_{th} \tag{3}$$

So as to improve the circuit noise performance, an RC low-pass filter assembled with off-chip components and with a 5.2 Hz cut-off frequency, is added to its output (not shown in Figure 3); R_{Fil} = 32.4 kΩ (metal film) and C_{Fil} = 940 nF (C0G). The voltage reference circuit is simple and does not employ calibration techniques to improve its V_{Ref} drift over temperature. It relies on the fact that a constant current biases and saturates the diode connected NMOS (M_{REF}), while the circuit is operated inside the V_{th} saturation temperature region (6 K – 50 K). This is a common situation for ICs intended to be used in large scale QC systems, since they are placed close to the physical quantum bits at environmental temperatures between 4 K and 10 K. Although self-heating is a concern at cryogenic temperatures, its effect is also proportional to the electrical power dissipated by the devices [23], [24], [25]. Due to its low power dissipation, estimated to be 70 µW during the circuit design flow, a negligible self-heating is expected from this circuit. Additionally, start-up circuits are used to prevent the current sources from latching-up. They can either operate autonomously or be manually triggered through configuration bits via the JTAG interface.

The measured response of a prototype reference circuit to a supply voltage (V_{Sup}) sweep at 6 K, is shown in Figure 4. The output voltage (V_{Ref}) and supply current consumption (I_{Sup}) indicate that the circuit starts operating at V_{Sup} = 1.25 V with V_{Ref} = 576 mV and I_{Sup} = 38.3 µA. Besides, this operation condition is reached once the start-ups are no longer forcing the gates of the M_1-M_6 transistors to ground, as to prevent a zero current condition in the beta-multiplier and self-bias V_{FGS} circuits. Hence, the start-ups action is noticed as a swift increment of V_{Ref} and I_{Sup} in Figure 4, when V_{Sup} is between 1 V-1.2 V. Once the V_{FGS} of M_7 and M_{10} have reached saturation levels due to enough V_{Sup} available for the

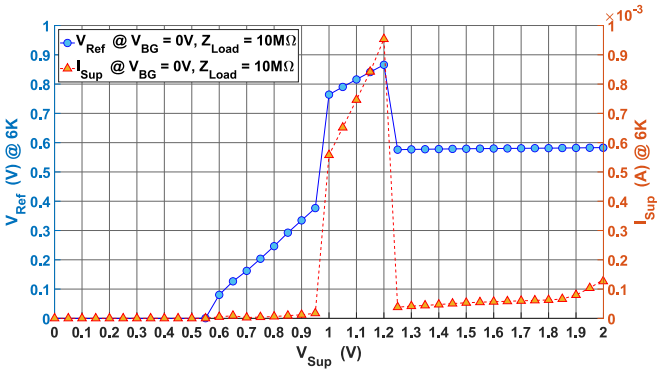


FIGURE 4. Measured output voltage and current consumption of voltage reference (sample 1) with respect to supply voltage (V_{Sup}), at 6 K.

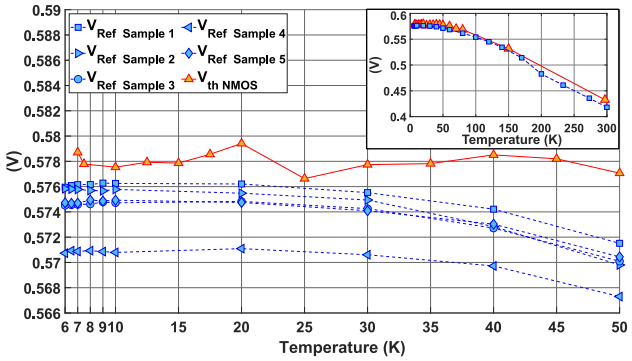


FIGURE 5. Measured output of voltage reference over the temperature range of interest (6 K – 50 K), with $V_{Sup} = 1.25$ V and $V_{BG} = 0$ V. The results correspond to 5 sample chips. Extracted V_{th} of I/O NMOS is added for comparison. Inset displays sample 1 data over a wider range (6 K – 300 K).

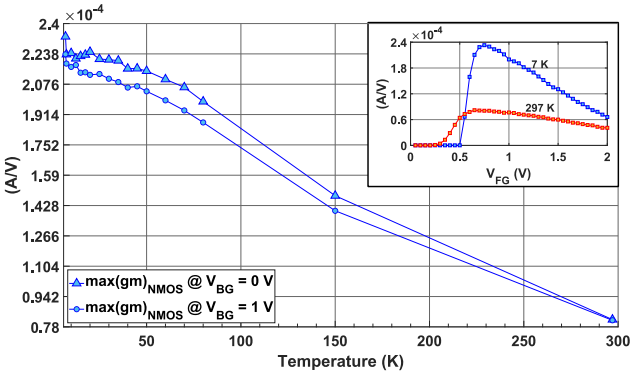


FIGURE 6. Maximum g_m of the I/O NMOS (W / L = 1 μm / 0.32 μm) over temperature, for $V_{BG} = 0$ V and $V_{BG} = 1$ V. Inset displays the g_m versus V_{FG} curve for 297 K and 7 K, at $V_{DS} = 0.1$ V and $V_{BG} = 0$ V.

circuits operation, the start-ups stop forcing the M_1-M_6 gates to ground, as the zero current condition has been prevented.

Figure 5 shows the measured V_{Ref} over temperature, together with the V_{th} extracted from the I/O NMOS device (Figure 2). As can be observed, V_{Ref} of sample 1 follows a trend similar to the one of the I/O NMOS V_{th} and deviates on average by 2.5 mV from it at temperatures between 6 K to 50 K. A total of 5 reference circuits, embedded in different ICs, are tested. The responses of these samples are shown in Figure 5 and they differ slightly between each other, but all follow the I/O NMOS V_{th} trend over temperature. Hence, these measurements demonstrate the reference feasibility at environmental temperatures between 6 K and 50 K.

B. TRANSCONDUCTANCE INCREASE

Another electrical characteristic that changes in a MOS transistor facing cryogenic temperatures is its g_m [15]. Figure 6 shows the maximum g_m values obtained from the super-low V_{th} I/O NMOS device at different temperatures. As can be noticed, the device maximum g_m value increases by 184 % at 7 K, when compared to its value at 297 K. A similar scenario occurs when the device back gate is set to 1 V, but with a slight reduction of its maximum g_m value. The g_m increase at cryogenic temperatures is linked to the carriers mobility increase due to reduced phonon scattering, while the shape change in the g_m vs V_{FG} curve (Figure 6, inset) is due to the Fermi-Dirac distribution exponential scaling [19]. As reported by [20], the cryogenic g_m increase phenomenon is expected in NMOS and PMOS devices of the 22 nm FDSOI technology.

In order to study the effects that the cryogenic g_m increase phenomenon has on an analog circuit, a linear voltage regulator is used as a test vehicle. Its circuit diagram is shown in Figure 7 (a). If this circuit uses a high gain amplifier, its regulated DC output voltage can be approximated as in (4).

$$V_{Reg} \approx V_{IN\,Ref} \cdot \frac{R_{F1} + R_{F2}}{R_{F2}} \tag{4}$$

The regulator employs an NMOS pass element whose back-gate terminal connection can be changed by an analog multiplexer controlled via JTAG interface. In this way it is possible to compensate for the V_{th} increase experienced by the pass element at cryogenic temperatures and to reduce the supply voltage level required by the regulator to start its operation. Although the use of an NMOS pass element will lead to a higher dropout voltage in contrast to a PMOS, it will also provide a superior power supply rejection ratio (PSRR); a requirement needed to supply high performance analog circuits [26]. Additionally, the feedback resistors values (R_{F1} and R_{F2}) can be modified for output voltage tuning via JTAG programming. Moreover, an off-chip compensation network with temperature stable electrical parameters, made up of a metal film resistor ($R_{C1} = 6.25\,\Omega$) and a polyphenylene-sulphide film capacitor ($C_{C1} = 47$ nF), is used for cryogenic stability [27].

The differential amplifier of the regulator, shown in Figure 7 (b), employs voltage followers for level shifting at their inputs and a resistive local common mode feedback at its core. Its open loop gain (A_{DA}) is approximated by (5) [28]. Since the regulator loop gain (A_{LG}) is proportional to A_{DA} as in (6), the load regulation (LR) and power supply rejection ratio (PSRR) are also depending on A_{DA} via A_{LG}; (7) and (8) [26]. As A_{DA} is proportional to the g_m of the MOS devices, it is expected that at cryogenic temperatures its

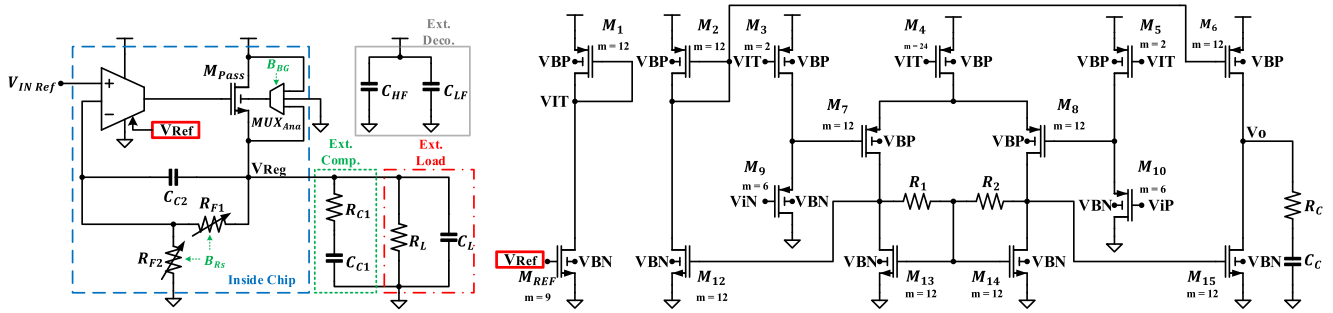


FIGURE 7. Linear voltage regulator. (a) The circuit is composed of an error amplifier, an NMOS pass element, a multiplexer and a resistive feedback network. Off-chip compensation elements (metal film R_{C1} and polyphenylene-sulphide C_{C1}), with stable electrical characteristics over temperature, are used to guarantee stability at cryogenic temperatures. (b) Differential amplifier in regulator; its tail current is biased by the reference circuit (Figure 3).

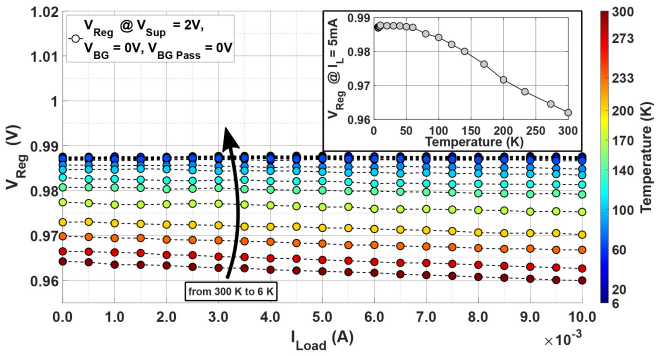


FIGURE 8. Measured regulator output voltage (V_{Reg}) in relation to current load (I_{Load}) and temperature; $V_{IN\ Ref} = 0.5$ V, $R_{F1} = R_{F2}$, $V_{BG} = 0$ V and $V_{Sup} = 2$ V. Inset shows V_{Reg} versus temperature; $I_{Load} = 5$ mA.

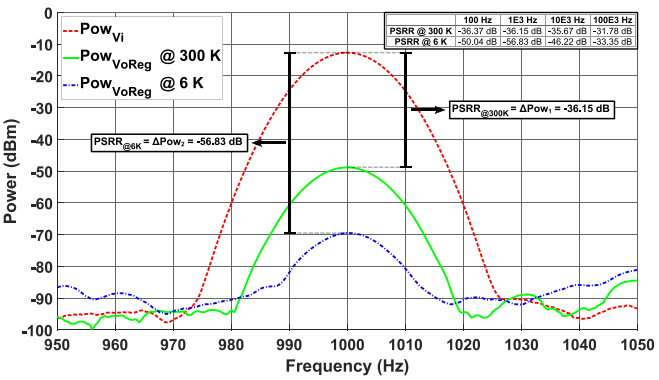


FIGURE 9. Measured regulator PSRR via spectrum analysis at 1 kHz, at 6 K and 300 K; $V_{IN\ Ref} = 0.5$ V, $R_{F1} = R_{F2}$, $V_{BG} = 0$ V, $V_{Sup} = 2$ V.

magnitude increases due to the g_m increase with temperature reduction. This results in an improvement of the regulator LR and PSRR.

$$A_{DA} \approx g_{m7,8} \cdot g_{m12,15} \cdot (R_{1,2} || r_{o7,8} || r_{o13,14}) \cdot Z_{out} \quad (5)$$

$$A_{LG} \approx A_{DA} \cdot \frac{R_{F2}}{R_{F1} + R_{F2}} \quad (6)$$

$$LR \approx \frac{1}{g_{mM\ Pass} \cdot A_{LG}} \quad (7)$$

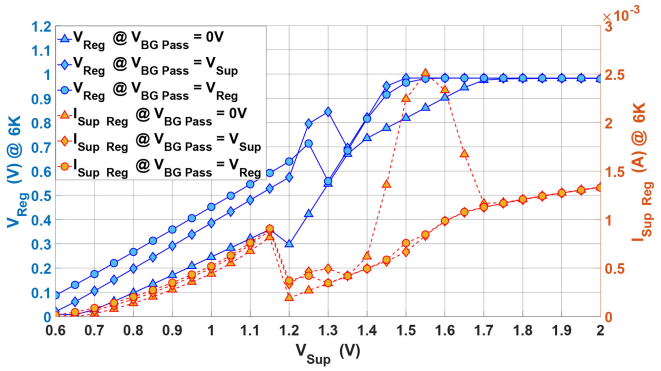


FIGURE 10. Measured regulator output voltage (V_{Reg}) and supply current ($I_{Sup\ Reg}$) at 6 K, in relation to supply voltage (V_{Sup}) and several back gate settings for the NMOS pass element.

$$PSRR \approx \frac{1}{g_{mM\ Pass} \cdot r_{oM\ Pass} \cdot A_{LG}} \quad (8)$$

Figure 8 shows the measured response of the prototype regulator in relation to load current (I_{Load}) and temperature, with $V_{IN\ Ref} = 0.5$ V, $R_{F1} = R_{F2}$, $V_{BG} = 0$ V and $V_{Sup} = 2$ V. $V_{IN\ Ref}$ is set to 0.5 V by means of an external voltage source in order to evaluate the regulator performance with regard to temperature. The mean regulator output voltage (V_{Reg}) is 962 mV at 300 K and it increases to 987 mV at 6 K. These changes indicate that an increase in A_{LG} reduces the regulator error and sets V_{Reg} closer to 1 V, the ideal output value. However, due to the amplifier input offset voltage, $V_{Reg} \neq 1$ V. Similarly, the regulator LR changes from 424mV/A at 300K, to 30mV/A at 6K; an improvement of 92.92 %. The regulator PSRR is shown in Figure 9 for 1 kHz, at 300 K and 6 K. At 300 K, the measured PSRR is −36.15 dB, while at 6 K it is −56.83 dB, corresponding to an improvement of 20.68 dB. The inset in Figure 9 indicates the measured PSRR for additional frequencies. Based on the measurements results previously described and (5) – (8), it can be inferred that the g_m increase is the main factor responsible for the cryogenic improvement of the regulator LR and PSRR.

Furthermore, Figure 10 shows the regulator response to a voltage supply sweep at 6 K, with different pass element back-gate configurations. With the back-gate set to ground, the regulator needs $V_{\text{Sup}} = 1.75$ V to start operation. In contrast, by setting the back-gate to the supply rail, the regulator needs $V_{\text{Sup}} = 1.5$ V to operate. Hence, a reduction of 250 mV is obtained. The regulator has an idle power consumption of 3.3 mW. Most of this consumption is produced by the enforced operation of the pass element in saturation due to cryogenic stability concerns, while our design estimations indicate that the error amplifier consumes 0.1 mW. An improvement in power consumption can be achieved by incorporating cryogenic simulation models into the regulator design flow. Unfortunately, cryogenic simulation models have not been available for the development of the prototype chip presented in this paper. Despite this, the regulator operates at temperatures between 6 K and 300 K.

C. LOW FREQUENCY EXCESS NOISE

In electronics, noise is defined as any electrical signal present in a circuit other than the desired signal, and is considered an undesired phenomenon since it can disrupt the functionality of a circuit [13]. Regarding cryogenic ICs for QC, it is expected that MOS transistors will produce most of their intrinsic noise. Moreover, since the noise produced by these ICs may interfere with the qubit devices operations, the study of the MOS transistor cryogenic LF noise has gained relevance [29], [30], [31].

According to Ghibaudo et al., the MOS transistor LF noise is dominated by the carrier number fluctuation and the mobility fluctuation phenomena, with a linear temperature dependence [32]. Therefore, a decrease of the MOS transistor LF noise is expected with temperature reduction. However, it has been found that this is not the case for temperatures lower than 100 K. A higher amount of LF noise has been measured at 4 K than at 300 K in FDSOI and planar-bulk MOS technologies [10], [11]. Moreover, it was recently demonstrated that at 2.5 K the LF noise is correlated with the MOS transistor oxide-Si interface traps density [30]. These traps produce energy states localized near the conduction-band, which at cryogenic temperatures have a strong interaction with the Fermi energy level. Hence, the capture and release of charge carriers induced by these traps substantially contribute to the MOS transistor LF noise.

Even though the mechanism generating the cryogenic LF excess noise has been identified, a model that can describe it has not been developed. On this basis, it is logical to assume that the LF noise produced by analog MOS circuits developed in 22 nm FDSOI is higher at cryogenic temperatures than at room temperature. However, how much difference exists between the LF noise spectra produced by a circuit operated at these temperatures is unknown. So as to shed light on this uncertainty, the LF noise produced by our prototype circuits is characterized at 8 K and 300 K. Moreover, while performing the characterization

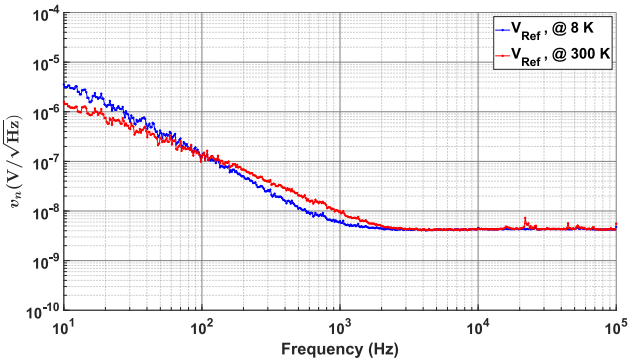


FIGURE 11. Voltage noise amplitude spectral density measured from the voltage reference circuit output at 8 K and 300 K; $V_{BG} = 0$ V and $V_{Sup} = 2$ V.

of the intrinsic LF noise from the prototype circuits, the ground isolation approach described in Section II is used.

Due to the voltage reference circuit limited current drive capability and the noise measurement equipment input characteristics (E5052B, with $C_{\text{in}} = 1410\,\mu$F and $R_{\text{in}} = 50\,\Omega$ for AC coupling), a low noise amplifier (SR560, with $C_{\text{in}} = 25$ pF, $R_{\text{in}} = 100$ MΩ and $R_{\text{out}} = 50\,\Omega$) is added to the noise measurement setup as intermediate stage. Additionally, the SR560 has a 1 MHz bandwidth and an average input noise voltage amplitude spectral density of $4\,^{\text{nV}}/\sqrt{Hz}$, when set to a voltage gain of 60 dB. Figure 11 shows the voltage noise spectra measured at the output of the voltage reference circuit while operated at 8 K and 300 K. As can be observed, for low frequencies the voltage amplitude spectral density produced by this circuit at 8 K is higher than the one at 300 K. The difference between both spectra can be quantified by means of their RMS voltage noise defined at the 10 Hz – 10 kHz LF bandwidth, as indicated by (9). Beyond 10 kHz both spectra are covered by the measurement equipment noise floor. It suffices to mention that the measured noise spectra are integrated by means of the trapezoidal numeric method. As a result, $V_{\text{Ref, n @ 8 K}} = 9.08\,\mu\text{V}_{\text{rms}}$ and $V_{\text{Ref, n @ 300 K}} = 4.73\,\mu\text{V}_{\text{rms}}$, indicating that the LF noise at 8 K is 1.92 times higher than the one at 300 K.

$$V_{\text{n,rms}} = \sqrt{\int_{f_1}^{f_2} v_n^2(f)\,df} \tag{9}$$

Concerning the voltage regulator, since this circuit can drive the input port of the E5052B, it does not require the SR560 as an intermediate stage. Figure 12 shows the voltage noise spectra measured from the regulator output at 8 K and 300 K. Similarly to the previous case, in the LF bandwidth the noise spectrum at 8 K is higher than the one at 300 K. Though, around 10 kHz both spectra reach similar values and at higher frequencies the 8 K noise spectrum is lower than the 300 K one. This behavior signals a reduction of the LF noise and an increase of the white noise impact in the voltage noise spectrum at 8 K, since for $f > 10$ kHz the voltage noise reduces with temperature reduction; electrical white noise in MOS devices

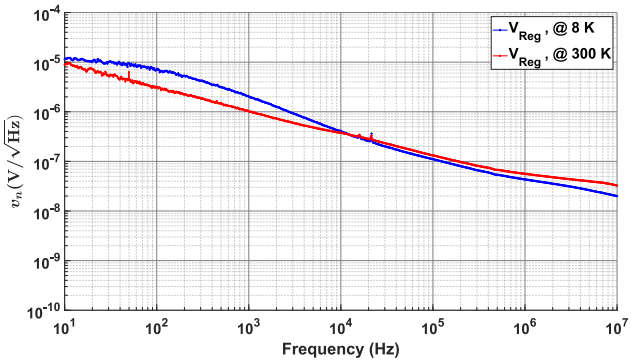


FIGURE 12. Voltage noise amplitude spectral density measured from the voltage regulator circuit output at 8 K and 300 K; $V_{IN\ Ref} = 0.5$ V, $R_{F1} = R_{F2}$, $V_{BG} = 0$ V, $I_{Load} = 5$ mA and $V_{Sup} = 2$ V.

TABLE 1. Measured RMS voltage noise values in the study.

BW	10 Hz – 10 kHz		10 Hz – 10 MHz	
Temp.	8 K	300 K	8 K	300 K
$V_{Ref,n}$	9.08 μV_{rms}	4.73 μV_{rms}	N.A.	N.A.
$V_{Reg,n}$	157.90 μV_{rms}	83.97 μV_{rms}	194.79 μV_{rms}	173.39 μV_{rms}

reduces with temperature reduction [31]. By evaluating the regulator RMS voltage noise at the LF bandwidth via (9), it is found that $V_{\mathrm{Reg,n\ @\ 8\,K}} = 157.90\,\mu V_{rms}$ and $V_{\mathrm{Reg,n\ @\ 300\,K}} = 83.97\,\mu V_{rms}$. The regulator LF noise at 8 K is 1.88 times higher than the one at 300 K. It is worth noting that in both circuits the LF RMS voltage noise increases roughly by 90 % at 8 K, when compared to its value at 300 K. This correlates with the cryogenic LF excess noise behavior reported for FDSOI transistors [10]. Table 1 provides a summary of the RMS noise values measured in this study.

D. DISCUSSION

The cryogenic V_{th} increase is a phenomenon experienced by all the cryogenic analog MOS circuits. Thus, their voltage supply requirements becomes higher. This situation will encourage the use of low voltage supply circuit techniques in cryogenic analog systems [33]. In the case of circuits based on FDSOI MOS transistors, back-gate V_{th} tuning is an effective way for the voltage supply requirements reduction of the cryogenic analog MOS circuits. This is demonstrated by the linear voltage regulator studied in Section III-B. Regarding bulk-MOS technologies, V_{th} tuning at cryogenic temperatures can be achieved via the forward body biasing [34]. Therefore, it is expected that the next generation of cryogenic analog MOS circuits uses the V_{th} tuning as a fundamental circuit technique. Concerning the cryogenic V_{th} saturation, although it can be used as working principle for the generation of a reference voltage, its use also involves some limitations. For instance, the measurement results provided in Section III-A indicate that the reference circuit is sensible to process variations. In addition, the cryogenic V_{th} saturation may not occur in all the MOS technologies. Hence, the development of a robust cryogenic voltage reference circuit demands the use of a MOS technology that has been characterized and modeled for cryogenic operation.

TABLE 2. Voltage reference comparison with the state of the art.

	[37]	[38]	[39]		This work
Technology	SiGe BiCMOS	40 nm CMOS	40 nm CMOS		22 nm FDSOI
Ref. device	SiGe HBT	DTMOS	PMOS	DTMOS	NMOS
Temp. operation range	0.7 K – 293 K	4 K – 300 K	4 K – 300 K	4 K – 300 K	6 K – 50 K
$V_{Sup.}$ min.	3.3 V	1.8 V	0.97 V	0.9 V	1.25 V
$V_{Ref.}$	1.156 V @ 0.7 K	0.81 V @ 4 K	0.71 V @ 4 K	0.6 V @ 4 K	0.576 V @ 6 K
Pow. cons.	130.35 µW	132 µW	7.37 µW	7.26 µW	47.88 µW
Line regulation	N.A.	8.3 %/V	1.2 %/V	1.1 %/V	1.652 %/V
Temp. coefficient	160 ppm/K	834 ppm/K	539 ppm/K	436 ppm/K	300 ppm/K
PSRR	N.A.	−23.4 dB	N.A.	N.A.	−46.14 dB @ 6 K, 1 kHz
Low frequency RMS noise	N.A.	N.A.	N.A.	N.A.	9.08 μV_{rms} @ 8 K, 10 Hz – 10 kHz
Area	N.A.	0.0004 mm^2	0.009 mm^2	0.009 mm^2	0.006 mm^2

The g_m increase experienced by MOS devices at cryogenic temperatures is a phenomenon that can be used to increase the gain of cryogenic amplifiers, as demonstrated by the results presented in Section III-B. However, for many amplifier topologies the gain is not the only electrical parameter relying on g_m; e.g., the circuit stability may also be influenced by it [35]. Therefore, a sensitivity analysis of the circuit parameters with regard to higher g_m values must also be included into the design process of cryogenic amplifiers.

Regarding the LF excess noise, based on the information available in the state of the art literature and the results presented in Section III-C, is clear to us that it will affect most of the cryogenic analog MOS circuits. Hence, the LF excess noise can become a hindering performance factor for many circuit blocks in cryogenic analog and mixed-signal ICs; e.g., current biases and voltage references circuits. Potentially influencing the performance of applications like quantum dot formation in semiconductor qubits, where DC voltages generated at cryogenic temperatures are supplied to the gates of the qubit devices [36]. Consequently, low noise circuit techniques and topologies must be implemented to counteract this cryogenic MOS phenomenon.

A comparison between the circuits studied in this paper and the state of the art is provided in the Tables 2 and 3 [27], [37], [38], [39]. The voltage reference in this work is simple and has a competitive temperature coefficient of 300 ppm/K, when operated in the 6 K – 50 K range. Moreover, its PSRR is −46.16 dB at 6 K, while its LF RMS voltage noise is 9.08 μV_{rms} at 8 K. Regarding this work voltage regulator, its LR, PSRR, and LF RMS voltage noise metrics fall behind the state of the art performance. However, the solutions presented in [27] rely on discrete components and need at least 3.3 V of voltage supply. In contrast, this work regulator operates with lower V_{Sup} and, excluding the compensation network, its components are integrated on chip. In addition, it is important to highlight that the regulator presented in this work can operate along the 6 K – 300 K range, a feature not common in commercial monolithic regulators [27].

TABLE 3. Voltage regulator comparison with the state of the art.

	[27]		This work
Technology	Discrete components based design		22 nm FDSOI
Pass element	NMOS (TSM2314)		NMOS
Nominal $V_{Sup.}$	VDD = 3.3 V (Error amplifier) VIN = 1.5 V (Pass element)		2 V
Error amplifier	AD8605	TLV271	Custom
$V_{Reg.}$	1.0086 V @ 4 K, $V_{Ref.}$ = 0.6 V, Z_{Load} = 100 Ω	1.0106 V @ 4 K, $V_{Ref.}$ = 0.6 V, Z_{Load} = 100 Ω	0.987 V @ 6 K, $V_{Ref.}$ = 0.5 V, I_{Load} = 5 mA
Idle pow. cons.	4.46 mW @ 4 K	0.1 mW @ 4 K	3.3 mW @ 6 K
Max. load current	300 mA @ 4 K	300 mA @ 4 K	10 mA @ 4 K
Load regulation	1.59 mV/A @ 4 K	0.81 mV/A @ 4 K	22 mV/A @ 6 K
PSRR	−75.1 dB @ 4 K, 1 kHz	−76.4 dB @ 4 K, 1 kHz	−56.83 dB @ 6 K, 1 kHz
Low frequency RMS noise	2.64 μV_{rms} ★ @ 4 K, 100 Hz – 100 kHz	7.03 μV_{rms} ★ @ 4 K, 100 Hz – 100 kHz	157.90 μV_{rms} @ 8 K, 10 Hz – 10 kHz
Area	N.A.	N.A.	0.075 mm^2

★Values calculated from data depicted in a graphical format.

Finally, the circuits studied in this work served as test vehicles for gaining an insight into the design and electrical characterization of cryogenic analog MOS ICs. This allows us to get the knowledge required for the development of optimized cryogenic analog circuits.

IV. CONCLUSION

In this paper, the design and cryogenic electrical characterization of a voltage reference and a linear voltage regulator, are presented. The circuits are developed in 22 nm FDSOI and are used for the cryogenic performance evaluation of this technology. We demonstrated that the cryogenic V_{th} increase and the subsequent increase in voltage supply requirements of the cryogenic analog MOS circuits can be countered with the V_{th} tuning technique via the back-gate terminal of the FDSOI MOS transistors. This work also showcased the use of the cryogenic V_{th} saturation exhibited by the I/O NMOS device, settled to 578 mV in the 6 K – 50 K range, as a working principle for the production of a cryogenic voltage reference. The effect that the g_m increase has on a voltage regulator performance is also observed in this work, and it directly improves the circuit LR and PSRR. The occurrence of the LF excess noise is observed in our test circuits. In both circuits, the LF RMS voltage noise increased by 90 % at 8 K, with respect to 300 K. This highlights the need for the adoption of low noise design techniques in cryogenic applications that are sensible to the LF noise. Essentially, we consider that the 22 nm FDSOI technology has MOS transistors whose electrical characteristics are suitable for the development of cryogenic analog MOS circuits that are intended to be used in QC applications. In the end, we expect that the information and outcomes provided by this paper support the advancement of the cryogenic analog MOS circuit design discipline.

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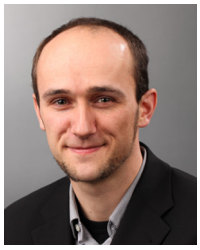

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