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An Ultra-Wideband Reference Frequency Chirp Generator Utilizing Fractional Frequency Divider With High Linearity

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ABSTRACT Using physically separated multiple-input multiple-output (MIMO) systems for millimeter-wave measurement systems based on linear frequency chirps poses unique challenges for generating a modulated reference chirp to apply high coherence. The reference frequency chirp is crucial for the measurement accuracy of the overall system and should feature high bandwidth, low phase noise, and high linearity. For this reason, we present a novel architecture combining a fixed-integer phase-locked loop (PLL) with a fast-modulated frequency divider. Thus, modulated output frequencies of up to 2 GHz with an adjustable bandwidth of up to 1.75 GHz are achieved while maintaining low phase noise of −140 dBc/Hz at 1 MHz from the carrier at the center frequency. Synchronous programming and modulation of the fractional frequency divider is done by a new type of control utilizing fast transceivers in a field-programmable gate array (FPGA), which does not require back-synchronization to the frequency divider. Measurements with the novel reference frequency chirp generator combined with a V-band PLL reveal a low RMS linearity error of 0.67 ppm of the reference chirp for a chirp duration of 1 ms and a bandwidth of 363 MHz.

INDEX TERMS Chirp modulation, FMCW, MIMO systems, signal generator, ultra-wideband radar.

I. INTRODUCTION

MICROWAVE and millimeter-wave (mm-wave) measurement systems based on linear frequency chirps are widely used in applications such as vector signal analysis [1], material characterization [2], [3], and imaging [4]. Generating a frequency chirp is one critical factor for the overall performance of the measurement system. The frequency chirp limits the measurements' precision, resolution, and accuracy due to linearity, bandwidth, and phase noise [5]. Moreover, the frequency chirp should be fast to achieve high measurement repetition rates. In recent times, it has been shown that using multiple-input multiple-output (MIMO) systems provides additional information and saves time during the measurements [6], [7]. Depending on the application, the MIMO systems can be integrated on a single chip [8] or with entirely physically separated channels, as is the case in tomography systems [9]. In the case of separated channels, the generation and distribution of the chirps are challenging due to the need to establish a sufficiently high coherence between the separated transmitting (TX) and receiving (RX) modules. Generating the mm-waves directly at the antenna's port is advantageous, as losses in the connections and cables result in a high attenuation of a high-frequency signal. Hence, a signal with a much lower frequency, either mono or modulated, is distributed and passed to each module as a reference for multiplication. Nevertheless, the reference chirp generator must provide a high bandwidth in the baseband to keep the multiplication factor in the subsequent TX and RX modules low. This results in a reduction of the phase noise at the antenna's

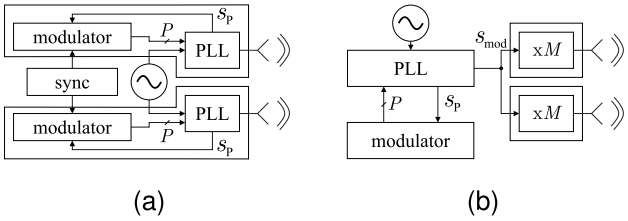

FIGURE 1. Common approaches for generating synchronized and coherent linear frequency chirps in MIMO systems based on phase-locked loops.

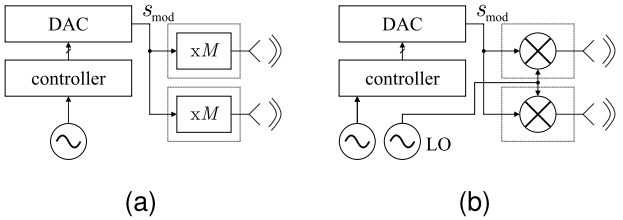

FIGURE 2. Common approaches for generating synchronized and coherent linear frequency chirps in MIMO systems based on DDS.

output [10] and increases the linearity [11]. Fig. 1 and Fig. 2 show four common approaches for generating the mm-wave chirp. Only two modules are shown in this example, but this can be scaled to more units.

The first approach shown in Fig. 1(a) uses a fixed reference frequency. The modules consist of one phase-locked loop (PLL) per module with an integrated modulator. The PLL's output frequency is the transmit frequency in the mm-band and is mainly limited by the voltage-controlled oscillator (VCO). The PLL is capable of ultra-wideband, low noise, and highly linear chirps in combination with the integrated modulator [12]. The fixed reference frequency, generated by an oscillator for all modules, operates in the sub-GHz range. Thus, the distribution via coaxial cable is feasible. The integrated modulator is responsible for the frequency chirp generation. It changes the frequency divider ratio P in the PLL feedback path on each edge of its output s_P. The synchronizer triggers each modulator at the same time. In addition to a common reference frequency, additional control and feedback channels are required to set each modulator to the same initial state. Otherwise, each PLL will have different start phases with each frequency chirp. This results in a high overall hardware cost, which increases with the number of modules, respectively.

The second approach is the modulation of the reference signal for all modules, as depicted in Fig. 1(b). A fixed oscillator is fed into a primary PLL, in which the feedback divider is modulated to generate the frequency chirp in the range of sub-GHz to a few GHz. This modulated reference frequency chirp is distributed to all modules and multiplied to the desired output frequency by PLLs or multiplier chains [9]. This concept minimizes routing complexity and offers higher coherence between the channels with decreased phase noise performance [13]. Nevertheless, in order to produce frequency chirps within the lower GHz range, it is necessary to employ a low input reference frequency to ensure achievable division ratios in the feedback path of the PLL. The low input frequency leads to fewer comparison operations in the phase frequency detector (PFD) and, thus, inevitably reduces the chirps's linearity. In addition, the increasing modulation's quantization noise increases the chirps' overall phase noise [11].

The third approach utilizes direct digital synthesis (DDS) in the reference path as depicted in Fig. 2(a). The DDS consists of an oscillator with a fixed clock frequency, a controller containing the phase accumulator and phase-to-amplitude converter, and a digital-to-analog converter (DAC). A reference frequency chirp, synthesized by the DDS in the baseband range, is distributed to the modules. Like the second approach, the frequency chirp is converted to the desired output frequency [14]. The limiting factor of this approach is the DAC. A trade-off exists between high spurious-free dynamic range (SFDR) and high output frequency. A DAC with a high SFDR but low output frequency needs high multiplication factors in the modules to provide the desired output frequency chirp. This harms the overall phase noise of the system.

The fourth approach uses a mixer in each module, as depicted in Fig. 2(b). Again, a DDS produces the low-frequency reference chirp, passed to a mixer in the transmit modules. Utilizing the mixers, another fixed-frequency LO shifts the frequency chirp to the desired output frequency for all transmit modules. This LO operates in the upper GHz range. Due to the high LO frequency, the distribution is still challenging. Moreover, the bandwidth of the chirp is considerably limited by the DAC's bandwidth, as the reference chirp is not multiplied in frequency to reduce the phase noise of the output chirp [15].

Our article presents a novel method for generating highly linear frequency chirps with low phase noise and high bandwidth using a new feed-forward architecture, addressing the limitations observed in previous systems. The innovative system revolves around utilizing a PLL in the reference path to generate a high input frequency, achieving low phase noise through a custom PLL monolithic microwave integrated circuit (MMIC). This high reference frequency is then modulated using a new custom frequency divider, ensuring excellent linearity in frequency chirp generation owing to the high input frequency. To fulfill the requirements for high frequency and modulation bandwidth, we will present a novel solution for synchronizing an FPGA during a frequency chirp. This solution enables the flexible reprogramming of the frequency divider, facilitating adjustments to effective bandwidth, chirp time, and modulation type as needed. Our approach delivers the highest effective modulation frequency of 2 GHz, exceptional linearity of 0.67 ppm, and the lowest phase noise compared to other chirp generators in the baseband [16], [17], [18], [19]. This is achieved through a combination of custom integrated circuits and precise synchronization based on emulating the fast frequency divider. The focus is on the novel system creating highly

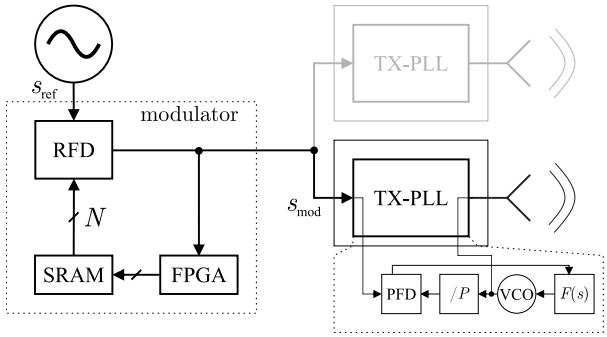

FIGURE 3. Closed-loop approach for generating linear frequency chirps by modulating a frequency divider in the reference path.

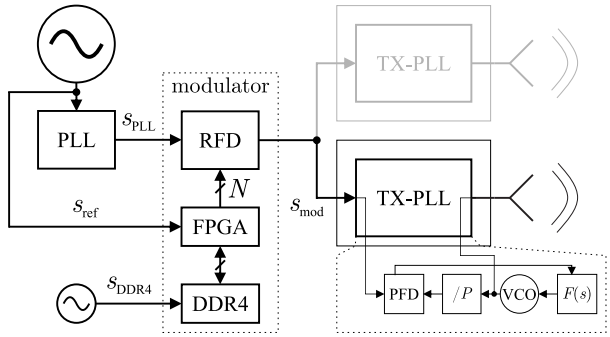

FIGURE 4. New open-loop approach for generating linear frequency chirps by modulating a frequency divider in the reference path.

linear frequency chirps in the baseband, referred to hereafter as the chirp generator, which will then be translated to the desired mm-wave range using a TX-PLL.

The subsequent sections are arranged as follows. First, the basic functional principle of modulating a frequency divider in the reference path is discussed. It also points out the limitations of achieving even higher frequencies. Subsequently, the new overall system architecture is presented. The new feed-forward concept is explained in detail, and all necessary hardware components are discussed. The fourth section contains the realization of the final chirp generator, including all hardware components. Subsequently, it is explained how linear frequency chirps are mathematically realized for the system concept. Finally, the chirp generator is fully characterized by measurements and compared to simulations. In addition, we prove the suitability of the chirp generator on a real TX-PLL for generating mm-waves.

II. BASIC CONCEPT

In [20], we first presented a new concept for generating a high linear frequency chirp based on a closed-loop approach, shown in Fig. 3. A commercial signal generator provides a fixed frequency to a high-frequency divider called the reference frequency divider (RFD). The modulated output of the RFD s_{mod} is fed into a clock input of a field programmable gate array (FPGA). On each rising edge of this clock, a precalculated division ratio N is fetched from a static random-access memory (SRAM) and is directly provided to the RFD, to modulate the incoming signal s_{ref} of the signal generator. The FPGA uses the modulated clock s_{mod} for the overall logic. Besides the high costs and low integration level, the signal generator limits the input frequency and, thus, the chirp linearity. Moreover, the clock frequency of the modulator is determined due to the utilized memory and the I/O ports of the FPGA. This corresponds to a low modulation bandwidth with a limited maximum reference frequency for the TX-PLL. The TX-PLL's frequency division ratio P must be increased for compensation. However, the generated phase noise in the TX-PLL transferred to the phase noise at the output is proportional to the division ratio P of the feedback frequency divider [21].

Faster memory and I/O ports are required to increase the modulation bandwidth. Calculating the required division ratios for the RFD is computationally complex and cannot be done in real time. Therefore, these must be temporarily stored in a fast memory. The memory speed and the I/O ports limit the effective modulation frequency of the RFD, as a new division ratio must be applied to it after each clock cycle of the RFD. In addition, the memory must be large enough to store many division ratios to guarantee long modulations. This can be achieved by using DDR4 memory. However, DDR4 memory can only deliver data at a fixed output frequency due to the need to use a separated fixed frequency clock s_{DDR4}. It can not provide data synchronized with the signal s_{mod}. Moreover, the FPGA's I/O ports are another limiting factor. These ports have a typical maximum data rate of around 500 Mbit/s. Modern FPGAs offer transceiver channels for much higher data rates. These consist of serializers with built-in PLLs. The maximum capable data rate is up to 58 Gbit/s. Due to the built-in PLLs of the transceiver channels in the FPGA, a frequency-modulated clock input can not be used. So, the RFD output s_{mod} can not be fed back into the FPGA, and the closed-loop concept cannot be used. Therefore, the FPGA and the DDR4 memory must be synchronized using the unmodulated input signal of the RFD. This makes synchronized and correctly timed programming of the RFD more demanding than for the closed-loop concept.

To avoid all these problems, a novel system has been developed. Fig. 4 shows the basic approach for generating a high linear frequency chirp in an open-loop configuration, from now on called a feed-forward system. A stable fixed-frequency oscillator s_{ref} is fed into a PLL to multiply the input frequency into the upper GHz range and into the FPGA as reference. In contrast to the system in Fig. 3, it can be seen that the FPGA now operates with the fixed reference signal s_{ref}. The output of the PLL s_{PLL} is forwarded to the RFD. The common reference ensures the synchronization of the FPGA with the RFD. The FPGA compensates for a slight phase misalignment caused by the PCB traces. The asynchronous DDR4 memory is synchronized using the FPGA, and previously stored $\Delta\Sigma$-modulated division ratios

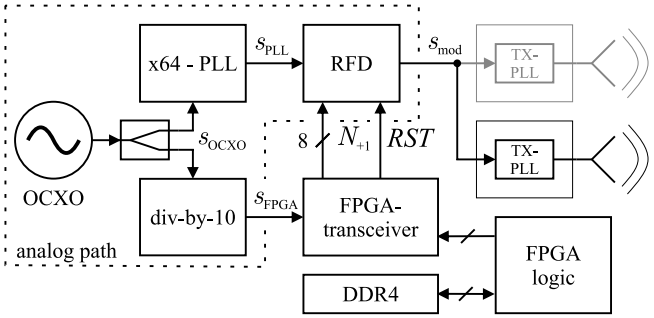

FIGURE 5. Architecture of the new chirp generator in a feed-forward design using synchronized high-speed transceivers in an FPGA and DDR4 memory based on an open-loop approach.

for the frequency chirp are forwarded to the RFD via fast transceiver outputs. It can be seen that the output of the RFD is not synchronized back to the FPGA.

Due to the high frequency provided by the PLL in combination with the modulated division ratios for the RFD, a high-frequency resolution and, thus, a highly linear frequency chirp in the range of sub-GHz to a few GHz can be achieved. Finally, the reference chirp is multiplied by the factor P in the TX-PLL to generate the desired output frequency and filter out the remaining quantization noise.

This concept offers many benefits. The reference frequency can be easily distributed, and low phase noise is achieved due to the use of PLLs [22], [23]. A nearly perfect chirp is generated due to the use of a $\Delta\Sigma$-modulator, and marginal spurs appear due to the binary output of the RFD. The additional noise generated by the $\Delta\Sigma$-modulator does not contribute to the phase noise at TX-PLL's output. As it exhibits a differentiating characteristic, it is filtered out by the TX-PLL's loop filter with the transfer function $F(s)$.

III. SYSTEM ARCHITECTURE

Fig. 5 shows the overall system block diagram for implementing the new feed-forward architecture. The primary reference source is a low-phase noise oven-controlled crystal oscillator (OCXO). It generates a highly stable signal s_{OCXO} with an output frequency of 1 GHz. The primary reference source is distributed to an x64-PLL and a divide-by-ten frequency divider. The x64-PLL generates the signal s_{PLL} with low phase noise at a frequency of 64 GHz for the RFD. This x64-PLL incorporates a custom MMIC, developed and designed by us, specifically designed to handle high input frequencies, particularly the high reference frequency of the OCXO. This specialized MMIC is configured to work optimally with the OCXO's high frequency, allowing a low feedback division ratio of 64. This low division ratio contributes to achieving extremely low phase noise in the system. The key benefit of pairing the 1 GHz OCXO with the x64-PLL is the notable reduction in effective frequency spacing between two division ratios, which effectively minimizes linearity errors in the subsequent TX-PLLs. The RFD accepts values of $N_{+1} = 12 \ldots 259$, so its output signal

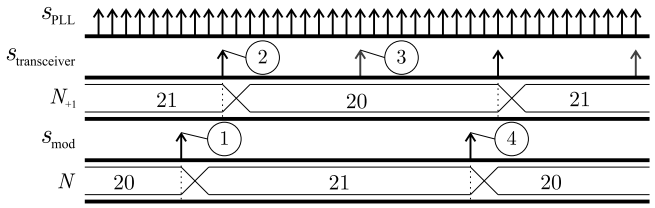

FIGURE 6. Exemplary timing diagram of the feed-forward concept for the modulation between the division ratios N=20 and N=21.

s_{mod} is capable of frequencies from 247 MHz ... 5.3 GHz. Eight transceiver channels of the FPGA feed the RFD's 8-Bit division ratio interface. Another transceiver channel is used to reset the RFD, which is necessary to synchronize the RFD with the FPGA's transceiver. Due to the limitation of the transceiver clock input buffers, the primary reference source is divided by ten to generate a stable 100 MHz reference signal s_{FPGA} for the transceivers. The internal PLLs of the FPGAs' transceivers multiply the frequency of s_{FPGA} by 64 to generate an output data rate of 6.4 Gbit/s, which is phase stable to the output of the RFD.

Due to the non-trivial calculation of the frequency patterns, a real time estimation of the required modulated division ratio for the RFD would limit the maximum output frequency of the system. Thus, these division ratios must be pre-calculated and stored in the fast DDR4 memory. During modulation, the FPGA logic loads these values back from the DDR4 and synchronizes them with the transceiver. The DDR4 memory is clocked at $f_{\mathrm{DDR4}} = 1.2$ GHz with 32 Bit bus width, corresponding to a peak transfer rate of 9.6 GB/s.

It is evident that the output of the RFD is not fed back into the FPGA, so the system is not working in a closed loop. Instead, all components work in parallel with proper synchronization. Due to the missing feedback from the RFD, the current output frequency has to be emulated by the FPGA to ensure proper modulation.

A. MODULATION IN THE FEED-FORWARD SYSTEM

Fig. 6 shows one exemplary timing diagram for modulation between the RFD's division ratios $N = 20$ and $N = 21$. The output pulses of the x64-PLL's 64 GHz output signal s_{PLL} and the 6.4 GHz output clock $s_{\mathrm{transceiver}}$ generated by the transceiver PLLs of the FPGA are shown in the time domain. Due to the same reference signal s_{OCXO}, all PLLs are synchronized with coherent phases. The N_{+1} signal represents the following division ratio provided by the transceivers, which is fetched from the DDR4 memory. The N signal shows the current division ratio of the RFD. The s_{mod} signal presents the output pulses generated by the RFD.

At the first output pulse, marked with point 1, the RFD loads the current adjacent division ratio from the N_{+1} data line into its current N flip-flop and changes its current division ratio to $N = N_{+1}$. A new output cycle of the RFD starts at this point. At marker 2, a new division ratio is fetched from the DDR4 memory into the transceiver and

is transmitted to the N_{+1} data line. The RFD loads its next division ratio only when the current output cycle is finished. Thus, N remains unchanged, and N_{+1} must be kept unchanged until the end of the next division cycle. At marker 3, the RFD is not ready to catch a new division ratio because the last output cycle still needs to be finished. Thus, the last N_{+1} value is held. At marker 4, the whole cycle starts again, and the RFD loads the new division ratio N_{+1}. The maximum output frequency of the signal s_{mod} has to be half of the maximum transceiver clock frequency. This guarantees that at least one clock cycle of the transceivers falls into the clock cycle of the RFD.

B. COMPONENTS

1) REFERENCE PATH

An OCXO of type NEL O-CEGM-70058ISEP is used as the primary reference so that the reference oscillator does not determine the phase noise of the overall system. Utilizing a fundamental 100 MHz OXCO and a multiple-by-ten stage, it has an output frequency of 1 GHz with low phase noise. A higher reference frequency would be affordable, but current commercial products in compact size are only available up to 1 GHz [24]. The OCXO offers a high output power of 12 dBm, which is needed to feed a resistive power divider of type Susumu PS2012GT2-R50-T1 to drive the x64-PLL and the div-by-10 divider of type Analog Devices AD9515. The power splitter offers an operating frequency of up to 10 GHz with a return loss better than 17 dB. The AD9515 is a programmable divider set to a fixed division ratio of ten with a duty cycle of 50%, which is needed for the transceiver PLLs in the FPGA.

2) X64 PHASE-LOCKED LOOP

The x64-PLL is based on a conventional PLL architecture. It consists of a custom MMIC, designed and developed by us, including the phase frequency detector (PFD), a feedback frequency divider with a fixed division ratio of 64, and a voltage-controlled oscillator (VCO) [25]. It is implemented in Infineon's SiGe:C BiCMOS B11HFC technology [26]. The VCO supports operating frequencies from 52 GHz up to 69 GHz and offers low phase noise of −105 dBc/Hz at 1 MHz offset of the free running VCO at 60 GHz. The highly linear PFD [27], supporting frequencies up to 10 GHz, is based on XOR system topology and has open-collector outputs of a differential current switch to drive an external differential active loop filter [28]. The loop filter is designed for the lowest integrated phase noise at 64 GHz. The simulated noise contributions to the PLL's output of its components and the total phase noise are shown in Fig. 7. For offset frequencies below 2 kHz, the reference noise of the OCXO, and for offset frequencies above 3.4 MHz, the VCO noise dominates the total phase noise. In between, the PFD's noise contribution is dominating. Due to the fixed output frequency of 64 GHz, the transient response can be neglected. Thus, the PLL was designed conventionally according to [21] with a loop bandwidth of 3.4 MHz and a high phase margin of 80°. The integrated phase noise from 100 Hz to 100 MHz corresponds to a jitter of 43 fs.

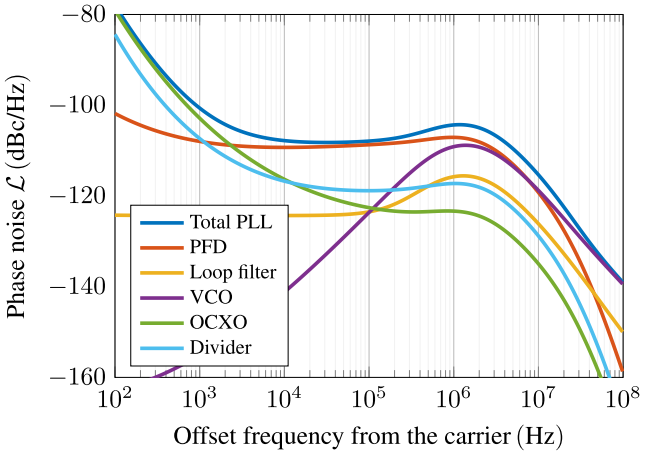

FIGURE 7. Simulated phase noise contribution of the components to the x64-PLL's output and the x64-PLL's total phase noise as a function of the offset frequency from the center frequency f_{PLL} = 64 GHz of the x64-PLL with a bandwidth of 3.4 MHz and a phase margin of 80°.

3) REFERENCE FREQUENCY DIVIDER

The RFD consists of another custom MMIC we designed and developed. It is fabricated in Infineon's SiGe:C BiCMOS B11HFC. The entire architecture is based on the dual-modulus principle, and an 8-bit parallel interface is provided for setting division ratios. The divider handles input frequencies up to 94 GHz and offers programmable division ratios between 12 and 259, provided by an 8-bit parallel interface. The RFD fetches a new division ratio only upon the next output pulse, using its internal flip-flops for synchronization. Transmitting a new division ratio via the transceiver during the alternate time cycle is secure. If a glitch were to occur during transmission, the RFD would ignore it. This divider, therefore, makes it possible to generate fractional division ratios by modulation. The overall architecture of the divider is described in detail in [29]. Additionally, the input stage of the parallel interface was modified to allow the high modulation frequency of the division ratios by implementing a differential input stage into the MMIC, which is compatible with the current mode logic (CML) of the FPGAs' transceivers with internal matching to 100 Ω. The differential input stage is DC-coupled. Otherwise, unmodulated bits would be in an undefined state and could toggle. Since the FPGA and the RFD only work in parallel during a chirp and the FPGA is aware of the current status of the RFD's internal counting registers by calculating the division ratios and the correct switching point beforehand, the synchronization of both can only be maintained within a chirp. The memory size of the DDR4 memory limits this. For this reason, the count registers of the RFD must first be reset before each chirp to restore synchronization, so an additional reset pin (RST) of the RFD is fed to another

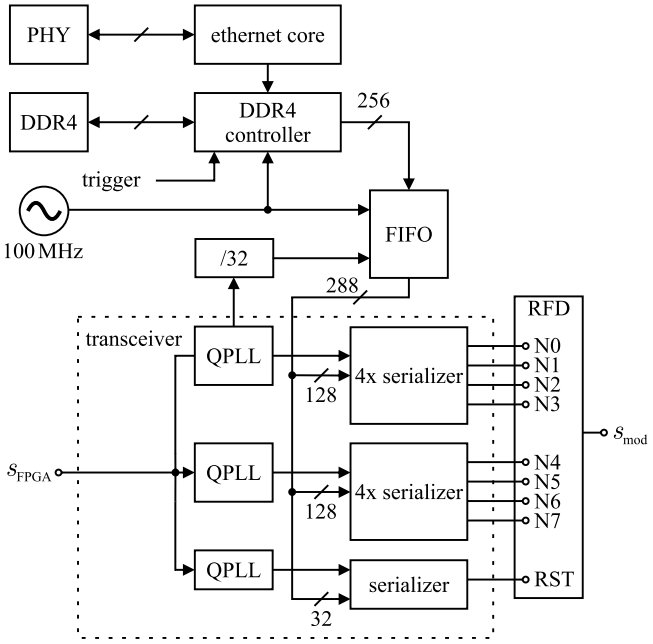

FIGURE 8. Design structure of the realized logic in the FPGA, including the ethernet core, the DDR4 controller, the transceiver, and the RFD.

transceiver channel. Otherwise, the FPGA would send new division ratios to the RFD incorrectly.

4) FIELD-PROGRAMMABLE GATE ARRAY DESIGN

Modern FPGAs like Xilinx Ultrascale or Intel Cyclone families contain standard high-speed I/O ports, which have clock capabilities of around 500 MHz and can be used directly by the logic without the need for serializers. However, these clock frequencies are too low for a high modulation frequency of the division ratios in the RFD. Modern FPGAs offer transceivers for high data rate transmission. We use a Xilinx Ultrascale+ FPGA, which supports data rates of up to 8 Gbit/s per channel [30]. Our design uses a data rate of 6.4 Gbit/s to have an integer transceiver PLL multiplication factor of 64. The FPGA is placed on an Enclustra Mercury XU7+ developer board. Moreover, the developer board has 1 GB of DDR4 memory directly connected to the programmable logic to achieve the highest possible peak data rate of 9.6 GB/s between the transceivers and the memory [31]. In our design, the processor system is not used to avoid unnecessary spurs in the output signal of the overall modulator, which are coupled in by the processor.

Fig. 8 shows the basic concept of the hardware and logic layout in the FPGA, which was designed using the Xilinx Vivado Design Suite. The overall DDR4 communication consists of several intellectual property (IP) cores. An external 1 Gbit/s ethernet physical layer transceiver (PHY) is connected via the media-independent interface (MII) to the ethernet core. The core consists of a media access control (MAC) block, an Internet protocol block, and a user datagram protocol (UDP) block, which we fully develop in very high-speed integrated circuit hardware description language (VHDL). Thus, the division ratios can be transferred to the DDR4 memory at maximum speed to minimize the overall startup time. The ethernet core receives the UDP data packages and rearranges the division ratios for the DDR4 controller. Furthermore, the DDR4 controller includes the Xilinx memory interface generator (MIG) IP-Core, which creates a bridge between the memory and the internal structure of the FPGA to allow easy access to the DDR4 memory [32]. The memory operates at 1.2 GHz with a data width of 32 bit [31]. The clock is generated from another 100 MHz XCO-Clock source on the developer board. The MIG uses a 4:1 data ratio, generating a parallel data bitstream of 256 bit. A standard I/O port is used as input for an external trigger to start the modulation of the RFD. After triggering, the DDR4 controller reads the DDR4 memory in ascending order. The MIG-Core generates the 256 bit, which could be directly forwarded to the transceiver. However, the MIG controller is not synchronized to the overall system OCXO. Moreover, due to the architecture of the DDR4 memory, a constant data flow is impossible. Hence, an asynchronous first-in, first-out memory (FIFO) with independent read and write clocks between the MIG and the transceiver is used. Thus, the DDR4 controller controls the MIG and the FIFO during modulation. It guarantees clock synchronization and that the FIFO is always adequately filled with values without going to an idle state.

The 8-bit parallel interface and the reset of the RFD are connected via the Xilinx high-speed transceiver of type GTH to the FPGAs logic. Each of the nine transceiver channels consists of a PLL and one serializer. Four transceivers share one PLL, called quad-PLL (QPLL) [33]. The QPLL operates at a frequency of 6.4 GHz. The divided 1 GHz OXCO reference signal is the primary reference clock source to guarantee a fixed phase shift between the output signals of the RFD and the QPLLs. A custom reset procedure was implemented for the QPLLs to generate a zero-phase shift at the transceiver's output, which is mandatory for high-speed modulation. One QPLL generates the application clock of 200 MHz. This clock is used to read the FIFO. The given bitstream is now directly forwarded to the serializers, which multiplexes the bitstream to the nine differential output stages of the GTH transceiver at the final output rate of 6.4 Gbit/s.

5) TRANSMIT PHASE-LOCKED LOOP

The following section briefly introduces the TX-PLL used in the further course. It should be noted that the TX-PLL is only used as an example to demonstrate the overall functionality of the chirp generator. In addition, the parameters of the chirp generator used in the further course for simulation and measurements are defined, as these are optimized for the used TX-PLL.

We utilize a V-band TX-PLL presented in [25]. The VCO has an output frequency of 52 GHz up to 69 GHz. For fast measurements, the chirp duration T_{chirp} is set to 1 ms. The output frequency of the signal s_{mod} of the RFD is modulated between 1.11 GHz and 1.47 GHz, corresponding to a fixed

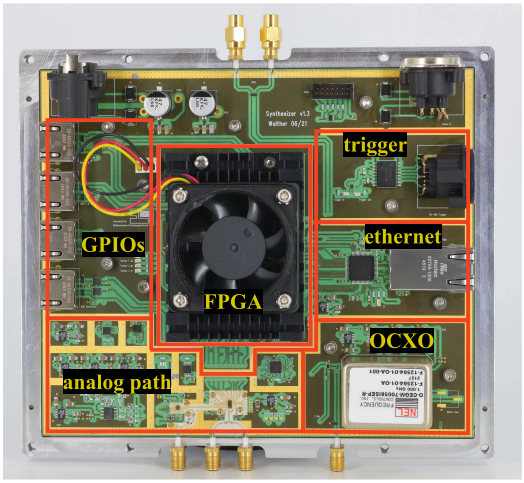

FIGURE 9. Manufactured chirp generator, including the FPGA and the custom PCB.

multiplication of 47 in the TX-PLL. A modulation frequency of the signal s_{mod} above 1 GHz avoids intermodulation with the 1 GHz OCXO reference. The resulting modulation bandwidth is $f_{\mathrm{BW}} = 362$ MHz.

IV. REALIZATION

The system consists of two modules, as depicted in Fig. 9. First is the FPGA module, including one system-on-chip (SoC) of type Zynq+ Ultrascale+, offering the FPGA, the DDR4 memory, and DC/DC converters. The FPGA bitstream can be programmed into a flash memory. This module is a commercial Enclustra of type Mercury+ XU7 product and offers a comprehensive arrangement of I/O ports, including the transceiver outputs. The module is mounted on a custom printed circuit board (PCB) using high-speed mezzanine connectors. The PCB contains all other peripherals and is made of a custom 4-layer stack. The top and first inner layer use Rogers RO3003 substrate with a thickness of 125 µm and reverse-treated electrodeposited 17 µm copper foil on both sides for low surface roughness of 1 µm RMS. RO3003 offers good RF characteristics ($\tan(\delta) = 0.0010$, $\epsilon_r = 3$) and is easy to handle during manufacturing. These good RF performances are needed due to the high frequencies of up to 64 GHz. The top layer is gold plated using an electroless nickel immersion gold (ENIG) plating process to bond the custom MMICs directly to the PCB. The core is made of FR4 with a thickness of 410 µm for mechanical stability. The second inner and bottom layers are used for power distribution.

The custom PCB is admitted and screwed into an aluminum enclosure. Due to the high power consumption of the MMICs, an excellent thermal connection is crucial. The thermal connection is guaranteed by direct contact with the aluminum enclosure. The chassis offers milled stands guided through the custom PCB so the MMICs can be directly glued to the chassis. The mixed-signal application of critical analog and digital parts requires excellent shielding between the components. Shielding is primarily relevant for the SoC

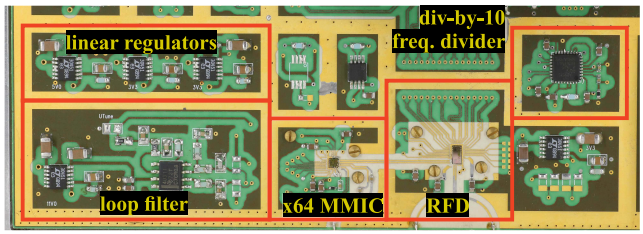

FIGURE 10. Close-up of the analog path, including the x64-PLL, the reference frequency divider, and the control circuitry.

module due to the DC/DC converters, which cause unwanted spurs in the output spectrum of the divider. Every group of components is individually shielded using cavities, as seen in Fig. 10. The cavities are realized in the top enclosure, which is mounted on the bottom enclosure. Proper contact between the top and bottom enclosure is ensured by using an additional conductive shielding gasket.

The design has several power lanes. All digital power lanes, including the SoC and the Ethernet PHY, are directly powered by the DC/DC converters of the SoC module. The analog power lanes of 3.3 V for the dividers, 5 V for the VCO and OCXO, and 10 V for the loop filter are individually blocked by linear voltage regulators, avoiding cross-talk. The input trigger is galvanically isolated to reduce ground loops when connected to external hardware. For future use, the custom PCB offers extended GPIO capabilities using standard RJ45 connectivity directly connected to the FPGA logic.

V. FREQUENCY SYNTHESIS

The overall architecture makes nearly every frequency modulation from 247 MHz to 2 GHz possible. As shown in Section III-B4, precalculating all division ratios is necessary, which can be done in a simple script, e.g., MATLAB. This section shows how to generate a high linear frequency chirp system based on a multi-stage noise shaping (MASH) $\Delta\Sigma$ modulator, one common frequency pattern approach for FMCW radar. The first step is calculating the ideal division ratios for the RFD for the most linear frequency chirp. The instantaneous frequency $f_{\mathrm{chirp}}(t)$ of a frequency chirp can be expressed as a function of the start frequency f_0, the desired bandwidth f_{BW}, and the chirp duration T_{chirp}:

$$f_{\mathrm{chirp}}(t) = f_0 + \frac{f_{\mathrm{BW}}}{T_{\mathrm{chirp}}} \cdot t. \tag{1}$$

The current output frequency f_{mod} of the RFD's output signal s_{mod} can be expressed for each timestep k by using the frequency f_{PLL} of the signal s_{PLL}:

$$f_{\mathrm{mod}}(k) = \frac{f_{\mathrm{PLL}}}{N_{\mathrm{ideal}}(k)}. \tag{2}$$

The frequency difference $\Delta f_{\mathrm{mod}}(k)$ between each timestep can be estimated by:

$$\Delta f_{\mathrm{mod}}(k) = f_{\mathrm{mod}}(k+1) - f_{\mathrm{mod}}(k) \tag{3}$$

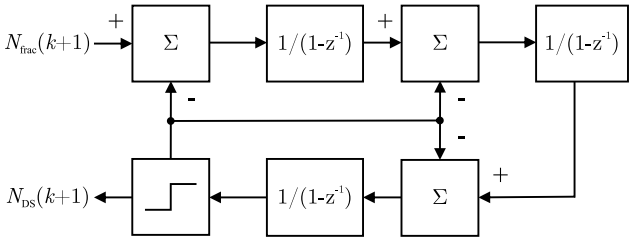

FIGURE 11. Third-order MASH architecture to generate the integer division ratios for the RFD.

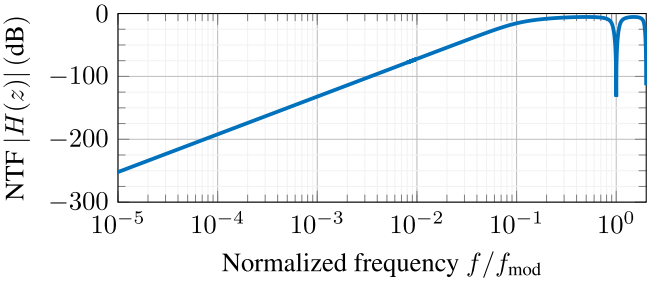

FIGURE 12. Noise transfer function for the quantization noise of the proposed third-order MASH architecture.

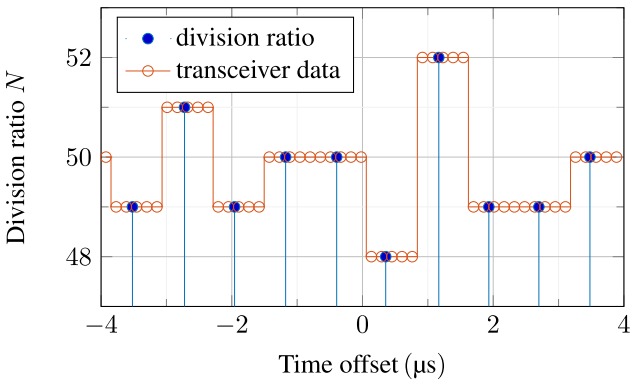

FIGURE 13. Calculated transceiver output and division ratios for a chirp duration of 1 ms at the center time of 500 μs.

and additional can be expressed by the linear equation with the ideal output division ratio N_{ideal}:

$$\Delta f_{\text{mod}}(k) = m \cdot \frac{N_{\text{ideal}}(k)}{f_{\text{PLL}}}, \tag{4}$$

with the chirp rate m:

$$m = \frac{f_{\text{BW}}}{T_{\text{chirp}}}. \tag{5}$$

Using all these equations results in the corresponding next division ratio:

$$N_{\text{ideal}}(k+1) = \frac{1}{\frac{1}{N_{\text{ideal}}(k)} + \frac{f_{\text{BW}}}{T_{\text{chirp}}} \frac{N_{\text{ideal}}(k)}{f_{\text{PLL}}^2}}. \tag{6}$$

The result of N_{ideal} is a rational number. However, the RFD supports only integer division ratios. To enable the fractional mode operation of the RFD and ensure high-frequency resolution during the frequency chirp, a $\Delta\Sigma$ modulator can be employed and implemented on the software side [34]. For instance, we utilize a third-order $\Delta\Sigma$ modulator in our chirp generator based on a MASH architecture, depicted in Fig. 11. This $\Delta\Sigma$ modulator handles the fractional part $N_{\text{frac}}(k+1)$ of the ideal division ratio $N_{\text{ideal}}(k+1)$ and alternates the output division ratio $N_{\text{DS}}(k+1)$ in a way that sets the correct average frequency due to the high clock frequency of the RFD [35]. This results in the final division ratio $N(k+1)$ for the RFD as follows:

$$N(k+1) = \text{floor}(N_{\text{ideal}}(k+1)) + N_{\text{DS}}(k+1). \tag{7}$$

However, due to the discrete frequency step size of the RFD, quantization noise occurs. According to [36], the noise transfer function (NTF) $H(z)$ of the $\Delta\Sigma$ modulator in Fig. 11 is defined as:

$$H(z) = \frac{(z-1)^3}{2z^3 - 6z^2 + 4z - 1}. \tag{8}$$

Fig. 12 shows the NTF normalized to the RFD's current output frequency f_{mod}. Notably, $H(z)$ exhibits high-pass behavior, significantly attenuating quantization noise near the carrier frequency. Moreover, it is evident that selecting a higher value for f_{mod} results in lower quantization noise near the carrier. Transitioning of the $\Delta\Sigma$ quantization noise to the phase noise $\mathcal{L}_{\text{DS}}$ at the output of the RFD can be approximated according to [34]:

$$\mathcal{L}_{\text{DS}} = \frac{f_{\text{PLL}}}{3N^3} \cdot \left(\frac{\pi}{f} \cdot |H(z)| \right)^2 \Bigg|_{z=e^{j2\pi f/f_{\text{mod}}}}. \tag{9}$$

Importantly, the quantization noise introduced by the RFD does not further impact the phase noise at the output of the TX-PLL, as the loop filter $F(s)$ within the TX-PLL effectively suppresses it for offset frequencies higher than its loop bandwidth [21]. This allows for very precise frequency resolution.

The last step is to generate the DDR4 memory bitstream the transceiver uses, as described in Section III-B4. The remaining time until the RFD loads the next division ratio is calculated for each frequency step. In this remaining time, the following division ratio is mapped to the fixed sampling points of the transceivers under consideration of setup and hold times. Fig. 13 shows the oversampled signal at the frequency chirp's center for an exemplary time point. The blue line represents the current division ratio in the RFD and the remaining time until the new division ratio is fetched. The red line represents the bitstream with its fixed sampling points. Lastly, a fixed number of samples will be adjusted to the entire bitstream to compensate for the phase delay between the FPGA and the RFD.

To demonstrate the full functionality of the chirp generator on a TX-PLL for generating mm-waves in the future, the chirp generator is now to be configured for an actual application with the parameters presented in Section III-B5.

Fig. 14 shows the simulated power spectrum of the RFD's output for three fractional division ratios to cover the entire bandwidth of the TX-PLL. The resolution bandwidth of the fast Fourier transformation (FFT) was chosen to

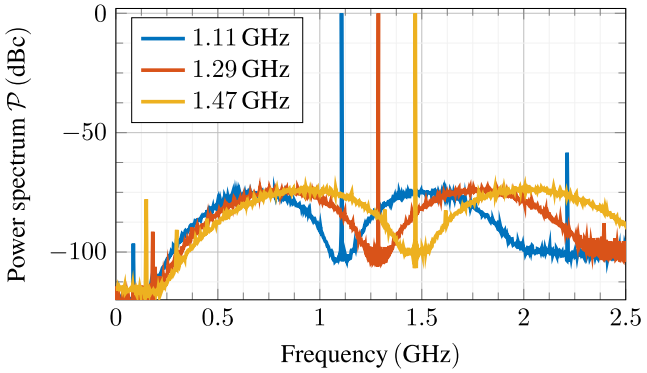

FIGURE 14. Simulated power spectrum for three frequencies of the RFD's output in fractional mode with a resolution bandwidth of 1 kHz.

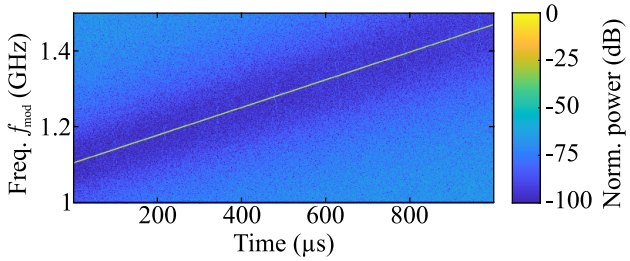

FIGURE 15. Simulated spectrogram for a frequency chirp duration of 1 ms from 1.11 GHz to 1.47 GHz at the RFD's output with a frequency resolution of 1 MHz.

$\Delta f_{\mathrm{FFT}} = 1\,\mathrm{kHz}$. The power spectrum was normalized to 0 dB. As anticipated, the quantization noise is shifted significantly away from the carrier, peaking at $1.5 \cdot f_{\mathrm{mod}}$ as depicted in Fig. 12, and can subsequently be suppressed by the loop filter of the subsequent TX-PLL. It can also be seen that the noise spectrum around the carrier is not symmetrical. This is caused by the noise shaping of the second harmonic, as is visible at $f_{\mathrm{mod}} = 1.1\,\mathrm{GHz}$.

Fig. 15 shows the simulated spectrogram of the output of the RFD based on a short-time Fourier transformation with a frequency resolution of 1 MHz. The output power of the frequency chirp was normalized to 0 dB. The noise shaping of the $\Delta\Sigma$-modulator is visible over the whole chirp length.

VI. VERIFICATION

A. PHASE NOISE

The phase noise of the x64-PLL was measured using a Rohde & Schwarz FSWP phase noise analyzer. Due to the limited input frequency of the analyzer, an integrated divide-by-four divider in the MMIC was used, corresponding to 16 GHz. Fig. 16 shows the measured phase noise compared to the simulation results from 100 Hz to 100 MHz. We used a cross-correlation factor (XCORR) of 1000, to avoid instrument noise of the FSWP in the measurement [37]. The results of the analyzer were already compensated for the divide-by-four frequency divider. The results are in good agreement with the simulation. The integrated phase noise from 100 Hz to 100 MHz was measured to −37.7 dBc, which corresponds to a jitter of 45 fs.

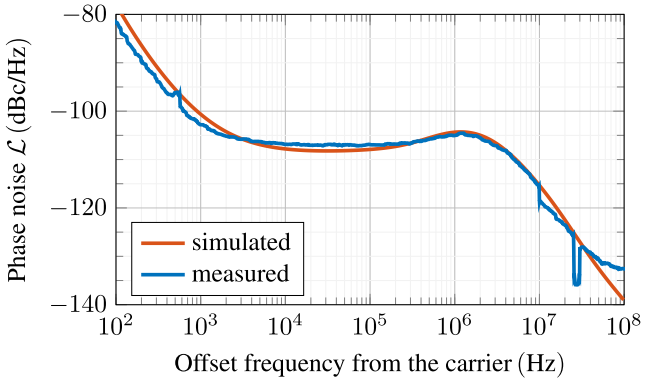

FIGURE 16. Measured and simulated phase noise as a function of the offset frequency of the x64-PLL at 64 GHz.

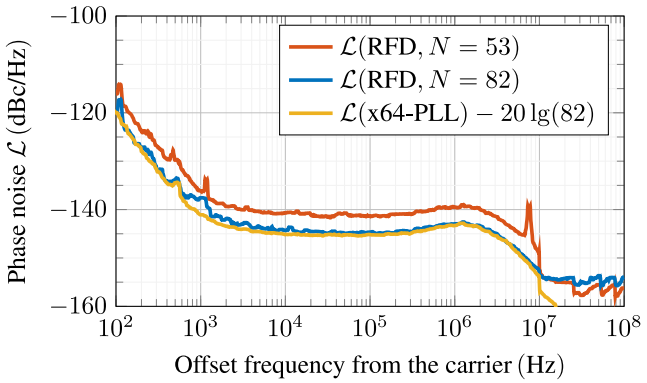

FIGURE 17. Measured phase noise as a function of the offset frequency of the reference frequency divider for fixed division ratios of N=53, N=82, and the phase noise of the x64-PLL compensated for the division ratio.

The phase noise of the RFD's output signal was also measured for fixed division ratios of $N = 53$ and $N = 82$. Due to the differential output of the RFD, we used a Marvell H-183-4 Hybrid to convert the output signal to the single-ended input of the FSWP to eliminate common mode spurs. As shown in Fig. 17, the phase noise is dominated by the x64-PLL output noise. The additive phase noise of the RFD is neglectable. The difference between the RFD's output phase noise for the two division rations is $20\log_{10}(82/53) = 3.8\,\mathrm{dB}$ as expected.

B. FRACTIONAL MODE

To demonstrate the maximum output frequency and the fractional control of the RFD, the FSWP in spectrum analyzer mode is used. The spectrum analyzer's resolution bandwidth (RBW) depends on the sweep time. Because the modulation sequence for the non-integer division ratio used for fractional mode is stored in the DDR4 memory, the maximum output sequence time is limited to 150 ms. This corresponds to the maximum feasible sweep time of the spectrum analyzer. An additional trigger channel ensures the spectrum analyzer captures the full sequence length. The trigger is generated by another transceiver channel, which can have a phase delay to the RFD output. So, another

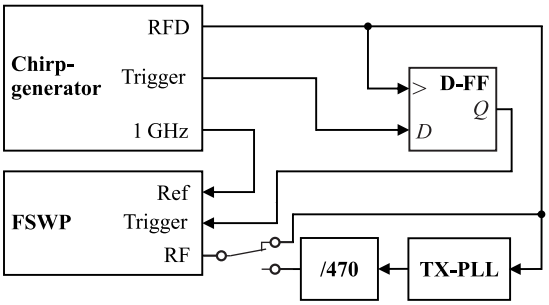

FIGURE 18. Test setup for verifying the fractional mode for proper synchronization of the FSWP with the chirp generator.

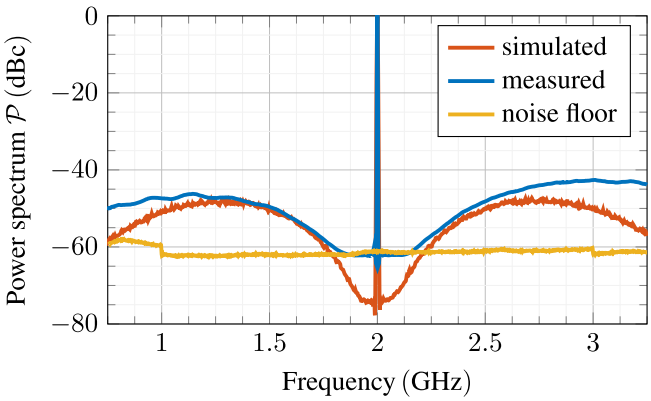

FIGURE 19. Measured spectrum of the reference frequency divider in the fractional mode for 2 GHz with an RBW of 2 MHz compared to the simulation.

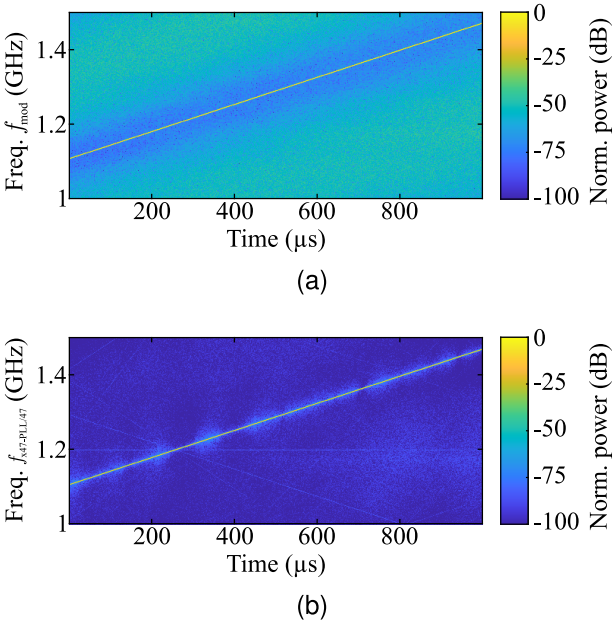

FIGURE 20. Measured spectrograms for a center frequency of 1.29 GHz with a bandwidth of 362 MHz directly at the output of the RFD (a) and at the output of a TX-PLL divided by 47 (b) for a chirp duration of 1 ms with an RBW of 1 MHz.

synchronization stage of the RFD's output and the trigger is necessary. This test setup is shown in Fig. 18. The output of the RFD is distributed to the RF-input of the Rohde and Schwarz FSWP and the clock input of a data-flip-flop (D-FF). The data port of the D-FF is connected to the trigger output of the chirp generator. The output of the D-FF is used as the trigger input of the FSWP to start a new measurement. The TX-PLL and the M-Divider were bypassed for the fractional mode measurements. The spectrum was measured for the maximum output frequency of the generator ($f_{\mathrm{mod}} = 2\,\mathrm{GHz}$) in fractional mode. The RBW was set to the minimum of 2 MHz with a video filter bandwidth of 10 kHz. The result is shown in Fig. 19, including simulations with the same RBW normalized to 0 dBm and compensated for the VBW. Moreover, the noise floor of the FSWP in this configuration was measured. The results are in good agreement with the simulations. The noise shaping is visible. However, the noise on the right side of the carrier is higher than expected. The noise of the second harmonic of the carrier causes this. Due to the high noise floor, which is limited by the sweep time, a more precise observation of the spectrum close to the carrier is impossible.

C. CHIRP MODE AND LINEARITY

A linear modulated frequency chirp was generated to demonstrate the chirp mode according to the procedure presented in Section V for the TX-PLL. The sequence comprises a center frequency of 1.29 GHz with a bandwidth of 362 MHz and a chirp duration of 1 ms. First, the generated frequency chirp was measured directly at the output of the RFD with a Keysight M9502A digitizer at 32 GS/s, and again, a spectrogram was formed, which is shown in Fig. 20(a). 1 MHz was chosen as the RBW for a sufficient trade-off between frequency and time resolution. The spectrogram shows a linear chirp without discrete spurs. However, the delta-sigma noise is visible. In the next step, the RFD's output signal was utilized as a reference frequency chirp for the TX-PLL. The output frequency of the TX-PLL is divided by 47 to compare its spectrogram with the reference signal. In Fig. 20(b), the spectrogram is depicted. It can be observed that the TX-PLL sufficiently suppresses the $\Delta\Sigma$-noise because it has a loop bandwidth of 3 MHz. Minor deviations of −70 dBc occur close to the chirp due to non-idealities in the PFD. Furthermore, additional interference lines are visible, generated by the clock generators and aliasing within the digitizer, and do not belong to the chirp generator.

To measure the reference frequency chirp generator's linearity, the same test setup as shown in Fig. 18 was used due to the digitizer's limited dynamic range. Still, we used the TX-PLL to filter out the $\Delta\Sigma$ noise. The frequency chirp of the TX-PLL is divided by $M = 470$ and sampled by the FSWP in the transient mode, which supports bandwidths up to 40 MHz. The result of the linearity error is shown in Fig. 21 for an averaging factor of 1000 to measure only systematic errors. The results are compensated for the M-divider and the TX-PLL to show the frequency error at the output of the RFD. The overall frequency error is smaller

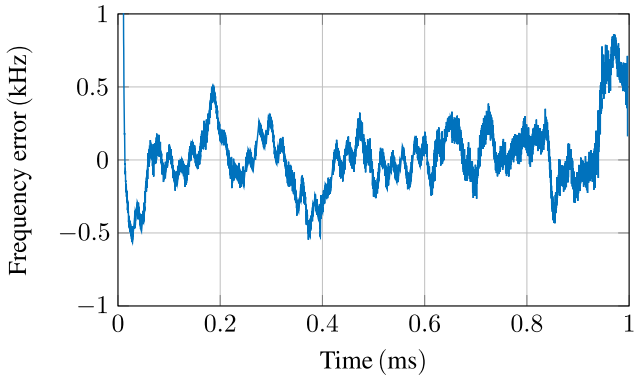

FIGURE 21. Measured frequency error for a 1 ms chirp duration with a modulation bandwidth of 362 MHz.

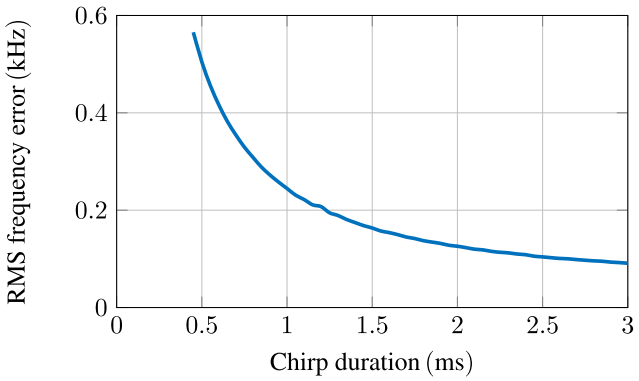

FIGURE 22. Measured RMS frequency error for chirps from 450 μ s to 3 ms in steps of 50 μ s with a modulation bandwidth of 362 MHz.

than 800 Hz, and the RMS frequency error is smaller than 241 Hz for a 1 ms chirp.

As the frequency error increases with decreasing chirp time and constant bandwidth, the RMS frequency error for chirp durations from 450 µs to 3 ms with a stepsize of 50 µs was measured to show the ability of fast chirps. The results are shown in Fig. 22. Faster chirp durations than 450 µs are possible, but the TX-PLL could not follow that chirp due to the limiting bandwidth.

VII. COMPARISON WITH STATE-OF-THE-ART SYSTEMS

Table 1 compares other current systems suitable as reference generators for linear chirps. Designs comparable to this work were selected for their center frequency and bandwidth. The table presents the absolute and normalized RMS frequency errors (ppm) based on the chirp bandwidth to facilitate better comparison. Additionally, the phase noise of all other systems was adjusted to our center frequency of 1.12 GHz for normalization.

In [16], an all-digital phase-locked loop (ADPLL) was developed to generate a linear frequency chirp with 300 MHz bandwidth at a center frequency of 12 GHz. The authors also emphasized fast measurement times and high linearity through two-point modulation combined with a digitally controlled oscillator. Although the system achieves significantly faster chirps and good linearity while maintaining good phase noise, this system provides only a third of our bandwidth. A significant advantage, however, is that the entire system has been integrated into a single MMIC. In [17], a classical PLL with fractional control of the in-loop divider was developed. The developed PLL has a similarly high bandwidth with faster chirp durations and is fully integrated. However, it performs significantly worse in terms of phase noise and linearity. In addition, distributing a 23 GHz signal as a reference for MIMO systems is complex. In [18], a DDS was developed based on an RF SoC. This technology is very flexible in principle since any frequency patterns can be programmed very easily. Both the bandwidth and the center frequency are comparable with our system. In addition, it also shows high linearity with very fast chirps, although our system still delivers better linearity. Unfortunately, no information on the SFDR could be found, which is a decisive criterion, especially when using DACs. In addition, no information was given on the phase noise. In [19], a combination of DDS was used as a reference and an ADPLL. The system thus achieves the highest bandwidth compared to the other methods but is most clearly defeated in linearity.

TABLE 1. Comparison with state-of-the-art systems.

Work	This	[16]	[17]	[18]	[19]
Architecture	Ref. freq. Frac.-N	ADPLL	PLL Frac.-N	DDS RF-SoC	DDS ADPLL
Implementation	Hybrid	Mono	Mono	Mono	Mono
Center freq. (GHz)	1.12	12	23	1.35	15
Chirp BW (GHz)	1.75	0.3	1.25	1.7	2
Max. slope (MHz/µs)	0.8	78	1.8	47	4
Sweep time (µs)	1000	1000	125	36	5000
RMS freq. err. (kHz)	0.241[2]	5.8	68.8	10.5	1210
RMS freq. err. (ppm)	0.67	19.33	55.04	6.17	605
Phase noise (dBc/Hz)[1]	-140	-134	-114	N/A	-123
Power cons. (W)	11.5	0.034	0.092	3.4	0.039
Size (mm^2)	1156	0.32	N/A	1444	0.665

[1] 1 MHz offset of the center frequency, normalized to 1.12 GHz
[2] For 362 MHz bandwidth

Because of the discrete implementation, power consumption and the total size is higher than fully integrated solutions. The power consumption totals 4.8 W for the analog path, which includes the OCXO, and 11.5 W for the FPGA and its peripherals, along with the DDR4 memory. The size encompasses the space occupied by the FPGA, DDR4 memory, the x64-PLL, and the RFD. However, the presented system offers decisive advantages over the integrated architectures regarding flexibility. For example, the frequency range, the chirp function, and the modulation type can be reprogrammed as required and can, therefore, be optimized for the given application. However, it should be noted here that an FPGA and additional control circuitry

are required to implement an FMCW MIMO system anyway, which can be combined with this system. Therefore, the increased consumption for an overall system can be neglected.

Although our system performs less well in the area of maximum slope in this comparison, it should be noted that the slope is limited by the subsequent PLL and not by the actual frequency generator. Our system is superior in all other parameters and currently provides the highest linearity, the lowest phase noise, and high bandwidth. In addition, the overall new concept of modulating a frequency divider in the feed-forward path was realized for the first time with a maximum output frequency of 2 GHz.

VIII. CONCLUSION

In this work, we have presented a novel reference frequency chirp generator based on a fractional frequency divider in the reference path for linear chirps by using a new feed-forward architecture. The generator allows modulated output frequencies of up to 2 GHz with an adjustable bandwidth of up to 1.75 GHz and simultaneous low phase noise of −140 dBc/Hz at 1 MHz offset from the carrier at the center frequency. Used as a reference for a PLL, the generator offers a low RMS linearity error of 241 Hz. This makes the reference chirp generator ideal for physically distributed MIMO systems to ensure high coherence between transmitting modules while achieving high measurement accuracies in the mm-wave range.

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