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FBMC vs. PAM and DMT for High-Speed Wireline Communication

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ABSTRACT This paper demonstrates the first silicon-verified FBMC encoder and decoder designed to emulate beyond $224Gb/s$ wireline communication. It also compares the performance of FBMC to PAM and DMT in three steps. First, the digital power and area consumption are compared using measured results from the manufactured test chip. Second, the data rate is determined using lab-measured results. And third, the performance when subject to notched channels is analyzed using simulation results. Finally, we present a method to emulate wireline links while reducing the emulator complexity and simulation time by one to two orders of magnitude over conventional over-sampled techniques. Our analysis indicates that given a smooth channel and an SNR which enables an average spectral efficiency of $4bits/sec/Hz$ at a bit-error rate of 10^{-3}, both DMT and FBMC perform similarly to a conventional PAM-4 link. However, when noise is reduced and a spectral notch is applied, thereby achieving an average spectral efficiency of $4.6bits/sec/Hz$, DMT and FBMC can outperform PAM by 2.1 and 2.3 times, respectively. In addition, we estimate FBMC's encoder and decoder power consumption at $1.53pJ/b$ and $1.98pJ/b$, respectively, and area requirement at $0.07mm^2$ and $0.17mm^2$, respectively, which is similar to DMT. These values are competitive with similar $22nm$ PAM transceivers, suggesting that DMT and FBMC are viable alternatives to PAM for next-generation high-speed wireline applications.

INDEX TERMS Discrete multi-tone (DMT), emulation, filter-bank multi-carrier (FBMC), orthogonal frequency division multiplexing (OFDM), pulse amplitude modulation (PAM), SERDES, wireline.

I. INTRODUCTION

PULSE-AMPLITUDE Modulation (PAM) has dominated the high-speed wireline industry since its inception [1]. Initially, PAM-2 achieved a spectral efficiency of $2bits/sec/Hz$, equating to one bit per sample, assuming the signal bandwidth is half the sampling frequency. However, as data rates increased, this put a strain on bandwidth requirements. To address this, the industry adopted PAM-4 modulation, achieving $4bits/sec/Hz$, doubling the data rate while maintaining the same channel and sampling frequency. However, with the recent jump to $224Gb/s$ [2], PAM-4 modulation is nearing its limit. To minimize the link's attenuation up to $56GHz$, these transceivers necessitate numerous bandwidth extension techniques such as distributed Electrostatic Discharge (ESD) protection and inductive peaking [3]. Furthermore, the systems impose stringent channel requirements, necessitating a smooth response with minimal reflections to limit the already power-hungry equalization [3], [4]. Enabling the next jump to $448Gb/s$ using PAM-4 would require a bandwidth of $112GHz$. Such an achievement has yet to be demonstrated using silicon technology and would require substantial performance improvements in areas such as bandwidth extension, clock generation, channel and package design, and could significantly increase the equalization's complexity [4]. Raising the modulation order is also undesirable as it would

necessitate increasing supply levels to meet Signal-to-Noise Ratio (SNR) requirements, significantly increasing the power consumption.

This has sparked interest in alternative modulation schemes such as multi-carrier signalling [5], [6]. These systems have been successful in other applications such as DSL, long-haul optical, and wireless due to: 1) their ability to achieve high spectral efficiency in challenging environments [7], [8], [9], [10], [11], 2) their improved frequency selectivity, overcoming spectral notches [12], [13], 3) their fully digital implementation, and 4) their power-efficient approach to equalization [5], [12]. However, the most well-known implementation, Discrete-Multi-Tone (DMT) modulation, has several challenges, including a high Peak-to-Average Power Ratio (PAPR), high latency, data rate overhead from adding a Cyclic Prefix (CP), data rate overhead from reserving bins for channel estimation and timing recovery, poor filtering characteristics, and limited noise and jitter tracking ability [14]. Recently, [14], [15], [16] have proposed methods to address these concerns, including adopting Filter-Bank Multi-Carrier (FBMC) modulation, an alternative to DMT [12], [13], [17], [18]. However, there remains uncertainty over the level of improvement that can be achieved by switching from PAM to DMT or FBMC. This paper compares the performance of these three modulation schemes using a combination of measurement and simulations. First, the digital power and area consumption are compared using measured results from a manufactured test chip. Second, the data rate is determined using lab-measured results. And third, the performance when subject to notched channels is determined using simulation results.

The paper is organized as follows: Section II provides a brief background of the three modulation schemes, discussing the limitations of each, and explaining their optimization procedure. Section III describes the FBMC test chip and discusses the proposed approach to efficient link emulation. Section IV compares the performance of the three schemes using results from silicon measurements, in-lab measurements, and simulations. Section V concludes the paper.

II. BACKGROUND

A. PULSE AMPLITUDE MODULATION (PAM)

As shown in Fig. 1a, a typical PAM-M transmitter maps $log_2(M)$ bits to a real-valued symbol $\Omega[n]$ where n is the discrete-time index. This symbol is sent through a pre-emphasis Finite Impulse Response (FIR) equalizer to produce $x[n]$ and converted through a Digital-to-Analog Converter (DAC) to a continuous-time analog signal $x(t)$. After passing through the channel, the received signal $y(t)$ is typically equalized through a Continuous-Time-Linear-Equalizer (CTLE) and sampled by an Analog-to-Digital Converter (ADC) to form $y[n]$. Feed-Forward Equalization (FFE) followed by Decision-Feedback Equalization (DFE) recovers the symbol $\Pi[n]$, which is converted back to bits to form the receiver output [3].

One of the challenges with PAM is the need to eliminate inter-symbol interference (ISI) to recover the transmitted symbols. This is difficult for non-smooth channels, such as those with a spectral notch caused by impedance mismatch along the signal path [19]. This increases power consumption, area requirements, and noise amplification at notched frequencies, degrading the SNR.

B. DISCRETE MULTI-TONE (DMT)

A solution to the above problem is multi-carrier modulation, which splits a channel into multiple frequency bins and sends a modulated tone in each to convey information [14], [15], [16]. This allows frequencies with poor SNR to be avoided. Additionally, multi-carrier modulation enables single-tap equalization, a more efficient alternative to PAM equalization [5].

DMT modulation is the most well-known implementation of multi-carrier signalling [12]. As shown in Fig. 1b, the transmitter maps binary input data to a set of complex-valued input symbols $\Omega_i[k]$, where $i \in \mathbb{Z}$ is the frame index, $k \in \{1, \ldots, N_{bin}\}$ is the bin index, and $N_{FFT} = 2N_{bin}+2$. The allocation of bits, referred to as the bit-loading optimization, dictates the size of each constellation [19]. These symbols are scaled by constant values, referred to as the power-loading optimization, before Hermitian symmetry is enforced, inserting complex conjugate symbols to form $X_i[k]$. Note that the DC ($k = 0$) and Nyquist ($k = N_{FFT}/2$) bins remain empty as they cannot support complex modulation [15]; however, they could be used for PAPR reduction [16]. The symbols are then fed through an Inverse Fast-Fourier Transform (IFFT) to produce samples $x_i[n]$, where $n \in \{0, \ldots, N_{FFT}-1\}$ is again the discrete-time index. A Cyclic Prefix (CP) is appended, extending the frame to $N_{FFT} + N_{CP}$ where N_{CP} is the length of the CP [5]. The samples are then serialized and converted through a DAC to a continuous-time analog signal $x(t)$ [15]. After passing through the channel, the received signal is sampled by an ADC and undergoes the reverse coding operation, removing the CP, passing through an FFT, and removing Hermitian symmetry. The resultant symbols $Y_i[k]$ are sent to a set of single-tap equalizers, one per bin, to recover the output symbols $\Pi_i[k]$ [14], [15]. Finally, these are mapped to the receiver's binary output data.

The work by [15] proposes a method to combine the process of channel estimation and timing recovery into a unified system. This approach adaptively determines equalization coefficients and accurately tracks sampling phase error, improving the jitter tracking performance without introducing additional data rate overhead. With this, DMT overcomes the challenges faced by PAM but introduces its own limitations. First, the lack of frame shaping results in abrupt transitions at frame boundaries, requiring a guard interval (the CP) to avoid performance degradation from ISI. This introduces data rate overhead, particularly for low-latency implementations with a short frame length [14]. Second, the CP changes the frame length,

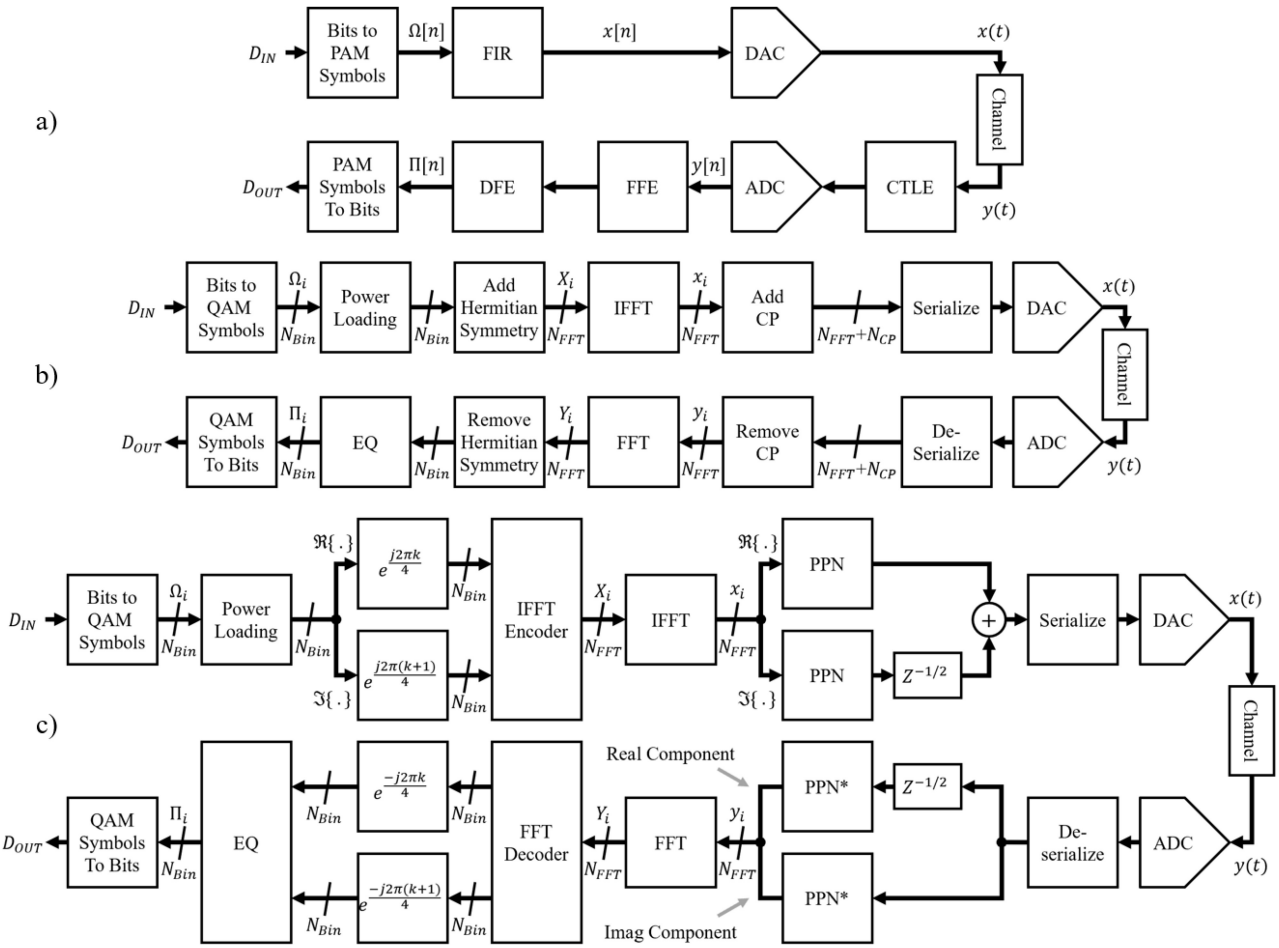

FIGURE 1. Top-level block diagram for: a) PAM, b) DMT, c) FBMC.

which complicates serialization/deserialization as gear shifting is needed to process the non-power-of-two samples. And third, rectangular windowing in the time-domain results in a sinc filter response in the frequency domain with large $-13dB$ sidelobes. This poor filtering characteristics results in interference among frequency bins when impairments are present [12], [13].

C. FILTER BANK MULTI-CARRIER (FBMC)

FBMC addresses several of the drawbacks mentioned for DMT. This alternative multi-carrier modulation scheme applies shaping to smooth the transition between frames and remove the need for CP, thus eliminating the data rate overhead and simplifying serialization/deserialization. Furthermore, with careful design of the frame shaping filter, sidelobes can be lowered considerably, reducing interference among frequency bins [12], [13], [18].

As shown in Fig. 1c and similar to DMT, bit-loading maps input data to complex-valued symbols $\Omega_i[k]$. However, after power-loading is applied, the in-phase and quadrature components of the symbols are separated, and a quadrature-phase rotation is applied to ensure a $\pi/2$ phase difference between neighbouring bins. Then IFFT coding is applied to produce $X_i[k]$ and enable the use of a single IFFT [14]. The output $x_i[n]$ is separated into its two components, and each is sent through a Poly-Phase Network (PPN) to shape the frames [12]. The quadrature waveform is staggered by half a frame period, combined with the in-phase waveform, serialized, and converted through a DAC to a continuous-time analog signal $x(t)$. At the receiver, the reverse operation is applied.

Although FBMC appears to be the most complex solution of the three alternatives, adopting techniques from [14] makes it possible to implement such a system efficiently, and as will be shown in Section IV, can ensure a similar complexity to PAM and DMT.

It is worth mentioning that multi-carrier systems do not require a CTLE. This reduces power, area, and noise [14]. However, a CTLE can be added to partially equalize the recovered signal. In DMT systems, this is recommended to reduce the overhead of the CP. In contrast, FBMC systems do not have this overhead, so the need is reduced. Nonetheless, both DMT and FBMC systems can achieve performance improvements with a CTLE as this reduces the link's attenuation, resulting in an improved SNR.

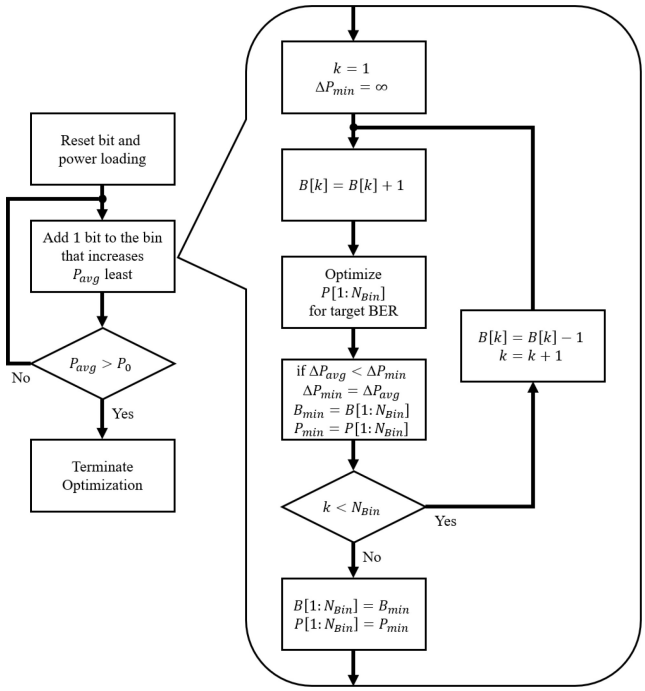

FIGURE 2. Bit- and power-loading optimization procedure.

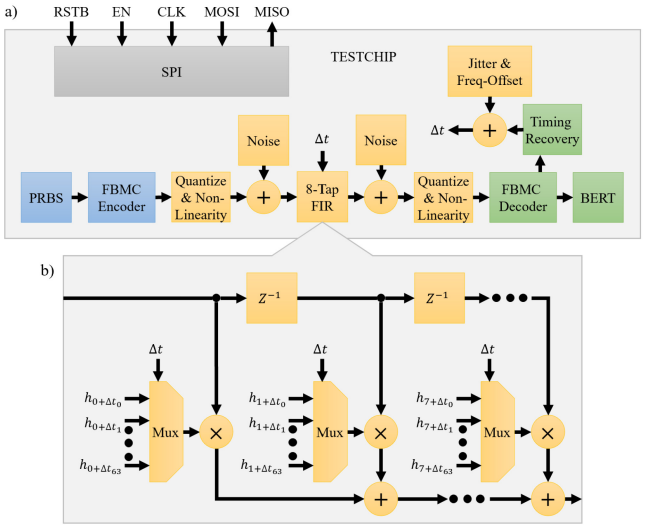

FIGURE 3. a) A block diagram of the implemented test chip where blocks in blue represent the encoder, green the decoder, yellow the emulation channel, and gray debug circuitry. b) a detailed block diagram of an 8-tap FIR, as used in a), with programmable parameters.

D. OPTIMIZATION

Whereas PAM must optimize numerous equalization knobs, a challenging task that may necessitate complex adaption techniques such as genetic search algorithms [20], in multi-carrier systems, each bin must only optimize three control knobs: single-tap equalization, bit-loading, and power-loading. The first is set trivially by observing the received constellations [15], and the latter two can be set according to the procedure in Fig. 2. This procedure is based on the Levin-Campello algorithm [21] but modified to include power-loading optimization. At a high level, bit-loading is optimized to transmit as many bits as possible within an average signal power constraint P_0, while power-loading is optimized to ensure each bin's BER equals the system's target [19]. The optimization begins with bit-loading $B[k]$ set to 0 and power-loading $P[k]$ set to 1 for all values of k. Then, one bit is added to the bin that increases the average signal power the least. This process is repeated until the average signal power P_{avg} reaches the power limit P_0, at which point the algorithm terminates. The inset depicts the trial-and-error bin selection process. A single bit is added to one bin at a time. When impairments are present, symbol interference will affect the performance of surrounding bins. As a result, power-loading is adjusted to ensure that the BER of each bin remains at the target. The change in average signal power ΔP_{avg} is recorded, and the system is returned to its original state. Once each bin has been trialled, the one which increased the average signal power the least ΔP_{min} is selected as the recipient of the next added bit. Thus, the corresponding bit-loading B_{min} and power-loading P_{min} is applied.

III. PROPOSED FBMC TESTCHIP

Our proposed test chip, designed and fabricated using Global Foundry's 22*nm* FD-SOI technology, is a fully-digital system that includes an FBMC encoder, decoder, and emulation blocks used to model functions and impairments of analog circuits. The chip employs a $3.3V$ IO supply and a $0.8V$ core supply. A block diagram of the complete test chip is shown in Fig. 3a. The encoder is coloured blue, the analog components and their impairments yellow, the decoder green, and the Serial-to-Parallel Interface (SPI) grey. Binary data is generated using 120 on-chip Pseudo-Random Binary-Sequence (PRBS) generators, enabling up to eight binary streams per frequency bin depending on the constellation size. Each stream operates at $fs/32$. Activating only 64 achieves the target emulated data rate of $224Gb/s$. The bits are encoded using FBMC modulation according to the procedure discussed in Section II and assuming a fixed 32-point FFT system with 15 frequency bins. Then, the signal undergoes processing through digital blocks that emulate the impairments commonly associated with analog circuits. DAC quantization and non-linearity are emulated using a Look-Up Table (LUT) that performs a 1-to-1 voltage mapping. Quantization is modelled by rounding the signal amplitude to its nearest quantization level, and non-linearity is modelled by compressing the mapping at either extreme to mimic the desired Total Harmonic Distortion (THD). DAC thermal noise is emulated by summing the outputs of up to 32 dedicated PRBS generators. DAC mismatch is emulated using a single PRBS generator with a variable amplitude disturbance. DAC clock injection noise is emulated using a CORDIC converter, which produces a sinusoidal disturbance with an adjustable magnitude and frequency [22], [23]. The channel, package, and CTLE frequency-dependant transfer functions are emulated using a programmable 8-tap FIR

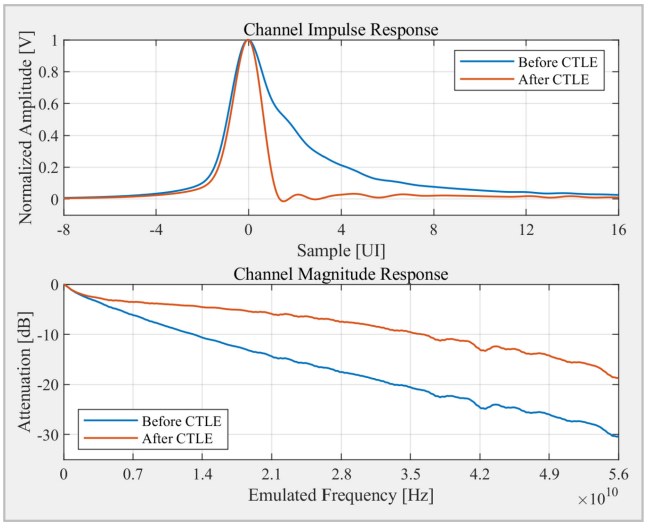

FIGURE 4. An example of the test chip's emulated channel response with 30*dB* attenuation at 56*GHz* sourced from the IEEE 802.3 Ethernet Working Group [24] before and after applying a CTLE with 12*dB* of peaking at 56*GHz*.

filter. As illustrated in Fig. 4, the test chip can model channel and package attenuation of up to 30dB, assuming a CTLE with 12dB of peaking partially equalizes the impulse response to less than 8UI in length when considering only the portion of the response where the absolute amplitude exceeds 3% of the main cursor. Although not implemented, package reflections could be emulated by adding additional floating taps. As will be discussed next, a variable Δt knob adjusts channel coefficients to emulate the effects of jitter and frequency offset. ADC thermal and deterministic noise, quantization, and non-linearity are all emulated in the same manner as for the DAC. Crosstalk can also be emulated by adding additional noise to the ADC input. The signal is then decoded and sent to an on-chip Bit-Error-Rate Tester (BERT) that can determine the performance of individual frequency bins. Assuming an emulated sampling frequency of 112GS/s and thus a 3.5GHz DSP clock, encoding and decoding each require 11 clock periods, resulting in a total link latency of 6.3ns.

The decoder implements adaptive decision-directed channel estimation and timing recovery, as described in [14], to adjust equalization and track phase and frequency disturbances, as discussed next. Finally, an SPI is used to write and read over 86, 000 knobs and test points, enabling control and monitoring over all aspects of the link.

This test chip implements timing recovery to track jitter and frequency offset. Both impairments are tracked in real-world systems by adjusting the ADC's sampling time in sub-Unit Interval (UI) increments, often using a Phase Interpolator (PI). This process can be modelled in the digital domain by over-sampling the transmitted signal. The receiver then selects one of these phases depending on the sampling time. However, emulating such a system is impractical as numerous samples must be calculated per UI. For instance, implementing a channel with a maximum pulse response length of 8UI and 64 phases would require a 512-tap FIR filter. This significantly increases complexity and limits the emulation clock speed. Instead, we propose a technique to model jitter and frequency offset without over-sampling.

When a signal $x(nT)$ passes through a channel, it is convolved with the channel's pulse response $h(nT)$, as given by Eq. (1). A change in the receiver's sampling phase can be modelled by a sub-UI Δt signal delay, as shown in Eq. (2). By using the time shift property of convolution [25], we can rewrite Eq. (2) as Eq. (3) which reveals that sampling phase adjustment by Δt is equivalent to changing the FIR coefficients. This alternative reduces the emulation complexity without affecting accuracy. Therefore, our test chip selects one of 64 coefficients per FIR tap on a per-UI basis. With this, jitter and frequency offset are modelled by adding disturbances to the Δt control knob in the form of a random offset and a ramping offset. This approach models jitter and frequency offset without noticeably affecting the implementation complexity or emulation clock speed. The technique can also accelerate conventional time-domain simulation.

$$y(nT) = \sum_{\tau=-\infty}^{\infty} h(\tau)x(nT-\tau) \tag{1}$$

$$y(nT+\Delta t) = \sum_{\tau=-\infty}^{\infty} h(\tau)x(nT+\Delta t-\tau) \tag{2}$$

$$y(nT+\Delta t) = \sum_{\tau=-\infty}^{\infty} h(\tau+\Delta t)x(nT-\tau) \tag{3}$$

IV. PERFORMANCE COMPARISON RESULTS

A. FBMC TEST CHIP

Figure 5 shows the measured silicon results of the test chip's synchronization procedure in the presence of frequency offset. This emulation applies 16-QAM constellations in all bins, sets the DAC and ADC resolution to 7-bits, adds 6.0$mVrms$ of thermal noise to reduce their ENOBs to 5.5-bit assuming a $1V_{pp,diff}$ swing, applies $-40dB$ THD to either converter, models a 12dB channel, and includes a 122ppm frequency offset.

Initially, a training sequence synchronizes the gain and rotation of the single-tap equalizers. Then, the rotation equalization, shown in Fig. 5a, is used to perform coarse timing synchronization. The PI, shown in Fig. 5b, is adjusted to drive the first bin's rotation equalization to zero, thus achieving coarse frequency and phase synchronization. Next, we incrementally observe the rotation equalization of more bins, with their values averaged to obtain fine jitter tracking. Finally, as shown in Fig. 5c, the error counter is reset to one, and the BER drops logarithmically, showing error-free communication [14], [15].

Figure 6 shows our jitter tolerance analysis. For this test, we extrapolate emulation results assuming a 112GS/s sampling rate with a 3.5GHz DSP clock frequency and apply both 4-QAM and 16-QAM constellations to all bins. Sinusoidal jitter, initially small, is increased until the system

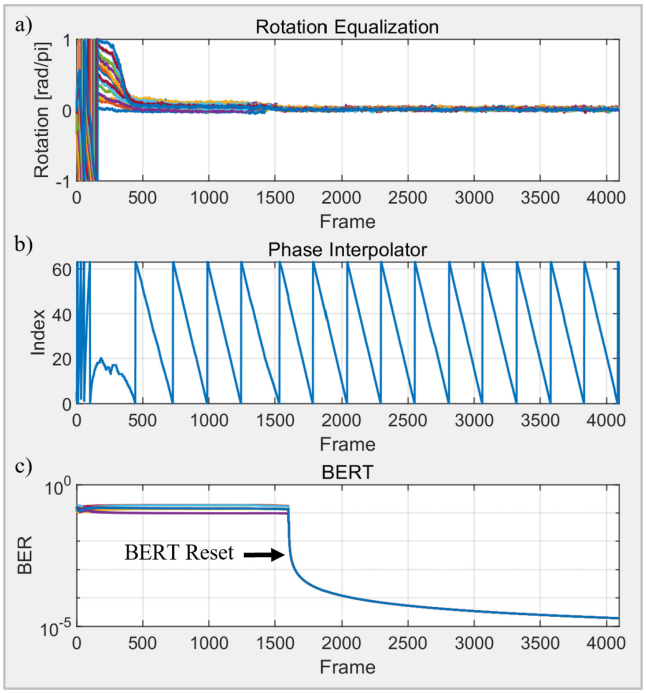

FIGURE 5. Measured synchronization procedure in the presence of 122*ppm* frequency offset.

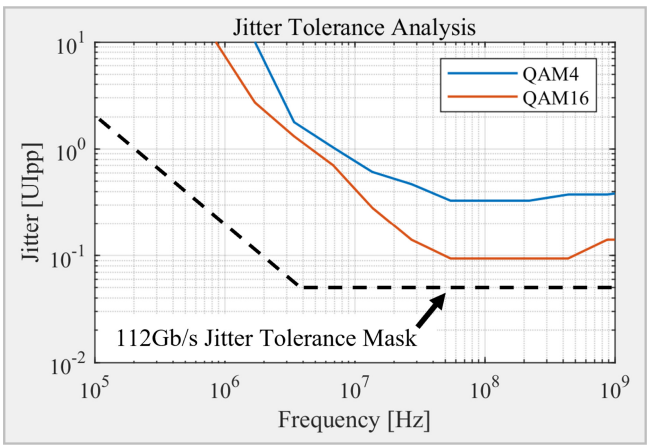

FIGURE 6. Measured jitter tolerance using QAM-4 and QAM-16 constellations assuming 112*GS*/*s*.

can no longer optimize power-loading to meet a BER of 10^{-3}. The figure shows that the system easily meets the jitter tolerance mask [26], and taking into account the higher operating frequency, closely matches simulation results from [15]. With 16-QAM, we attain an emulated data rate of $210Gb/s$. However, with optimized bit/power-loading and by increasing the constellation size, thereby reducing the jitter tolerance towards its mask, the test chip's data rate can exceed the $224Gb/s$ target.

A die photo is shown in Fig. 7. The area of the complete test chip is $2.3mm^2$. The encoder and decoder have areas of $0.14mm^2$ and $0.23mm^2$, respectively. This includes the 120 PRBS generators and BERTs, and PPNs with a length

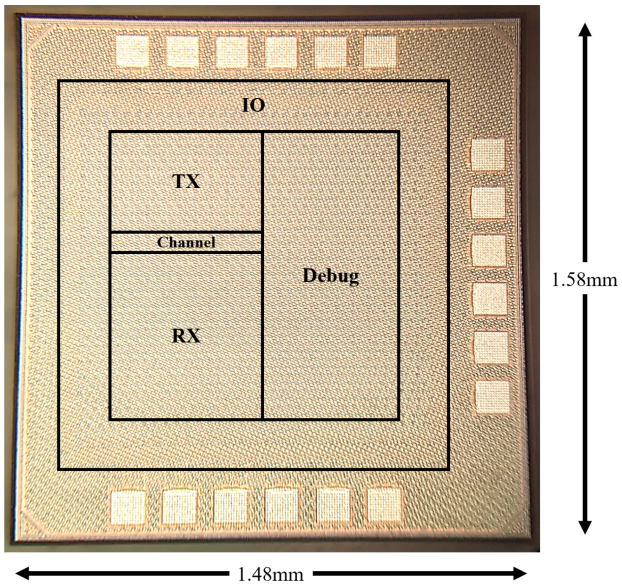

FIGURE 7. 22*nm* test chip die photo, overlayed with approximate module areas.

of eight. If we exclude this debugging circuitry and reduce the PPNs to a more typical length of four [14], the areas are reduced to $0.07mm^2$ and $0.17mm^2$, respectively. This is comparable to the DSP area of similar $22nm$ PAM transceivers [27]. These values are expected to reduce substantially with smaller technology. As indicated in [14], the complexity of FBMC is also comparable to that of DMT. This suggests that the complexity of the two multi-carrier schemes are competitive with conventional PAM modulation. Adopting techniques from [28] allows for an increase in the number of frequency bins without a notable rise in DSP power or area. However, latency increases linearly with the number of bins. To maintain a latency that is comparable to a PAM system, we limit the number of bins in the test chip to 15, as done in [14].

This test chip performs real-time emulation, and thus power consumption results are extrapolated to an assumed sampling rate of $112GS/s$ using the first-order approximation $P = \mu CV^2 f$ where μ is the transition activity, C is proportional to the relative number of gates, V is the supply voltage, and f is the clock frequency. The encoder and decoder are expected to consume $1.91pJ/b$ and $2.62pJ/b$, respectively, assuming a frame overlap factor of $O = 4$ [14] and a spectral efficiency of $5bits/sec/Hz$, which, as will be shown next, is a typical value that can be achieved with FBMC. However, without debugging circuitry, this is reduced to $1.53pJ/b$ and $1.98pJ/b$, respectively. These results are again comparable to similar $22nm$ PAM transceivers [27] and are also expected to improve with smaller technology.

B. MEASURED DATA RATE

The lab measurement setup is shown in Fig. 8. In this setup, the encoder and decoder are simulated in MATLAB, while real lab equipment is used to model the front-ends

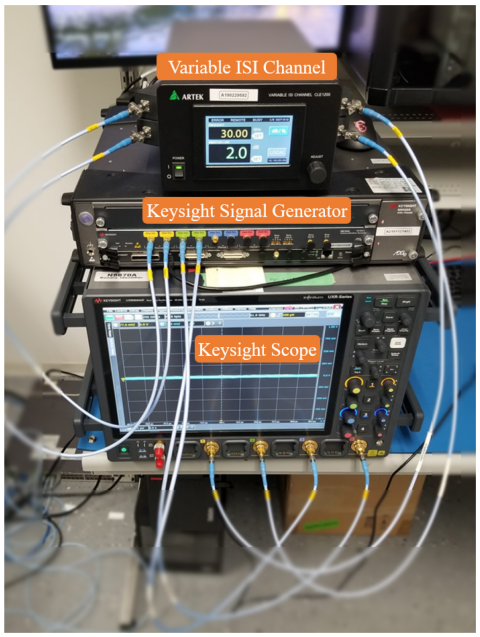

FIGURE 8. Lab measurement setup including a Keysight M8194A AWG, an Artek CLE1200 variable ISI channel, and a Keysight UXR0594AP real-time scope.

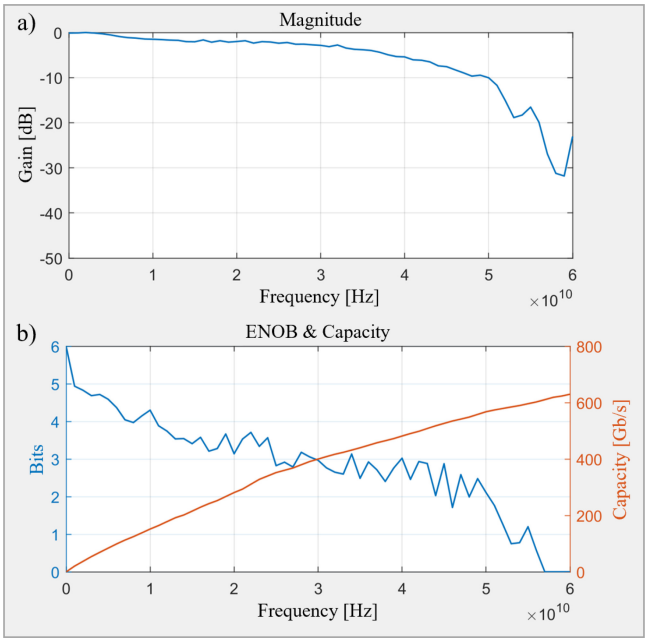

FIGURE 9. Lab measured 5*dB* at 40*GHz* channel including a) a magnitude response, b) an ENOB and capacity versus bandwidth analysis.

and the channel. This differs from the test chip, which implements the proposed encoder and decoder in silicon but emulates the analog circuits and their impairments in the digital domain. The offline encoder model generates a PAM, DMT, or FBMC waveform, assuming a sampling rate that is twice the signal's bandwidth. This waveform is upsampled to $120GS/s$ and transmitted using a Keysight M8194A Arbitrary Waveform Generator (AWG) with 8-bit resolution and $1.6V_{pp,diff}$ swing. The differential signal is fed through an Artek CLE1200 variable Inter-Symbol-Interference (ISI) channel and sampled by a Keysight UXR0594AP real-time scope with 10-bit resolution at $256GS/s$. The data is down-sampled back to the encoder's operating frequency and post-processed using the offline decoder model. Differential clock forwarding is used to aid recovery and minimize jitter. Equalization is performed in the encoder and decoder models. PAM applies 5-tap FIR equalization in the encoder and 25-tap FFE and 5-tap DFE equalization in the decoder. These values are typical for state-of-the-art transceivers, as discussed in [4], [19]. Least Mean Squared (LMS) is performed to optimize tap values. Multi-carrier applies the bit- and power-loading optimization described in Section II and uses adaptive decision-directed single-tap equalization described in [15] to equalize the 15 frequency bins. Due to equipment limitations, we do not apply CTLE or include crosstalk with any of the modulation schemes.

As mentioned, the encoder, AWG, oscilloscope, and decoder all assume different operating frequencies. As a result, re-sampling is performed at three locations along the signal path. Despite our best efforts, this introduced significant noise and necessitated limiting the channel attenuation to $5dB$ at $40GHz$ to maintain an average Effective Number of Bits (ENOB) of around three, as shown in Fig. 9. ENOB is calculated by sweeping a full-swing tone across frequencies. At each frequency, a windowed Fourier Transform isolates the tone and compares it to the total integrated noise to determine the SNR. This value is converted to ENOB using: $SNR = 6.02 \times ENOB + 1.76$ in dB. We perform a similar operation for capacity analysis, where the SNR of a full-swing tone is measured across frequencies, considering only the noise within the corresponding frequency bin. Then, the capacity per bin is calculated using Eq. (4) where B is the frequency bin's bandwidth, Γ is the gap to capacity which relates the symbol error probability $P_e \approx BER = 10^{-3}$, N_e is the average number of nearest neighbour symbols ($N_e = 4$ for QAM modulation), and Q is the Q-function [19].

$$C = B \times log_2\left(1 + \frac{SNR}{\Gamma}\right)$$
$$\Gamma = \frac{1}{3}\left[Q^{-1}\left(\frac{P_e}{N_e}\right)\right]^2 \tag{4}$$

Data rate results are shown in Fig. 10. We compare PAM-2, PAM-4, and PAM-8 to DMT and FBMC at a maximum signal bandwidth of $10GHz$, $20GHz$, $30GHz$, and $40GHz$, each time assuming $BER = 10^{-3}$, $N_{bin} = 15$, DMT's $N_{CP} \leq 4$, and FBMC's overlap of $O = 4$.

At $10GHz$ and $20GHz$ bandwidth, both DMT and FBMC achieve approximately the same data rate as PAM-8. However, at $30GHz$ bandwidth and beyond, PAM-8 no longer meets the BER requirements. As shown in Fig. 11, at $40GHz$ bandwidth, PAM-4 achieves a BER of $2 * 10^{-3}$, almost meeting the requirement. We assume that with more advanced equalization techniques, such as using a sliding-block DFE [4], we could lower the BER to meet the

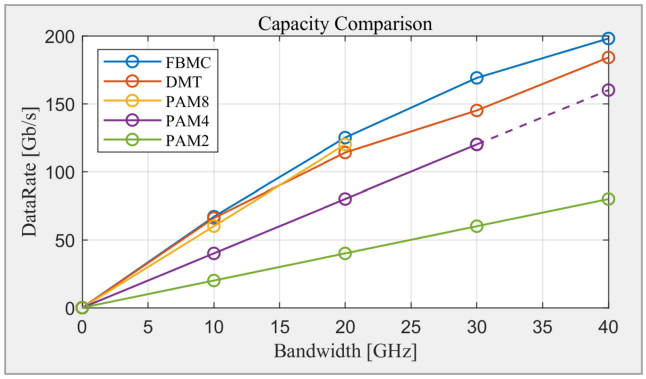

FIGURE 10. Measured data rate versus signal bandwidth results assuming 5 TX FIR taps, 25 RX FFE taps, 5 DFE taps, $N_{FFT} = 32$, $N_{CP} \leq 4$, $O = 4$, and $BER = 10^{-3}$.

requirement. In contrast, DMT and FBMC continue to follow a spectral efficiency of approximately $5bits/sec/Hz$. With a $40GHz$ bandwidth, PAM, DMT and FBMC achieve data rates of $160Gb/s$, $184Gb/s$, and $198Gb/s$, respectively. Thus, both multi-carrier systems outperform PAM in our setup, with FBMC achieving a data rate that is 8% higher than DMT and 24% higher than PAM-4. Our results closely match those of [29], [30] but with fewer frequency bins and thus significantly reduced latency. Furthermore, these results approach the target data rate of $224Gb/s$ but are limited by lab setup limitations. If the memory depth constraints of the AWG were overcome, allowing for the use of a 128-point FFT system, the data rate would improve, closing the gap to the $224Gb/s$ target. Moreover, should the setup limitations that necessitate resampling be addressed, thus enabling a 40% higher signal bandwidth from $40GHz$ to $56GHz$, the data rate would further increase.

C. SIMULATED DATA RATE

Previous setup limitations led to signal impairments not typically present in standard links. To circumvent these issues, the following section performs time-domain simulations with both the transmitter and receiver operating at $112GS/s$, accommodating a signal bandwidth of $56GHz$. We consider four high-attenuation channels, each originating from the publicly available IEEE 802.3 Ethernet Working Group [24]. The first channel (CH1) is a smooth $35dB$ at $56GHz$ channel, shown in Fig. 12. We apply $5.3mV_{rms}$ of random noise to consider common sources of impairments that degrade the SNR, such as random and deterministic noise and jitter, quantization, non-linearity, and crosstalk, achieving an overall ENOB of around 4 bits [19]. The second channel (CH2) is the same as the first but with a $20dB$ notch centred at $35GHz$. This impairment is generated using Eq. (5) where ω controls the center frequency, ζ the width, and η the depth.

Notches can occur from non-idealities in packaging and connectors, and reflections from impedance mismatch. Furthermore, insufficient clock shielding can introduce noise which degrades the SNR at in-band frequencies. These

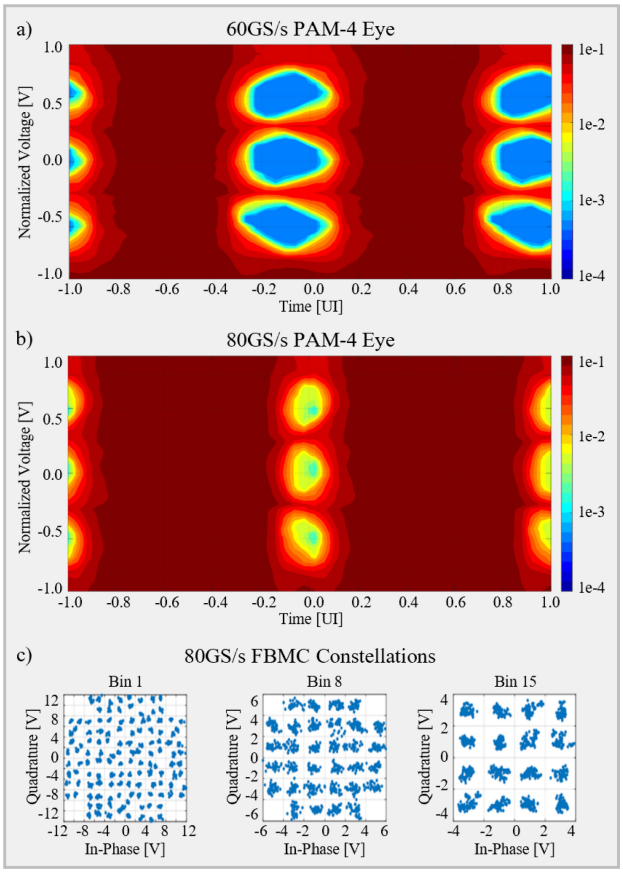

FIGURE 11. Lab measured PAM-4 BER contour plot at a) $60GS/s$ and b) $80GS/s$, and c) FBMC constellations at $80GS/s$.

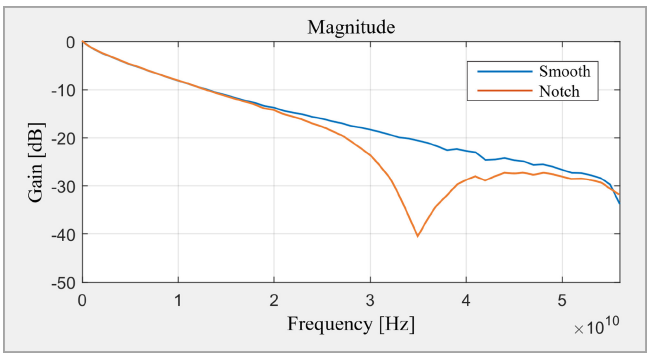

FIGURE 12. Simulated channel response for: a) simulated smooth $35dB$ at $56GHz$ channel, b) simulated $35dB$ at $56GHz$ channel with a $20dB$ notch at $35GHz$.

impairments are present in multi-drop bus memory applications [31] and are expected to become increasingly common in Ethernet applications as the industry strives to achieve even higher data rates and signal bandwidths. As such, this simulated notch serves as a proof of concept to highlight multi-carrier's ability to circumvent any impairment that leads to in-band frequencies with reduced SNR. The third (CH3) and fourth (CH4) channels are the same as the first two but with less noise, $3mV_{rms}$, corresponding to an average ENOB of around 5 bits. This analysis assumes the same

TABLE 1. Simulation results for (CH1) a smooth channel with $5.3mV_{rms}$ of noise, (CH2) a notch channel with $5.3mV_{rms}$ of noise, (CH3) a smooth channel with $3mV_{rms}$ of noise, (CH4) a notch channel with $3mV_{rms}$ of noise. We assume DMT and FBMC use $N_{FFT} = 128$.

	Smooth $5.3mV_{rms}$	Notch $5.3mV_{rms}$	Smooth $3.0mV_{rms}$	Notch $3.0mV_{rms}$
PAM	224 (4-PAM)	112 (2-PAM)	224 (4-PAM)	112 (2-PAM)
DMT	206	177	262	231
FBMC	221	194	286	258
Spectral Eff	$4.0b/s/Hz$	$3.5b/s/Hz$	$5.1b/s/Hz$	$4.6b/s/Hz$

encoder and decoder models as before but applies a 128-point FFT to highlight the upper-end performance improvements achievable by switching from PAM to multi-carrier modulation. Again, increasing the number of frequency bins can be achieved without significantly affecting the DSP power and area [28]. We do not apply CTLE. Simulation results are shown in Tab. 1. The link's average spectral efficiency is also displayed, by taking the maximum data rate of the three modulation schemes.

$$H(s) = \frac{s^2 + \zeta\omega s/\eta + \omega^2}{s^2 + \zeta\omega s + \omega^2} \tag{5}$$

For channel (CH1), $5.3mV_{rms}$ of noise produces a PAM-4 $224Gb/s$ link at $BER = 10^{-3}$. As such, we achieve an average spectral efficiency of $4.0bits/sec/Hz$, corresponding to $224Gb/s$ at $112GS/s$. Results show that FBMC achieves approximately the same data rate as PAM, with DMT not far behind. This is expected because, for smooth channels, PAM can outperform multi-carrier modulation due to its lower PAPR and thus higher average signal power [19], [32]. However, this gap is expected to close as the FFT size is increased.

When a notch is applied in (CH2), the channel's capacity drops by only 7%, but results in a 50% drop in PAM's data rate because PAM-4 no longer meets the BER requirement. Instead, we must apply PAM-2 modulation, transmitting half the number of bits at the same sampling rate. In contrast, both DMT and FBMC's data rate are less affected, reducing by only 14% and 12%, respectively. In this scenario, FBMC outperforms the two alternatives, achieving more than 1.7× the data rate of PAM-2 and 10% higher than DMT. This is also expected since PAM must equalize the notch, resulting in significant noise amplification.

The simulation results from (CH1) and (CH2) suggest that multi-carrier outperforms PAM only for channels with a spectral notch; however, Fig. 10 says otherwise. Thus, to verify the lab results, we reduce the noise of channels (CH3) and (CH4) and reperform the comparison.

In channel (CH3), the system can easily support PAM-4 but not PAM-8. As such, PAM does not support any increase in data rate. However, DMT and FBMC experience noticeable improvements, the latter achieving an average spectral efficiency of $5.1bits/sec/Hz$, or $286Gb/s$ at $112GS/s$. After applying a notch with channel (CH4), the

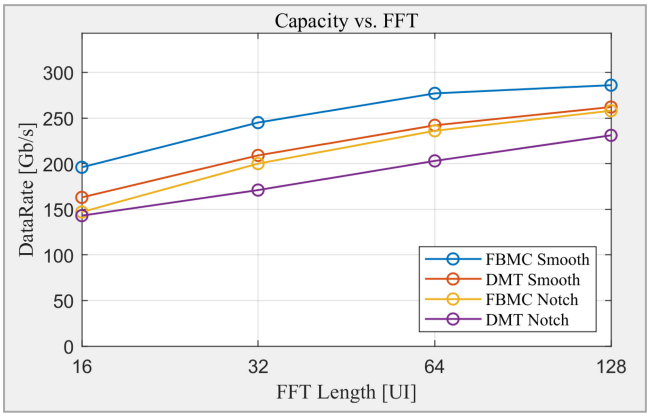

FIGURE 13. Simulated data rate versus FFT size for $BER = 10^{-3}$.

relative performance improvement is further increased. The channel's capacity drops by only 4%, but once again halves PAM's data rate as it no longer meets the BER requirement with PAM-4 and must switch to PAM-2. DMT and FBMC are again less affected, dropping their data rate by only 12% and 10%, respectively. With this channel, FBMC achieves a data rate improvement of more than 2.3× over PAM and 12% higher than DMT. Again, this improvement is expected to grow as the FFT size is increased.

As a result, and assuming a maximum signal bandwidth of $56GHz$, multi-carrier modulation can outperform PAM, even for smooth channels. The improvement depends on the link's spectral efficiency. In other words, conventional PAM modulation can only achieve coarse increments in spectral efficiency whereas DMT and FBMC can achieve fine increments in spectral efficiency. Under certain circumstances, PAM can under-utilize the link's available capacity. As a result, smooth channels with an average spectral efficiency of either 2.0, 4.0, 6.0, or $8.0bit/sec/Hz$, such as (CH1), will limit multi-carrier's improvement. However, channels with any other average spectral efficiency, such as (CH3) and Fig. 9, and channels with a notch, such as (CH2) and (CH4), will favour multi-carrier modulation. For example, a channel with an average spectral efficiency of $5.9bits/sec/Hz$ would only permit PAM-4 ($4.0bits/sec/Hz$), wasting $1.9bits/sec/Hz$. In contrast, DMT and FBMC could come close to the available capacity, outperforming the competition. When a spectral notch is applied, this improvement is further increased.

To analyze the effect of increasing the number of frequency bins, we repeat the capacity analysis for channels (CH3) and (CH4) while varying the FFT size from 16 to 128. As shown in Fig. 13, varying the number of bins affects the data rate by as much as 50%. However, as is reported in [19], we experience diminishing returns beyond $N_{FFT} = 128$. This result depends on the smoothness and slope of the channel's response. However, as discussed in [14], [15], multi-carrier's latency is proportional to the FFT size. Thus, there exists a tradeoff between improving performance and reducing latency. This compromise depends

on the application's requirements. Nevertheless, data rates at and beyond $224Gb/s$ are possible whether a 32, 64, or 128-point FFT multi-carrier system is employed.

Finally, for applications targeting a specific data rate, such as $224Gb/s$, DMT and FBMC's improved spectral efficiency can be used to reduce the required signal bandwidth or to meet more challenging link requirements. In other words, we can maintain the same data rate while reducing the required DAC and ADC sampling rate, or we can allow for channels with large spectral notches and/or higher levels of impairment.

V. CONCLUSION

This paper demonstrates the first silicon-verified FBMC encoder and decoder designed to emulate beyond $224Gb/s$ wireline communication. It also compares the performance of FBMC to PAM and DMT in three steps. First, the digital power and area consumption are compared using measured results from the manufactured test chip. Second, the data rate is determined using lab-measured results. And third, the performance when subject to notched channels is analyzed using simulation results. Finally, we present a method to emulate wireline links while reducing the emulator complexity and simulation time by one to two orders of magnitude over conventional over-sampled techniques. Our analysis indicates that given a smooth channel and an SNR which enables an average spectral efficiency of $4.0bits/sec/Hz$ at a bit-error rate of 10^{-3}, both DMT and FBMC perform similarly to a conventional PAM-4 link. However, when noise is reduced and a spectral notch is applied, thereby achieving an average spectral efficiency of $4.6bits/sec/Hz$, DMT and FBMC can outperform PAM by 2.1 and 2.3 times, respectively. In addition, we estimate FBMC's encoder and decoder power consumption at $1.53pJ/b$ and $1.98pJ/b$, respectively, and area requirement at $0.07mm^2$ and $0.17mm^2$, respectively, similar to DMT. These values are competitive with similar $22nm$ PAM transceivers. This highlights the considerable performance benefits of switching from PAM to DMT and especially FBMC.

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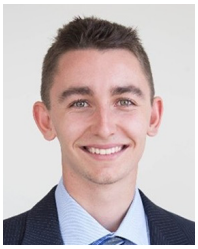

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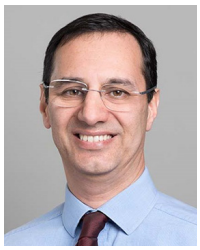

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