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A 0.69-mW Sub-Sampling NB-IoT Receiver Employing a Linearized Q-Boosted LNA

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***Abstract*—This paper presents a receiver for NB-IoT that eliminates the need for an RF local oscillator (LO) via a sub-sampling architecture. A pseudo-balun Q-boosted LNA provides sharp anti-aliasing filtering with a noise figure (NF) of 5.6 dB. A direct-coupling derivative superposition technique where low-V_t and thick-gate transistors with opposite non-linear characteristics are combined to improve the measured IIP3 by 7 dB to -18 dBm with little NF overhead. Fabricated in 65 nm CMOS, the entire receiver, including the LNA, a S/H circuit and a 10-bit SAR ADC, consumes only 0.69 mW while meeting NB-IoT specifications.**

***Index Terms*—NB-IoT, sub-sampling, receiver, LNA, linearity.**

I. Introduction

LOW-POWER, RF receivers (RXs) have become increasingly essential for IoT applications, as they enable extended battery life and facilitate the deployment of energy-efficient, large-scale wireless networks. The demand for low-power solutions is growing, particularly in applications such as environmental monitoring, smart agriculture, and asset tracking, where devices often operate in remote or hard-to-reach locations with limited access to energy sources. Narrowband IoT (NB-IoT) is a 3GPP-based standard designed to facilitate low-power communication via existing cellular infrastructure. Regrettably, even though NB-IoT employs low data rates (approximately 100 kbps) and bandwidth (180 kHz), which typically result in low-power implementations, its operation within LTE bands necessitates exceptional linearity and precision filtering to attenuate substantial interferers. Consequently, most NB-IoT receivers utilize conventional mixer-based architectures that demand frequency synthesizers consuming milliwatts of power [1]–[3], which is excessive for numerous emerging IoT applications.

To decrease overall RX power, previous research has explored the removal of power-intensive frequency synthesizers [4], [5]. Both cited instances employ thin-film bulk acoustic resonators (FBARs) to establish a frequency reference at approximately 2.4 GHz with restricted tunability, and utilize multiple reconfigurable dividers to supply desired clocks for mixers, ADCs, etc., operating at varying frequencies. Though suitable for targeted WBAN and ISM-band applications, meeting interference tolerance requirements proves challenging when directly applied to NB-IoT receivers, as depicted in Fig. 1. For example in [4] the RF signal is mixed with a low-frequency clock (77 MHz in the example) to accomplish channel selection before undergoing filtration via a Q-boosted FBAR-based filter. This process substantially heightens the dynamic range requirements, as an out-of-band (OOB) jammer

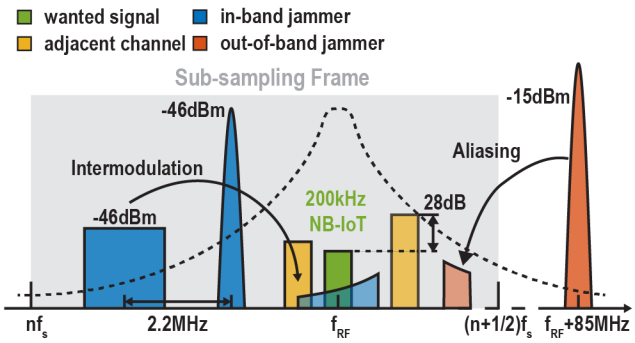

Fig. 1. NB-IoT spectrum and challenges for sub-sampling receivers.

as high as -15 dBm could be down-converted by the mixer clock's harmonics. [5] mitigates the OOB jammer issue by placing an FBAR band-selection filter at the antenna. However, since it employs a low-frequency clock in its second mixer, the in-band jammer rejection requirement of NB-IoT is difficult to fulfill due to the clock's harmonics. Moreover, these jammers can degrade the baseband SNR by mixing with the clock's phase noise if not sufficiently filtered. Thus, the RF jammer must be considerably attenuated at the first undesired harmonic of the down-conversion clock in an NB-IoT receiver.

An alternative to generating an RF LO and mixing entails directly digitizing the RF signal using an ADC with a low-IF sampling rate, while exploiting aliasing to effectively perform down-conversion to an IF for eventual I/Q demodulation [4], [6]. This sub-sampling approach is appealing, as it only requires a low-frequency, power-efficient clock generator. However, all other content surrounding integer multiples of the sampling clock, including both noise and potentially large interferers, will also alias down to the low-IF, as illustrated in Fig. 1. To address this, robust filtering is imperative before the sample-and-hold circuit to significantly attenuate this content; otherwise, the sub-sampling frequency must be large enough to avoid noise figure degradation, as demonstrated in [7], where a clock around 2 GHz is employed to down-convert Wi-Fi signals and consumes 27.8 mW.

Q-boosted LNAs offer high gain, narrow bandwidth, and relatively low power consumption within a single stage [4], [6], [8], making them an excellent candidate for the requisite filtering. However, the linearity of such amplifiers typically falls short of NB-IoT requirements due to the positive feedback of the cross-coupled pair (XCP), which partially cancels the conductance of the LC tank to concurrently enhance Q and

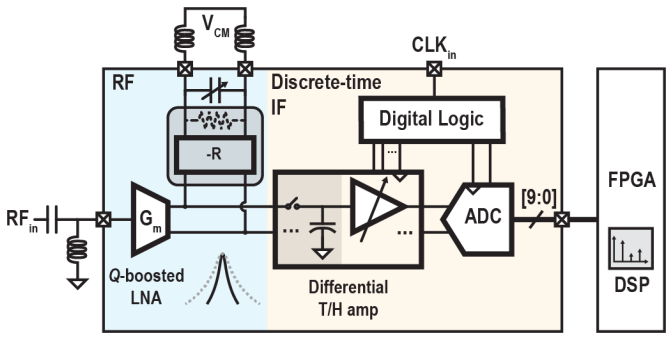

Fig. 2. System block diagram of the proposed sub-sampling receiver. The chip boundary is indicated using ☒.

gain. For instance, the designs in [4] and [8] achieved an IIP3 of -38.7 dBm and -43 dBm, respectively, while the NB-IoT standard demands better than -21.1 dBm. Owing to the differential nature of the cross-coupled pair, prior Q-boosted LNAs necessitate off-chip baluns, further exacerbating system noise figure degradation and escalating costs.

This paper introduces a linearized Q-boosted LNA that addresses the linearity issue by employing a derivative superposition method [9]. This method provides auxiliary devices that cancel the 3$^{\text{rd}}$-order coefficient of the main g_m devices. Normally, resistors and DC decoupling capacitors supply distinct bias voltages. However, when directly applied to a cross-coupled pair, these passive decoupling components diminish the quality factor of the resonant tank, thereby increasing power consumption for the same bandwidth (i.e., requiring more power from the XCP to cancel the increased effective parallel resistance from the low-Q passives to reach the same effective Q as before). To address this issue, the proposed LNA employs a combination of low-V_t and thick-gate transistors, thereby enabling direct coupling without the need for decoupling circuits, resulting in a superior overall quality factor and, as a result, a lower overall power consumption. Owing to the more than 40 dB gain from the LNA, the remainder of the RX chain can be designed with reduced power consumption and, crucially, without necessitating a power-intensive RF LO, all while satisfying the specifications of NB-IoT standard.

The organization of this paper is as follows: Section II computes the noise figure degradation resulting from sub-sampling and establishes specifications for various blocks. Section III delves into the design of the proposed linearized Q-boosted LNA. Section IV explores the discrete-time IF circuit, while Section V presents measurement results. Finally, Section VI offers conclusions.

II. Sub-sampling Receiver Noise Analysis

Fig. 2 depicts the proposed sub-sampling receiver architecture. Here, the incident RF signal undergoes 40 dB of amplification and band-pass filtering through a Q-boosted LNA. Subsequently, a track-and-hold (T/H) amplifier samples the LNA output, providing an additional gain ranging from 0 to 20 dB. A 10-bit SAR ADC quantizes the output and transmits the data to an off-chip FPGA for further processing. In contrast to traditional single-balanced mixers employing a 25% duty-cycle LO, which exhibit 3 dB of single-sideband NF [10], sub-sampling mixers may possess considerably higher NF due to noise aliasing.

The degradation in SNR due to the sub-sampling operation following an LNA can be determined by:

$$F = \frac{S_{\text{in}}/N_{\text{in}}}{S_{\text{out}}/N_{\text{out}}} = F_{G(f_0)} \sum_{k=-\infty}^{\infty} \frac{|G(f_0 + k \cdot f_s/2)|^2}{|G(f_0)|^2}, \quad (1)$$

where F represents noise factor of the cascaded system, f_0 is the center frequency of the RLC resonant tank, $G(f)$ is the gain of the LNA at frequency f, $F_{G(f_0)}$ is the noise factor of the LNA at frequency f_0, and f_s is the sampling frequency [6]. Given the overall quality factor Q of the resonant tank including negative impedance, the relative rejection of the LNA with respect to f_0 can be written as:

$$\left|\frac{G(f)}{G(f_0)}\right|^2 = \frac{1}{1 + \left(\frac{f - f_0}{f_0/2Q}\right)^2} \quad (2)$$

for f close to f_0, i.e., $|f - f_0| < 20f_0/Q$. As frequency deviates from f_0, especially towards DC, (2) starts to introduce error. Nonetheless, the band-pass filter shape of the LNA ensures that the summation in (1) is dominated by terms near the resonant frequency f_0 , rendering the approximation in (2) accurate for estimating the overall noise factor.

Using (1) and (2), the noise factor F can be expressed by:

$$\begin{aligned} F &= F_{G(\omega_0)} \sum_{k=-\infty}^{\infty} \frac{1}{1 + \left(k \cdot \frac{f_s}{f_0} \cdot Q\right)^2} \\ &= F_{G(\omega_0)} \cdot \frac{\pi f_o}{Q f_s} \coth\left(\frac{\pi f_o}{Q f_s}\right), \end{aligned} \quad (3)$$

where $\coth(x)$ is hyperbolic cotangent function and $x \coth(x) \to 1$ as $x \to 0$. Fig. 3 shows the noise figure degradation caused by sub-sampling by plotting $10\log_{10}(F/F_{G(\omega_0)})$ from (3) for $f_0 = 800$ MHz. Given Q higher than 150 and f_s larger than 40 MHz, sub-sampling degrades the NF by less than 0.3 dB, enabling good sensitivity and low power consumption. Given a 2 dB minimum SNR for demodulating NB-IoT baseband signals, the receiver necessitates a maximum noise figure NF_{max} of 10.8 dB at sensitivity including the loss of front-end passive components [11]. In this design, a 6 dB NF budget is allocated to the LNA, with the remaining 2 dB NF assigned to the subsequent blocks, leaving a 2.8 dB margin.

Although the NF_{max} requirement is readily satisfied at sensitivity by a sub-sampling receiver featuring a Q-boosted LNA, the receiver must also endure the presence of blockers. Fig. 4 illustrates the relative power levels of signals and noise at the ADC output for the system depicted in Fig. 2. As per [12] and Table I, the continuous-wave (CW) blocker can reach as high as -15 dBm at an 85 MHz offset; therefore, the in-band quantization noise of the ADC QN_{ADC} must be sufficiently minimal to ensure adequate dynamic range. In the presence of an OOB blocker exhibiting a power of $P_{Blocker} = -15$ dBm, the required SQNR of the ADC is:

$$\begin{aligned} SQNR_{\text{ADC}} =& P_{\text{Blocker}} - (P_{\text{in,REFSEN}} + 6) \\ &+ SNR_{\text{min}} - R_{\text{BLK}} + MG, \end{aligned} \quad (4)$$

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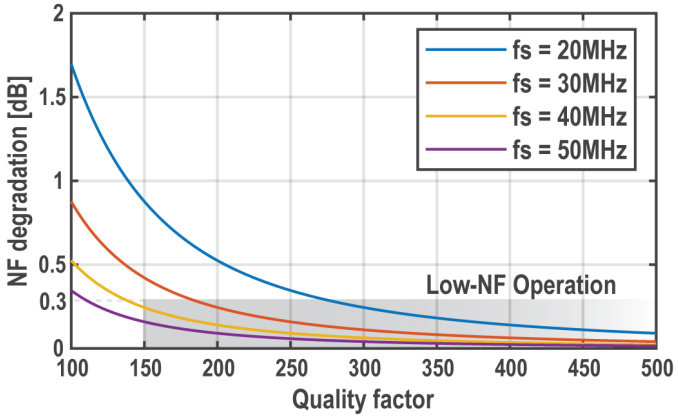

Fig. 3. Noise figure degradation introduced by sub-sampling.

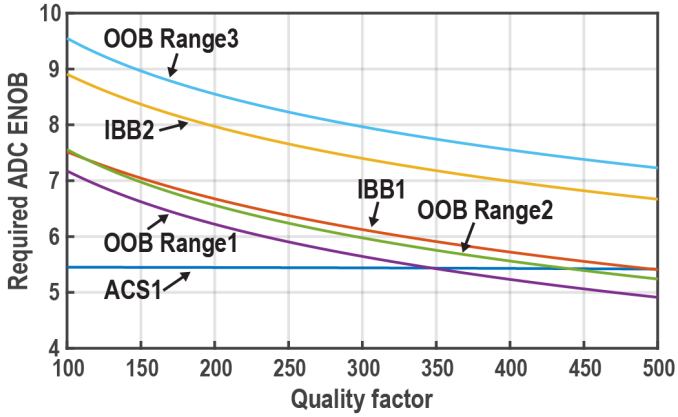

Fig. 5. Required ADC ENOB versus the quality factor of the Q-boosted LNA in different NB-IoT blocker tests.

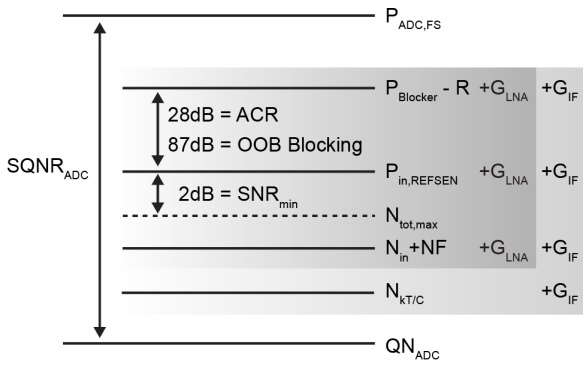

Fig. 4. Receiver noise planning with blocker presented.

where R_{BLK} is the blocker rejection that can be be estimated by (2) providing frequency offset Δf and Q; MG is the design margin in dB, setting to 16 dB in the following analysis to make the quantization noise contribute less than 10% of the total noise.

Fig. 5 shows the required $SQNR_{\text{ADC}}$ calculated from (4) under different test condition and Q. The following values are used for nearly all tests: sampling capacitor $C = 400$ fF, signal frequency $f_{\text{sig}} = f_0 = 850.5$ MHz, LNA gain $G_{\text{LNA}} = 40$ dB, and $G_{\text{IF}} = 20$ dB, except for $G_{\text{IF}} = 0$ dB in OOB test range 3. For tests involving non-zero bandwidth blockers, the PAPR is set to 9 dB, accounting for OFDM sub-carriers. Among all tests, the OOB blocker in range 3 imposes the most stringent requirement on the ADC dynamic range. However, with a sampling frequency $f_s = 42$ MHz, digital filtering provides over 20 dB of process gain $10\log_{10}(f_s/2BW)$, rendering the required ENOB less than 10 and 8 when Q exceeds 100 and 300, respectively. In the actual design, 10-bit SAR ADC is chosen to provide sufficient margin for both noise and dynamic range.

TABLE I
NB-IoT BLOCKER TESTS

	ACS1	IBB1	IBB2	OOB Blocker		
				Range 1	Range 2	Range 3
Psig [dBm]	-94.2	-102.2				
Pblocker [dBm]	-66.2	-56	-44	-44	-30	-15
Offset [MHz]	0.2	7.5	13	15	60	85
BW [MHz]	0.2	5	5	CW	CW	CW

III. Linearized Q-boosted Pseudo-balun LNA

A. Linearity Requirements in NB-IoT

As specified in [12], NB-IoT user equipment must pass a wideband intermodulation test, as shown in Fig. 1. An E-UTRA interferer signal with a 1.4 MHz bandwidth intermodulates with a continuous wave tone spaced 2.2 MHz away, generating a 3rd-order intermodulation product (IM3) that jams the wanted signal. The power of the input-referred IM3 is

$$P_{\text{in,IM3}} = 3P_{\text{in,jam}} - 2IIP3, \tag{5}$$

where $P_{\text{in,jam}}$ is the power of the interferer, equal to -46 dBm as specified in the standard. Because the IM3 bandwidth is larger than the signal bandwidth, the requirement of input-referred IIP3 is calculated under 6 dB of in-band noise floor degradation:

$$\begin{aligned} P_{\text{in,IM3}} &- 10\log_{10}(BW_{\text{E-UTRA}}) \\ &= (-174\,\text{dBm/Hz} + NF_{\max} + 6\,\text{dB}) \\ &\ominus (-174\,\text{dBm/Hz} + NF_{\max}), \end{aligned} \tag{6}$$

where $\ominus$ denotes minus operation in the linear domain and $NF_{\max}$ is the maximum required NF at reference sensitivity.

From (5) and (6), the minimum required input-referred IIP3 that maintains an output SNR of 2 dB is $\text{IIP3}_{\min} = -21.1$ dBm. NB-IoT imposes a similar linearity requirement on user equipment compared with 4G LTE standards that require IIP3 > -21.7 dBm, derived from the intermodulation test [13].

B. Linearity Analysis of an XCP

The linearity requirements derived above remain challenging for Q-boosted LNAs due to the positive feedback of the XCP used to generate negative impedance and large swing

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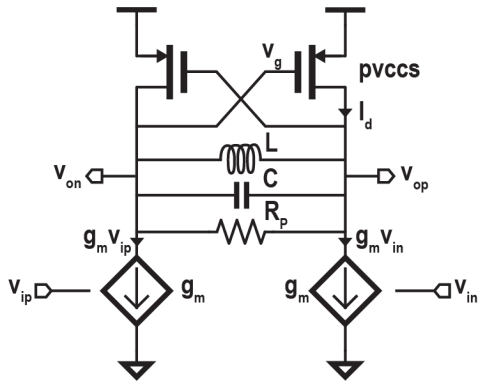


Fig. 6. Simplified model of Q-boosted LNA for IIP3 derivations.

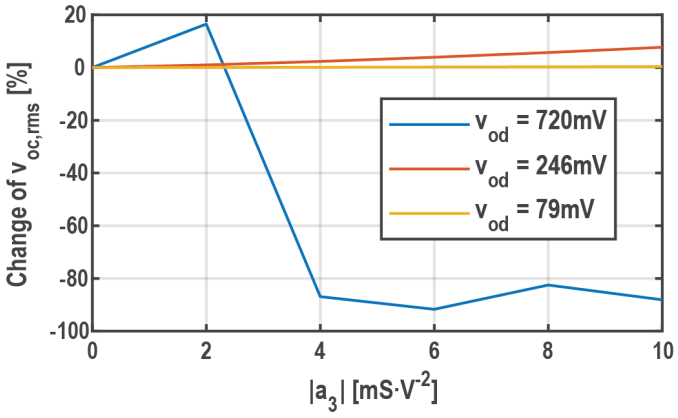


Fig. 7. Percentage change of the output common-mode voltage v_{oc} v.s. a_3 for different differential output voltage v_{od}.

at the output. The IIP3 of a Q-boosted LNA can be derived using a simplified model shown in Fig. 6. The transistors used in XCP can be modeled as 3rd-order polynomial voltage-controlled current sources (pvccs) given by

$$I_d = I_D + a_1 v_{gs} + a_2 v_{gs}^2 + a_3 v_{gs}^3, \tag{7}$$

where I_d, I_D, v_{gs} are the total drain current, the DC bias current, and the small-signal gate-source voltage, respectively. a_{1-3} represents coefficients of the pvccs. R_L is the equivalent parallel load resistor of the RLC resonant tank.

The in-band IIP3 $v_{p,\text{IIP3,IB}}$ at resonance frequency $f_c = 1/(2\pi\sqrt{LC})$ can be determined by first writing KCL equations at two output nodes and replacing the output voltage with $v_{op} = (v_{oc} + v_{od})/2$ and $v_{on} = (v_{oc} - v_{od})/2$:

$$\frac{1}{4}a_3 v_{oc}^3 + \frac{1}{2}a_2 v_{oc}^2 + \left(a_1 + \frac{3}{4}a_3 v_{od}^2\right) v_{oc} + \frac{1}{2}a_2 v_{od}^2 = 0, \tag{8}$$

$$\frac{1}{4}a_3 v_{od}^3 + \left(a_1 + a_2 v_{oc} + \frac{3}{4}a_3 v_{oc}^2 - \frac{2}{R_L}\right) v_{od} + g_m v_{id} = 0. \tag{9}$$

Directly solving (8) and (9) to obtain an intuitive closed-form expression for $v_{od} = f(v_{id})$ is challenging. From Fig. 7, simulation results show that v_{oc} changes less than 1% while sweeping a_3 for the peak of v_{od} less than 79 mV. This corresponds to the condition of two tones separated by 2.2 MHz with $P_{\text{in}} = -40$ dBm. Thus, for NB-IoT with $P_{\text{in}} = -46$ dBm, it is safe to assume that all terms associated with a_3 can be neglected in (8).

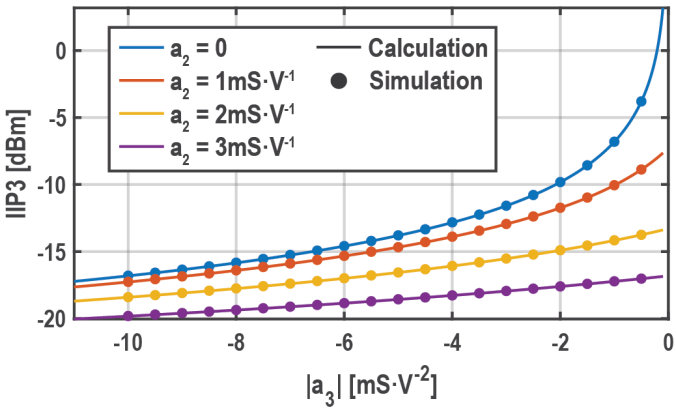


Fig. 8. Comparing the IIP3 results obtained from calculations using (13) with those from simulations using the circuit in Fig. 6.

Letting $a_3 = 0$, v_{oc} can then be expressed in the following equation:

$$v_{oc} = \frac{-a_1 + a_1\sqrt{1 - a_2^2 v_{od}^2/a_1^2}}{b} = -\frac{a_2}{2a_1}v_{od}^2 + O\left(v_{od}^4\right). \tag{10}$$

Neglecting $O\left(v_{od}^4\right)$ and substituting (10) into (9) enables v_{od} to be written in terms of v_{id}:

$$v_{od} = \frac{g_m}{2/R_L - a_1}v_{id} + \left(\frac{a_2^2}{2a_1} - \frac{a_3}{4}\right)\frac{g_m^3}{\left(2/R_L - a_1\right)^4}v_{id}^3. \tag{11}$$

The in-band IIP3 is given as

$$v_{p,\text{IIP3,IB}} = \sqrt{\left|\frac{16\left(2/R_L - a_1\right)^3}{3g_m^2\left(2a_2^2/a_1 - a_3\right)}\right|}. \tag{12}$$

For any two tones away from f_c, L and C reduce the magnitude of the output impedance and thus the swing at the output, making the intermodulation product smaller than that generated by two tones in proximity of f_c. A generalized expression of IIP3 is given by

$$IIP3 = IIP3_{\text{IB}} + R_{\text{tone1}} + \frac{R_{\text{tone2}}}{2}, \tag{13}$$

where $R_{\text{tone1,2}}$ denotes the rejection of tone 1 and 2 with respect to the gain at f_c. Fig. 8 compares the IIP3 predicted with (13) to simulation results from SpectreRF. The simulated IIP3 is extrapolated when P_{in} = -46 dBm and Δf = 2.2 MHz. It demonstrates that (13) remains accurate under NB-IoT specifications.

C. Proposed Linearity-Enhanced Q-Boosted LNA

Fig. 9 illustrates the detailed implementation of the proposed LNA. The shaded area on top represents the proposed linearized XCP, which generates negative impedance primarily through M_3, while $M_{3\text{aux}}$ serves as an auxiliary device that cancels the 3rd-order coefficient of M_3, as shown in the top of Fig. 10. Normally M_3 and $M_{3\text{aux}}$ are designed using the

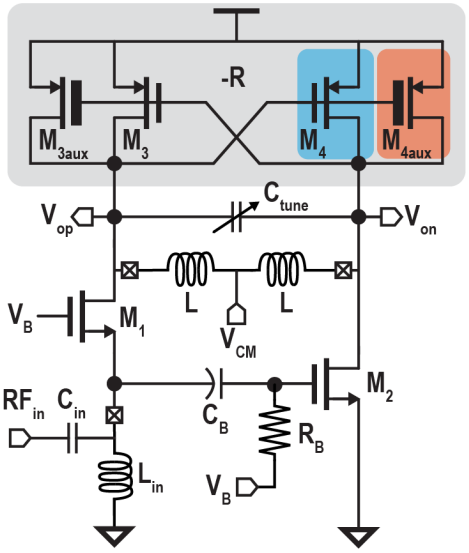


Fig. 9. Schematic of the proposed Q-boosted LNA.

same transistor type and would require explicit Q-degrading DC biasing [9], but in this design by using low-V_t ($V_t \approx 300$ mV) and thick-gate devices ($V_t \approx 500$ mV), they can be DC coupled, thereby maximizing the quality factor of the resonant tank. The power consumption when boosting the Q factor to 350 is reduced by more than 26% compared to using a separate RC-based DC bias in post-layout simulations.

Due to the lack of separate bias tuning on the auxiliary path, the impact of process variation on the proposed linearization technique is shown in Fig. 10. In the middle part of Fig. 10, 1000 Monte-Carlo simulations of a_3 with cancellation are conducted with global process and local mismatch variation enabled. Each simulation plots a a_3 curve with 1% opacity; darker region represents more overlaps across simulations and thus a_3 is less susceptible to process variation if the bias voltage V_{sg} is set to such region. When V_{sg} is set to 0.51 V, the distribution of a_3 is shown at bottom of Fig. 10 where a_3 has smallest variation. With the optimum bias voltage, the Monte-Carlo simulation result of IIP3 with global process variation is shown in Fig. 11, demonstrating IIP3 values exceeding -18 dBm and -21 dBm for 84% and 97.5% of trials, respectively, both satisfying NB-IoT specifications. The table on the right side summarizes the simulation result at each corner with local mismatch variation enabled. The proposed LNA fails to meet the NB-IoT spec in the FF corner, while meeting the spec in the rest of the corners. As for temperature variation, Fig. 12 indicates that the proposed technique remains effective from $-40°$C to $85°$C.

Interestingly, it can be seen that from (12) that the XCP can theoretically achieve an infinitely large IIP3 when $a_3 = 2a_2^2/a_1$. However, this is not a practical design choice due to the positive peak of a_3 occurring when the transistor's V_{SG} is biased around the threshold voltage, leading to susceptibility to process variation. Additionally, the quality factor Q_{ind} of the off-chip inductor L is not accurately modeled, preventing precise prediction of a_1.

Fig. 13 shows the impact of various design parameters on

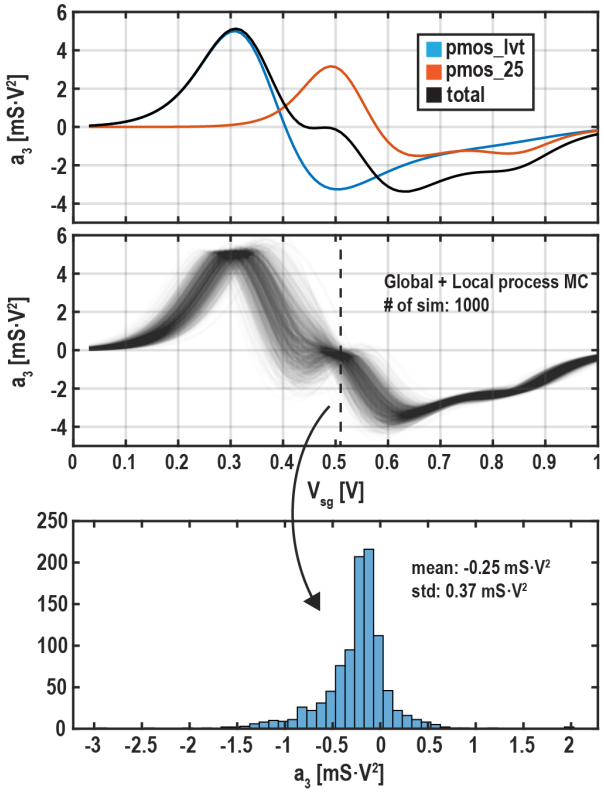
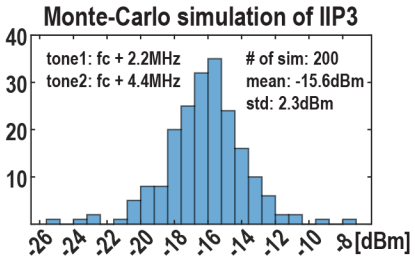


Fig. 10. Effect of process variation on the proposed linearization technique.



	IIP3 [dBm]	
	μ	σ
MC	-15.6	2.3
TT	-14.87	0.38
FF	-23.39	0.27
SS	-13.16	0.87
SF	-14.47	0.62
FS	-16.15	0.67

Fig. 11. Monte-Carlo simulation of IIP3 in global and local process corners.

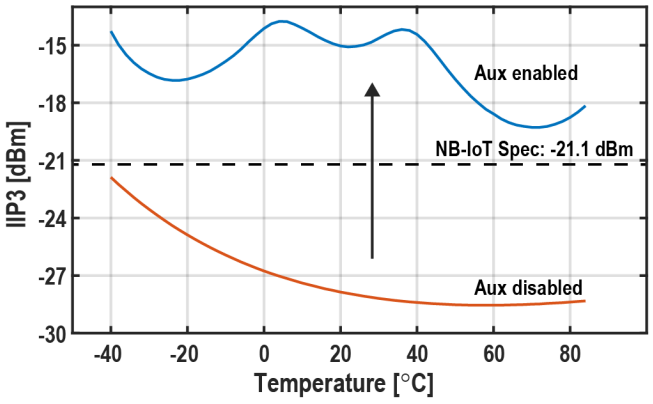


Fig. 12. IIP3 of the proposed LNA vs. temperature.

IIP3. Fig. 13(a) demonstrates that increasing Q_{ind} from 40 to 45 shifts the optimal output common-mode bias voltage V_{CM} by 3.5 mV, as less a_1 is needed to compensate for the loss

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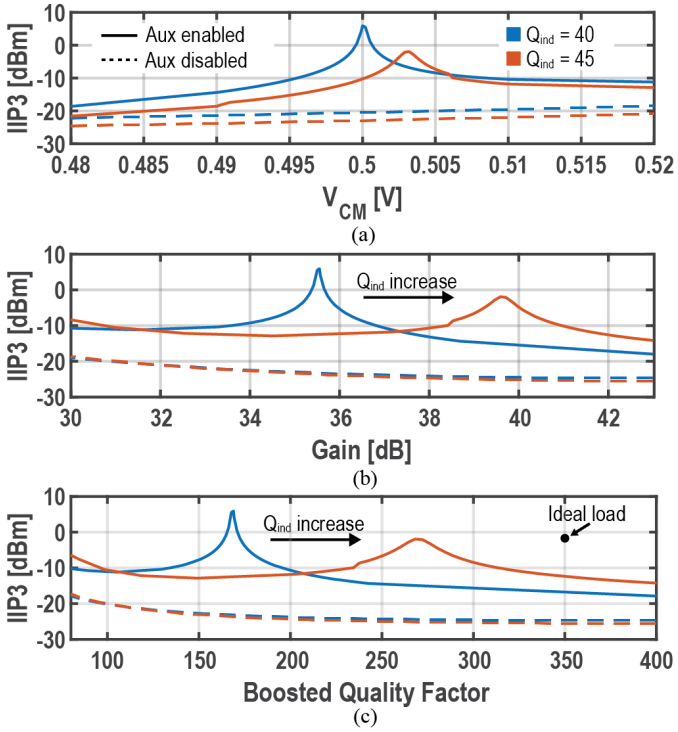

Fig. 13. Simulated IIP3 of the proposed LNA versus (a) output common-mode bias voltage, (b) small-signal gain and (c) equivalent quality factor after Q-boosting for different Q_{ind}.

in a higher Q inductor. Fig. 13(b) and (c) indicate the same trend: higher Q_{ind} corresponds to larger optimal values of gain and boosted quality factor. Although IIP3 is sensitive to both V_{CM} and Q_{ind}, the proposed linearization technique exhibits an improvement from 3 dB to 26 dB compared to a traditional XCP, as shown by the dashed lines in Fig. 13. Consequently, the LNA is designed to operate within the flat region of the IIP3 curve, which accommodates greater Q_{ind} uncertainties, rather than at the tiny tip.

When replacing the Q-boosted load with an pure LC load with the same $Q = 350$, the balun LNA has -2 dBm IIP3, proving that the XCP degrades the linearity by more than 20 dB. By zeroing a_3 of the XCP, the LNA achieves an IIP3 of -15.2 dBm in simulation, a 9.8 dB improvement from -25 dBm, by employing the thick-gate auxiliary device.

In addition to linearity, the LNA's NF also constrains receiver performance. As illustrated in Fig. 9(a), the proposed LNA incorporates on-chip single-ended to differential conversion by feeding the signal to the source and gate of M_1 and M_2, respectively. This topology circumvents the need for an off-chip balun, which incurs additional loss preceding the LNA, leading to an NF improvement compared to [8].

To analyze the NF, the block diagram of the LNA in Fig. 14, representing KCL equations written on the input and output nodes, can be utilized. The gain from each source to the output can be calculated using Mason's gain formula. Assuming $g_m r_o >> 1$, loop L_1 dominates since L_2 and L_3 are attenuated by r_o. The gain from noise sources to the output

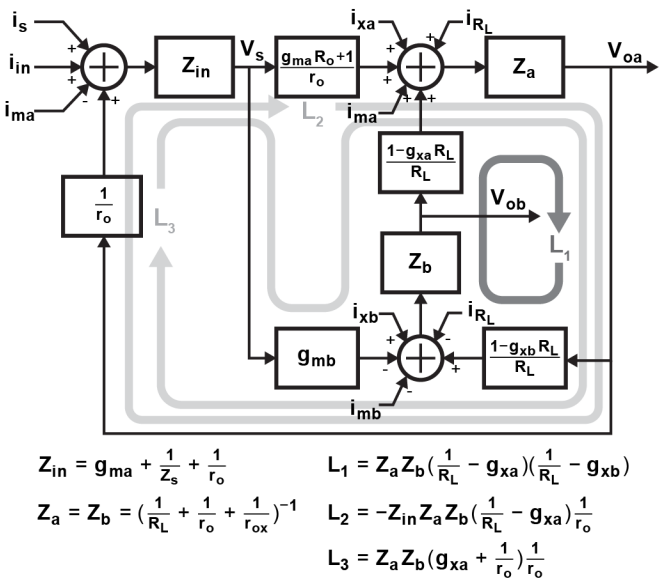

Fig. 14. Block diagram of the proposed LNA shown in Fig. 9(a).

can be represented as:

$$\begin{aligned} |Z_{T,i_{in}}| &= \frac{2g_m Z_{in} Z_o}{1 + Z(\frac{1}{R_L} - g_x)}, \\ |Z_{T,i_{ma}}| &= \frac{Z_o(1 - 2g_m Z_{in})}{1 + Z(\frac{1}{R_L} - g_x)}, \\ |Z_{T,i_{mb}}| = |Z_{T,i_{xa}}| = |Z_{T,i_{xb}}| &= \frac{Z_o}{1 + Z_o(\frac{1}{R_L} - g_x)}, \end{aligned} \tag{14}$$

where $Z_a = Z_b = Z_o$, $g_{m1} = g_{m2} = g_m$, and $g_{m3} = g_{m4} = g_x$. Under the impedance matching condition $Z_s = 1/g_m$, the common-gate transistor M_1 does not contribute to the output noise, as its noise current i_{m1} appears entirely as a common-mode voltage at the output, rendering $|Z_{T,i_{ma}}| = 0$. Using equation (14), the noise factor can be written as:

$$\begin{aligned} F &= 1 + \gamma + \frac{1}{g_m}(\gamma g_m + 2\gamma g_x + \frac{4}{R_L}) \\ &= 1 + 2\gamma + \frac{1}{g_m}(\frac{(2\gamma + 3)C\omega_c}{Q_{\text{ind}}} - \frac{2}{G}\sqrt{\frac{g_m}{Z_{\text{ant}}}} - \frac{1}{r_o || r_{ox}}), \end{aligned} \tag{15}$$

where G represents the available voltage gain of the LNA. Equation (15) suggests that the NF increases when the quality factor of the inductor Q_{ind} decreases and G rises, as they necessitate larger g_x values to compensate for the resonant tank's loss to achieve the same overall Q. When lower NF is needed, power can be increased, or the Q of the input matching network can be increased, with a trade-off of reducing the operating frequency range.

For $G = 40$ dB and $f_c = 750$ MHz, the transconductance of the input NMOS g_{m1} is set to 1.6 mS, ensuring the NF is under 5.5 dB for $Q_{\text{ind}} = 40$ as displayed in Fig. 15, while consuming 81 μA in simulation. In the presence of blockers, the LNA achieves 5.9 dB blocker NF in simulation at 85 MHz offset specified in OOB Blocker Range 3 shown in Table I. Consequently, the LNA attains low power consumption

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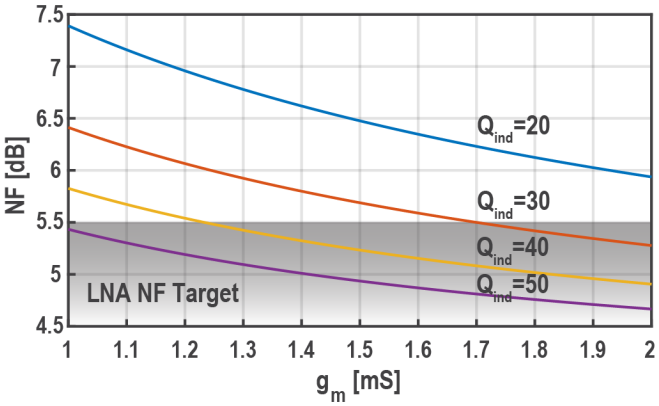

Fig. 15. NF of the LNA given different g_m and inductor quality factor Q_{ind}.

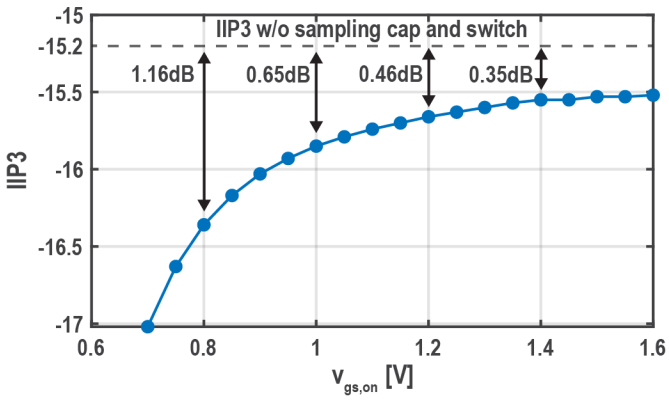

Fig. 17. Simulation results of IIP3 v.s. $v_{gs,on}$ of the sampling switches.

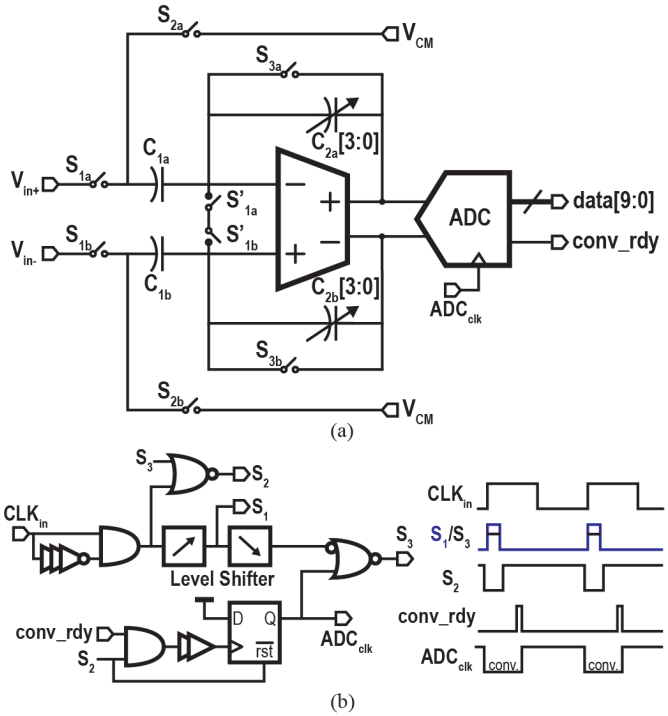

Fig. 16. The discrete-time IF circuit of the proposed RX including (a) a track-and-hold (T/H) amplifier and (b) a timing generation circuit and its waveforms.

and satisfactory linearity and noise performance for NB-IoT applications.

IV. Discrete-time IF

After being filtered and amplified by the Q-boosted LNA, the signal is sampled by the T/H amplifier, which provides additional gain G_{IF} to drive the ADC. This section will discuss the T/H amplifier design, taking into account linearity, noise, speed, timing generation circuit, and the ADC.

A. T/H amplifier

The T/H amplifier [14] is implemented as shown in Fig. 16(a). The bandpass-filtered signal is sampled on $C_{1(a,b)}$ by switches $S_{1(a,b)}$ while $S_{2(a,b)}$ are turned off. During the hold phase, $S_{1,3(a,b)}$ are turned off and $S_{2(a,b)}$ are turned on, transferring charge from $C_{1(a,b)}$ to the 4-bit capacitor banks, $C_{2(a,b)}$, which control the gain from 0 dB to 20 dB. Proper timing is generated by a set of logic gates and level shifters depicted in Fig. 18(b). The input clock, CLK_{in}, generates a pulse with a width controlled by delay cells. This pulse sets $S_{2(a,b)}$ to "0" and $S_{1(a,b)}$ to "1" through a NOR gate and an "up" level shifter, respectively. The falling edge of $S_{2(a,b)}$ arrives earlier than the rising edge of $S_{1(a,b)}$ by making the delay of the NOR gate smaller than the level shifter. The pulse at $S_{1(a,b)}$ propagates through a "down" level shifter and a NOR gate with an inverting input on one side, toggling the "reset" switch $S_{3(a,b)}$ on and off. The subsequent edge of $S_{3(a,b)}$ returns to the top NOR gate and pulls $S_{2(a,b)}$ up. This architecture ensures non-overlapping operation of track and hold. Signal-dependent charge injection is minimized by connecting more NMOS fingers to $S'_{1(a,b)}$ compared to $S_{1(a,b)}$, causing $S'_{1(a,b)}$ to turn off slightly earlier than S1, a technique known as bottom plate sampling [15]. The ADC clock is supplied by a series of an AND gate, delay cells, and a flip-flop. The following edge of the ADC clock is ensured to arrive before the rising edge of $S_{3(a,b)}$ by properly controlling the delay and the right-most NOR gate.

During the track phase, the sampling capacitors connect to the output of the XCP through $S_{1(a,b)}$. These switches significantly influence overall system linearity. As illustrated in Fig. 17, the sampling circuit degrades IIP3 by 0.65 dB, 0.46 dB, and 0.35 dB when $v_{gs,on}$ equals 1 V, 1.2 V, and 1.4 V, respectively, in simulations. The curve's slope becomes almost flat after $v_{gs,on}$ exceeds 1.4 V. Thus, in the design, these sampling switches are driven by a 1.4 V_{pp} level-shifter-generated control signal to enhance linearity in a reliable manner, transitioning from hot carrier injection-based voltage limits to time-dependent dielectric breakdown voltage limits for transistors biased in the triode region. For a common-mode voltage $V_{cm} = 0.55$ V, the level shifter's supply voltage must be 1.95 V, causing the switch driver circuit to consume 26% more power compared to using a 1 V_{pp} square wave while only improving the IIP3 by 0.3 dB. However, due to the sub-sampling architecture, the driver's power consumption is only 73 μW, which is 11% of the total power consumption of the

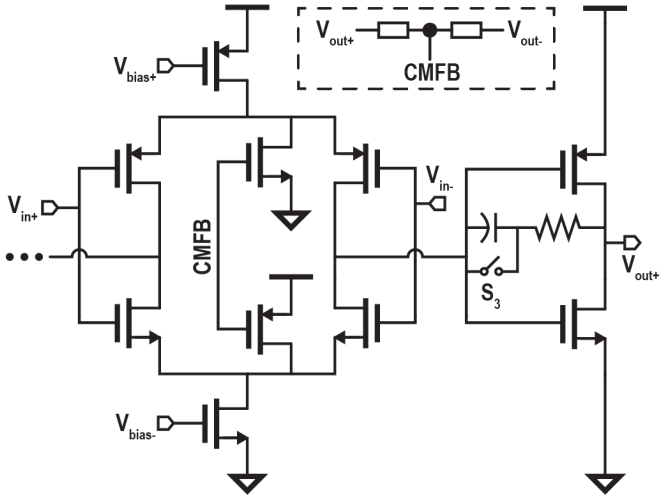

Fig. 18. Schematic of the OTA used in the T/H amplifier.

receiver. Consequently, the net power increase of the switch-driving level-shifters in terms of the entire system remains negligible.

The input-referred noise of the differential T/H amplifier can be expressed in the following equation from [14]:

$$\overline{v_{n,in}^2} \cong \underbrace{\frac{2kT}{C_1}\left(1+\frac{C_2+C_{par}}{C_1}\right)}_{\text{Track}} + \underbrace{\left(\frac{C_2}{C_1}\right)^2 \frac{\alpha}{\beta}\cdot\frac{2kT}{C_{eq}}}_{\text{Hold}}, \quad (16)$$

where C_{par} is the parasitic capacitance from the OTA input summing node to the ground, α is the ratio of the input-referred noise PSD of the OTA to that of a resistor, $\beta = C_2/(C_1+C_2+C_{par})$ is the circuit's feedback factor, and $C_{eq} = C_{\text{in,ADC}} + (1-\beta)C_2$. Unlike a single-stage OTA with the excess noise factor $\alpha_1 = \overline{v_{\text{n,in,OTA}}^2} G_m/(4kT\Delta f)$, the excess noise factor of a 2-stage OTA, α_2, can be derived from

$$\overline{v_{\text{n,in,OTA}}^2} = 4kT \cdot \underbrace{\alpha_2 \cdot \left(g_{m2}r_{o1} + \frac{1}{g_{m1}r_{o1}}\right)}_{\alpha} \frac{1}{G_m}\Delta f, \quad (17)$$

where g_m and r_o represent the transconductance and output impedance of a single stage, respectively, and subscript 1 or 2 denotes the stage number. G_m is the total transconductance of the OTA. To maximize g_m/I_D efficiency and output driving capability, the OTA, depicted in Fig. 18, employs a 2-stage inverter-based structure. The OTA achieves an input-referred noise PSD of 3.3 $\text{nV}/\sqrt{\text{Hz}}$ for its differential half-circuit in simulation, with a calculated $\alpha_2 = 0.79$. With $C_1 = 400$ fF, $C_2 = 40$ fF at maximum gain, and $C_{\text{in,ADC}} = 300$ fF, the simulated $\overline{v_{\text{n,in,PSD}}^2} = 2.06\ \text{fV}^2/\text{Hz}$, degrading the system NF by 1.1 dB.

The unity gain-bandwidth requirement of the OTA is 620 MHz in simulation, satisfying the settling time constraint by making the hold phase nine times longer than the track/reset phase. However, the short duration of the reset phase creates a problem in which the OTA, biased at low current to minimize power consumption, is too slow to clean up the residue from previous sampling instances, which could be more than 3 mV

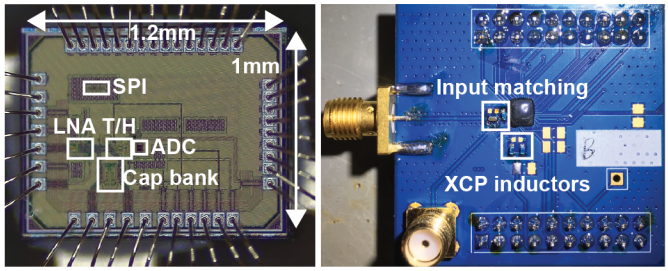

Fig. 19. Photos of the die and its PCB package.

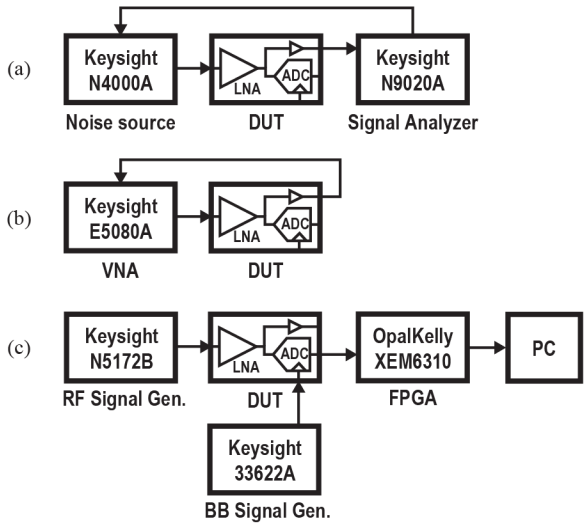

Fig. 20. Measurement setup for (a) noise figure, (b) S.-parameters and (c) sensitivity.

in the worst case. To solve this issue, an additional switch across the OTA's Miller compensation capacitor is added to periodically reset the dominant compensation capacitor during the track/reset phase. This significantly helps reduce the residue from previous samples to less than 100 nV and enables lower settling time without consuming extra power.

Post layout simulation demonstrates that the LNA and track-and-hold amplifier achieve a 6.7 dB noise figure and -15.9 dBm of IIP3 while consuming 395 uW. The proposed design offers a satisfactory performance in terms of noise, linearity, and power consumption, making it suitable for NB-IoT applications.

B. ADC

The 10-bit SAR ADC is implemented using the structure proposed in [16], and features a total input capacitance of 300 fF to further minimize the gm requirement of the OTA. With 1000x oversampling, 14b of ENOB is achieved to accommodate up to a -15 dBm OOB jammer.

V. Measurement Results

The chip is fabricated in 65 nm technology, occupies 1.2 mm^2, as depicted in Fig. 19(a), and is wirebonded to a FR4 PCB shown in Fig. 19(b). The majority of the on-chip area consists of digital I/O pads for ADC outputs and RF/analog

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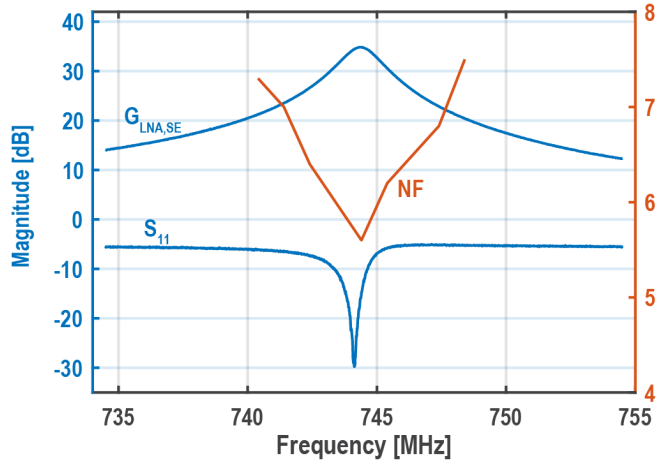
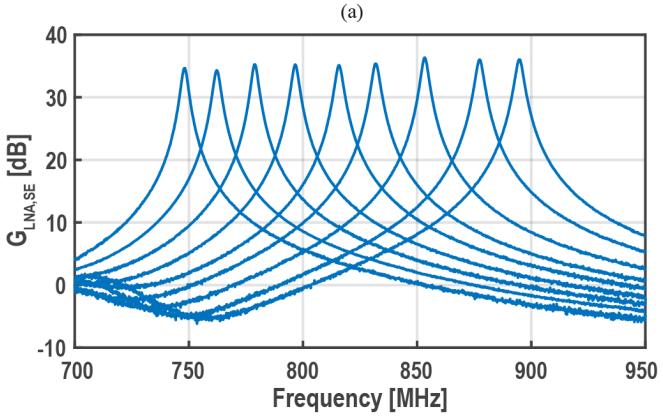
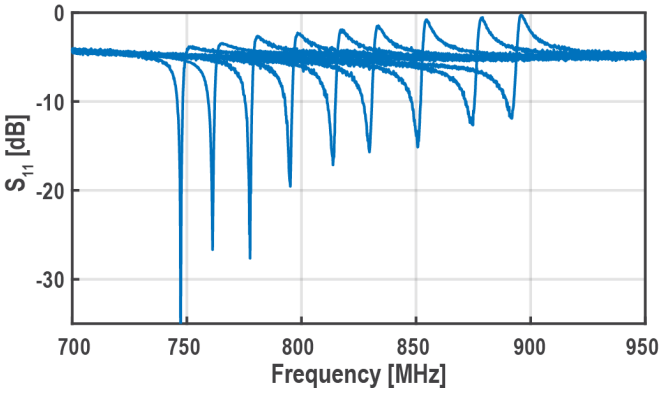


(a)



(b)



(c)

Fig. 21. Measurement of (a) the input matching S_{11}, single ended LNA gain $G_{\text{LNA,SE}}$ and NF, (b) LNA gain with different center frequency and (c) S_{11} with different center frequency.

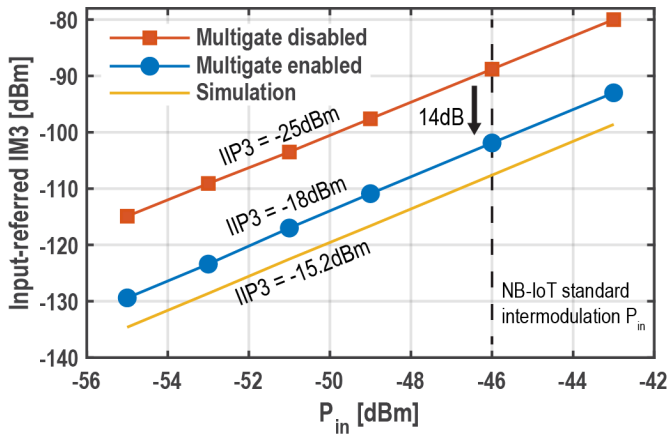
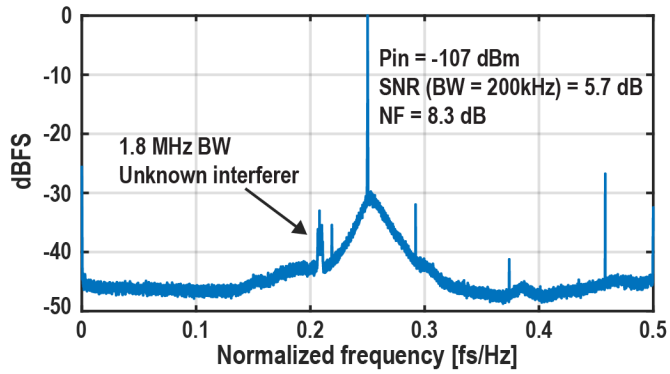
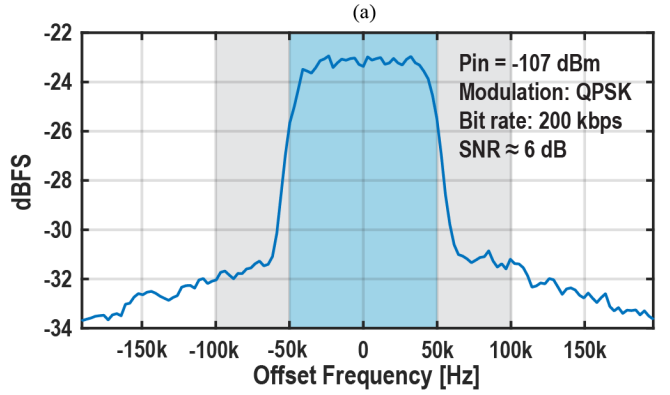


Fig. 22. Measured IIP3 improvement with the proposed multi-gate technique.



(a)



(b)

Fig. 23. Spectrum at the output of ADC with (a) a sinusoidal input and (b) a 200 kbps QPSK modulated input. The offset frequency is defined relative to $f_s/4$.

pads for signals and power supplies, as the inductor resides on the PCB. A 27 nH Coilcraft 0402DC series inductor is used for input matching, while two 8.1 nH Murata LQW15 series inductors serve the XCP. Fig. 20 illustrates the measurement setup for noise figure, S-parameters, and sensitivity.

Fig. 21 and Fig. 22 present the measurement results for the proposed LNA. As observed in Fig. 21(a), the LNA achieves a single-ended gain ($G_{\text{LNA,SE}}$) of 34.7 dB, S_{11} of -23.8 dB, NF of 5.6 dB, and a bandwidth of 1.64 MHz. The center frequency and bandwidth remained consistent for over two weeks of data collection without recalibration, verifying that the Q-boosting positive feedback was not overextended. Fig. 21(b)(c) demonstrates the LNA's ability to operate at different center frequencies. As frequency increases, input matching starts to degrade due to C_{gd} of M2 in Fig. 9, which would result in a rise in NF. Nevertheless, higher frequencies employ fewer on-chip capacitors with lower Q due to controlling switches, causing the NF to increase by less than 1.7 dB from 744 MHz to 880 MHz. With a sufficient input matching of $S_{11} < -10$ dB, the proposed LNA operates from 750 MHz to 850 MHz, encompassing E-UTRA bands 5, 13, 18, 19, 26, and partially 20, where NB-IoT user equipment functions.

TABLE II
COMPARISON WITH STATE-OF-THE-ART DESIGNS

	[4]	[6]	[1]	[2]	[3]	3GPP requirement	This work
Target standard	Generic FSK	WBAN(PSK)	NB-IoT				
Architecture	Sub-sampling		Low-IF			-	Sub-sampling
Process	180nm	65nm	180nm	28nm	55nm	-	65nm
Supply	1.8V	0.6V	1.7V	0.9V	0.9/1.1V	-	1/1.9V
Frequency band	2.4GHz	2.4GHz	750~960MHz	750~960MHz	450~2200MHz	-	750~850MHz
Bandwidth	1~6MHz	1MHz	180kHz	180kHz	180kHz	180kHz	180kHz
NF(LNA)	NR	4dB	<2.7dB	NR	NR	-	5.6dB
NF(Sys)	8.6dB	6dB	4dB	8dB[c]	3.5-4.5dB	10.8dB[d]	8.3dB
IIP3	-38.7dBm[a]	NR	NR[b]	NR	NR	-21.1dBm[e]	-18dBm
Power	10.69mW[f]	1.05mW[f]	25mW	2.1mW	11.8mW	-	0.69mW

[a] Δf = 0.5MHz. [b] -6.2dBm at the lowest gain setting. [c] Due to 1/f noise.
[d] SNRmin = 2dB based on 3GPP TR 36.802. [e] Assuming ideal digital filter with 180kHz bandwidth.
[f] Including baseband demodulator.

The IIP3 results depicted in Fig. 22 are obtained by transmitting two tones at 2.2 MHz and 4.4 MHz offsets. Due to the LNA's narrow bandwidth, the 2-tone jammer undergoes significant filtering; IIP3 is calculated by input-referring the IM3 and comparing it to the input power of jammers. The proposed linearization technique enhances IIP3 by 7 dB compared to disabling the multi-gate transistor linearity improvement method, fulfilling NB-IoT requirements. The off-chip inductors' quality factor was not accurately predicted, causing VCM not to be set at the optimal biasing point considering bandwidth constraints, resulting in a 3 dB IIP3 degradation compared to simulation results shown in Fig. 13.

The receiver's NF is measured by transmitting a tone with a center frequency $f_c = 744$ MHz, a sampling frequency $f_s = 40.767$ MHz, and calculating the SNR at the ADC output, as shown in Fig. 23(a). The signal power is determined using the sinusoidal minimum error method, extracting the magnitude and phase information of a sinusoid with a known frequency from a discrete-time data sequence. After removing the signal at $f_s/4$, the noise is integrated over a 200 kHz bandwidth, yielding a total front-end noise figure of 8.3 dB, encompassing the LNA, track-and-hold amplifier, and ADC. Fig. 23(b) shows the ADC output spectrum with a 200 kbps QPSK modulated input with $P_{\text{in}} = -107$ dBm, demonstrating approximately 6 dB SNR. With a minimum required SNR of 2 dB for NB-IoT downlink reference measurement channels, the system achieves a sensitivity of -110.7 dBm.

Fig. 24 shows the measured NF degradation of the receiver in the presence of a continuous wave blocker with 15, 60 and 85 MHz frequency offset. With the specified power levels in Table I, the receiver was able to deliver sensitivity required by NB-IoT.

Table II compares the design with prior work, exhibiting over 17.1x lower power consumption than state-of-the-art NB-IoT RXs and 3x lower power than an NB-IoT wake-up receiver. Additionally, it demonstrates the lowest power and best linearity among other low-sampling-frequency sub-sampling RXs, validating the sub-sampling approach's viability for practical applications.

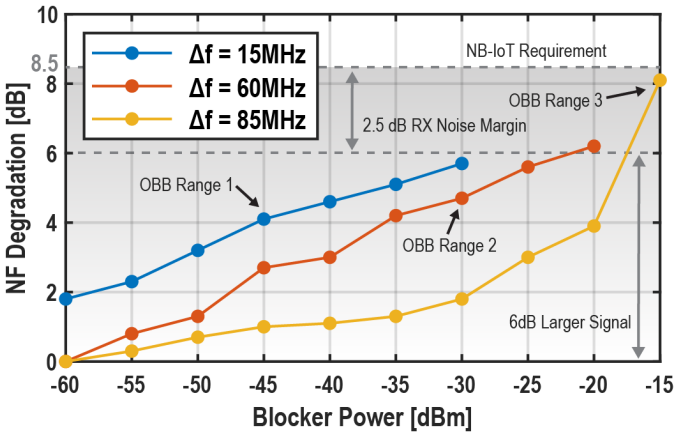


Fig. 24. Measured system NF degradation with continuous-wave blocker located at 15, 60 and 85 MHz offset frequencies.

VI. CONCLUSIONS

This paper presents a sub-sampling receiver that achieves sub-mW power consumption while satisfying NB-IoT NF and linearity requirements. The proposed Q-boosted LNA improves NF by eliminating the need for an off-chip balun and enhances linearity using an auxiliary transistor that cancels the 3rd-order coefficient of the main XCP. Future work could focus on reducing the dependency between IIP3 and Q_{ind} or separating the bias of the auxiliary transistor from the main XCP at the expense of NF. The overall receiver has an NF of 8.3 dB while consuming only 0.69 mW of power.

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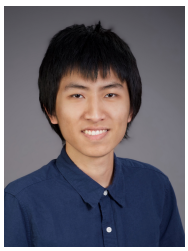

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