Staircase Matrix Modulation for the Switched-Capacitor Modular Multilevel Converter with Sensor-less Capacitor Voltage Balancing

Rami F. Yehia, *Member, IEEE*, Zhehui Guo, *Member, IEEE*, Hui Li, *Fellow, IEEE*, and Fang Z. Peng, *Fellow, IEEE*

Abstract Staircase modulation is a switching technique ubiquitous in multilevel inverters utilizing large number of output voltage levels. With tens of levels, the output of a multilevel inverter employing staircase modulation approaches a sinusoid without requiring switching harmonics filters. Out of various multilevel inverter topologies, the modular multilevel converter (MMC) became prominent due to its modularity, scalability, and efficiency. However, balancing the submodule (SM) capacitor voltages poses a significant challenge in MMC operation. In this work, a staircase matrix modulation (SMM) strategy, which achieves sensor-less capacitor voltage balancing, is proposed for the switched – capacitor MMC (SCMMC), an MMC topology with a very small arm inductor. The proposed SMM utilizes a full rank, symmetric switching matrix, where specific switching patterns are assigned for each voltage level. The structure of the proposed matrix, its unique features, and the process of populating its entries for any converter voltage level are described. Theoretical analysis on the operation of the proposed SMM, simulations for an 11-level SCMMC, and experimental results on a single-phase, 2kW, 425V, 4-level SCMMC prototype are presented to illustrate the voltage balancing capability of the proposed SMM. The resulting switching frequency of the SCMMC under SMM is also analyzed.

Index Terms— capacitor voltage balancing, low-frequency modulation, staircase PWM, switched-capacitor modular multilevel converter

I. INTRODUCTION

MODULAR multilevel converters (MMC) have garnered significant interest in recent years in medium voltage (MV), high power applications[1]. MMCs are prevalent nowadays in high voltage direct current (HVDC) transmission systems, grid integration of renewable energy sources, traction drives, and power quality enhancement applications [1], [2], [3], [4]

One key factor influencing the MMC performance is the selection of its modulation strategy. Fig. 1 presents a summary of various MMC modulation strategies, and classifies them into the high frequency and low frequency modulation techniques. This categorization is based on the nature of the output voltage waveform as shown in Fig. 1 and

This paper is an extension of the following conference paper: R. F. Yehia and F. Z. Peng, "Staircase Matrix Modulation for the Switched-Capacitor Modular Multilevel Converter with Sensor-less Voltage Balancing," in 2023 IEEE APEC, Mar. 2023, pp. 2839–2844

Rami F. Yehia is with the Vehicle Electrification Systems group at Aptiv PLC, Troy, MI, 48083 USA (rami.f.yehia@gmail.com).

Zhehui Guo is with Milan M. Jovanović Power Electronics Laboratory, Delta Electronics (Americas) Ltd., Research Triangle Park, NC, USA 27709 (zg18b@fsu.edu),

Hui Li, and Fang Z. Peng are with the Center for Advanced Power Systems, Florida State University, Tallahassee, FL 32306 USA (e-mail: hli@caps.fsu.edu; fpeng@eng.famu.fsu.edu).
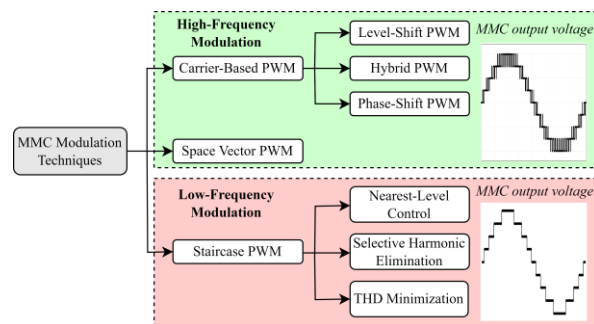
Fig. 1. Conventional MMC Modulation Techniques

not the actual switching frequency of the SMs.

High frequency modulation techniques include the carrier-based and the space-vector pulse-width-modulation (PWM) techniques. These techniques are typically used with passive LC filters to obtain sinusoidal output voltage and current waveforms from high-frequency PWM waveforms. On the other hand, low-frequency modulation techniques generate a multilevel output voltage waveform by approximating it with a series of discrete voltage levels, resembling a staircase. These techniques often result in lower switching frequencies, which becomes beneficial in high-power applications where efficiency is critical [5], [6], [7], [8].

Regardless of the adopted modulation technique, one

Table I. Comparison of MMC Voltage Balancing Solutions

	Implementation Complexity	Sensor-less Balancing	High-Level Reachability	Workability with Staircase Voltage	Applicability to SCMMC
Sorting Algorithm [1], [9], [10]	Hardware and Control Complexity	No	Tens of levels	Yes	Yes
Local Controller [11], [12], [13]	Control Complexity	No	Hundreds of levels	No	Yes
Pattern Swapping [14], [15], [16], [17]	Extensive Computation	Yes	Few Tens of levels	No	No
Topology Modification [18], [19], [20], [21]	Hardware Complexity	Yes	Hundreds of levels	Yes	No
Y-Matrix Modulation [22], [23]	Moderate Computation	Yes	Hundreds of levels	No	Yes
Proposed SMM	**Simple Computation**	**Yes**	**Hundreds of levels**	**Yes**	**Yes**

design challenge faced in MMCs is maintaining the voltage balance across its SM capacitors. Various control strategies have been proposed in the literature to address the MMC capacitor voltage balancing problem. A summary of these strategies is given in Table I, and include:

1) Sorting algorithm [1], [9], [10]: these methods involves sensing and sorting SM voltages, then selecting accordingly which SMs to be inserted, taking into consideration the arm current direction. This method is robust, but it is expensive and complicated to implement (bulky voltage and current sensors, signal conditioning boards, computational complexity).

2) Local controllers [11], [12], [13]: these methods use local controllers such as PI control or model predictive control to balance each SM capacitor voltage individually. These methods are good for converters with large number of voltage levels, and can preserve uniform switching frequency among all MMC submodules. However, they may cause higher harmonic distortion and require sensing the SM voltages.

3) SM pattern swapping [14], [15], [16], [17]: these methods involve rotating between SM switching sequences for a given voltage level. They can achieve sensor-less balancing, but they are not extendable to MMC with large number of levels or require complex switching pattern generation.

4) Topology modification [18], [19], [20], [21]: these methods involve modifying the submodule circuitry to add an inherent balancing feature. They are reliable techniques. However, they require additional components, and increase the system's implementation cost.

To solve the aforementioned challenges, a Y-matrix modulation (YMM) scheme based on a full-rank switching matrix has been proposed for the switched-capacitor MMCs (SCMMC) [22], [23]. YMM is a high-frequency modulation method that leverages the SCMMC self-voltage balancing capability to balance the SM voltages without requiring complicated algorithms, additional circuitry, or feedback control. It is also applicable to SCMMCs with large number of voltage levels. To achieve capacitor self-voltage balancing, YMM requires the arm inductor voltage drop to be negligible; hence, it works best for the SCMMC [24]. The SCMMC self-voltage balancing capability has been validated under steady-state, transient, and startup conditions with YMM [25]. YMM is implemented with two stages; first, the phase voltage level is determined from the voltage reference. Next, the PWM signals are generated by rotating among certain switching states for each voltage level. These switching states are grouped in a matrix, and it was shown that using a full rank Y-matrix is necessary to achieve voltage balancing for an MMC exhibiting a switched capacitor behavior [22], [26].

In this paper, we show that even with a full rank matrix, YMM cannot achieve voltage balancing with the SCMMC if a staircase output voltage is required [26], [27]. A new staircase matrix modulation (SMM) is proposed for SCMMC, which achieves sensor-less capacitor voltage balancing with a staircase output voltage. The proposed SMM is derived from YMM, but it uses a different switching matrix, hereby called the C-matrix **C**. Besides the full rank characteristic discussed in [23], the C-matrix proposed herein for SMM possesses a unique symmetry feature in the distribution of ones and zeros, which represent the SMs' inserted and bypassed states. It will be shown that the full rank and the symmetry features of the switching matrix **C** are both required to achieve self-voltage balancing for a SMM-modulated SCMMC.

The rest of the paper is organized as follows. In section II, we review the SCMMC topology and YMM [23], and then we highlight the voltage unbalancing issues caused by applying YMM at low PWM frequencies. Next, in section III, the proposed SMM is introduced and its voltage balancing mechanism is explained. The structure and features of the new switching matrix **C** and the process of generating it for any converter voltage level are then described. Also, a theoretical proof on the symmetry requirement is presented. Afterwards, we analyze the choice of the frequency at which redundant switching patterns are rotated in SMM, and describe the effect on the converter switching frequency and on the voltage balancing performance. To validate the proposed modulation strategy, open and closed-loop simulation results for an 11-level SCMMC under SMM are provided in section IV, and experimental results on a single-phase, 2kW, 425Vrms, 4-level, SCMMC prototype are presented in section V, both under steady-state and transient conditions. A highlight of the features and characteristics of the SCMMC under the proposed SMM are presented in section VI. Finally, section VII concludes the paper.

II. THE SWITCHED – CAPACITOR MMC AND Y-MATRIX MODULATION (YMM)

A. The SCMMC Topology

Fig. 2 shows a 3-phase, $(N + 1)$-level SCMMC with N half-bridge SMs per arm. Compared to the traditional MMC, the SCMMC has an arm inductor two to three orders of
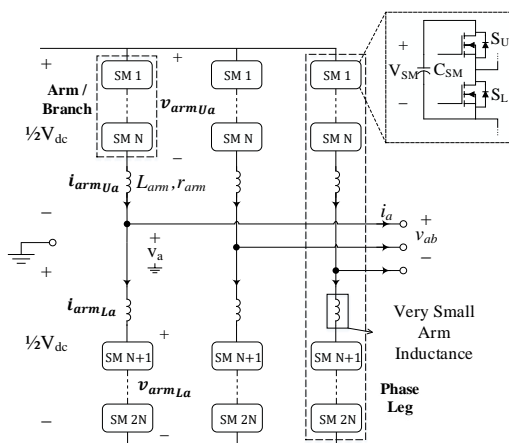
Fig. 2. 3-phase $(N+1)$-level SCMMC

magnitude smaller, which promotes higher power density and self-voltage voltage balancing features [26]. To leverage this self-voltage balancing capability, a Y-matrix modulation (YMM) has been proposed in [23]. To maintain voltage balancing, YMM requires the arm inductor to be small enough such that the voltage drop across it can be ignored [24]. In this case, the MMC behaves as a switched-capacitor converter, rather than a series of cascaded voltage source converters.

B. Review of YMM

The YMM of a 4-level SCMMC is presented in Fig. 3. It is implemented in two stages; in the first stage, the SCMMC phase voltage level is determined from the voltage reference using carrier-based PWM methods. After the voltage level is determined, a certain switching pattern is chosen from the switching matrix (Y-Matrix) in the second stage. The Y-Matrix **Y** of an $(N+1)$-level MMC consists of $N+1$ submatrices Y_1, Y_2, ..., Y_{N+1}. Each submatrix corresponds to a specific voltage level and consists of $2N$ columns, where columns 1 to N correspond to the switching states of the upper N SMs and columns $N+1$ to $2N$ correspond to the switching states of the lower N SMs. A matrix row indicates the switching state, at a certain instant, of all SMs starting from SM 1 at the leftmost column to SM 2N at the rightmost column. The submatrices consist of ones and zeros representing the switching states of the MMC. An entry of 1 means the corresponding SM is inserted (SU on, SL off), whereas an entry of 0 indicates the SM is bypassed (SU off, SL on). The relation between the capacitor voltages V, the dc bus voltage V_{dc} and the Y-matrix **Y** is given in (1) and its matrix form is given in (2).

$$V_{dc} = \mathbf{Y} V_C \qquad (1)$$

$$\begin{bmatrix} V_{dc} \\ \vdots \\ V_{dc} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_1} \\ \vdots \\ \mathbf{Y_{N+1}} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_{2N} \end{bmatrix} \qquad (2)$$

$$\begin{bmatrix} V_1 \\ \vdots \\ V_{2N} \end{bmatrix} = \frac{1}{N} \begin{bmatrix} V_{dc} \\ \vdots \\ V_{dc} \end{bmatrix}. \qquad (3)$$

It was demonstrated in [22] that if **Y** has a full rank equal to 2N, then the capacitor voltages have a unique solution
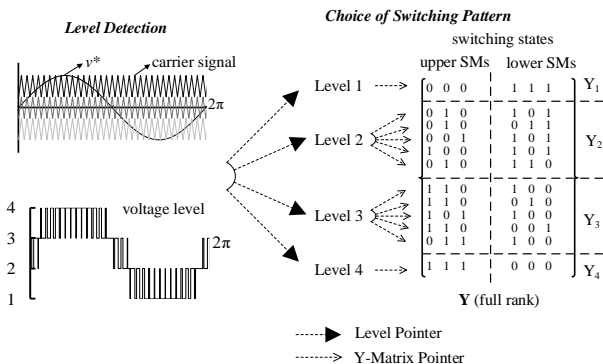

Fig. 3. YMM of a 4-Level SCMMC

given in (3) and they are balanced at their nominal value $\frac{V_{dc}}{N}$. It is important to reiterate that (1) and (2) are formulated assuming the voltage drop across the arm inductor is zero; hence, YMM can only achieve voltage balancing with the SCMMC topology.

C. Limitations of YMM Under Low-Frequency Operation

The ability of YMM to achieve sensor-less voltage balancing for the SCMMC is only possible for high-frequency operation. By high frequency, we mean the carrier signal frequency of Fig. 3, which reflects the PWM frequency of the output voltage and the frequency at which the voltage level updates (level pointer frequency). In other words, YMM cannot achieve voltage balancing with the SCMMC at low PWM frequency, even with a full rank matrix; hence, it cannot be used when a staircase output voltage is required. This limited operation can be explained by analyzing the switching pattern rotation scheme of YMM. Consider the 4-level YMM shown in Fig. 3: when the level pointer is at 3, five switching states are possible, which are the rows of submatrix Y_3. The choice of the switching pattern among the five possible ones for level 3 is determined by the Y-matrix pointer. The Y-matrix pointer is updated as illustrated in the following example:

1) Suppose the level pointer is at 3 and the Y-matrix pointer is at the first row of Y_3. In this case, the switching pattern [110100] is used.

2) When the level pointer becomes 4, the pattern [111000] is used as it is the only one available for level 4 (Y_4 has one row).

3) When the level pointer becomes 3 again, only now the Y-matrix pointer initially set at the first row of Y_3 is incremented and the pattern [110010] is used. This pattern is used and the Y-matrix pointer does not change unless level 3 is reached again.

This analysis of the YMM rotation scheme shows that the switching pattern (Y-matrix pointer) only changes when the voltage level (level pointer) is updated. Hence, under fundamental PWM frequency modulation where the output voltage is an $(N+1)$-level staircase waveform, each voltage level m (where $2 \leq m \leq N$) is reached twice in one fundamental cycle; consequently, the switching pattern for each voltage level only updates twice in one fundamental
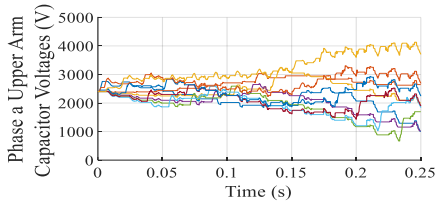
Fig. 4. SM capacitor voltages under YMM with staircase output voltage

cycle. Thus, the same loading condition is applied on each SM for half a cycle. With such a long time where the same pattern is applied on a specific SM, its corresponding capacitor voltage begins to diverge from its nominal value, and voltage balancing would take longer time to be achieved (more than 1 switching cycle). Even worse, voltage balancing will be completely lost if the next switching state applied is not complementary to the previous one; i.e., if the charge absorbed/released from the SM capacitor in one switching cycle is not released/absorbed in the following one. This case is illustrated in Fig. 4, which shows the capacitor voltage unbalance under YMM with a staircase output voltage.

III. STAIRCASE MATRIX MODULATION (SMM)

To address the constraints of using YMM at low PWM frequencies and achieve sensor-less SM voltage balancing with a staircase output voltage, the staircase matrix modulation (SMM) is proposed. SMM also relies on the SCMMC self-voltage balancing capability to achieve capacitor voltage balancing and it is derived from YMM. However, SMM uses a different switching matrix compared to YMM. Two switching pattern rotation schemes will be developed for SMM. The first being the high – frequency pattern rotation scheme (HFRS), initially introduced in [27] and described in detail in this section. A. In, HFRS, the switching patterns are rotated at a certain rotation frequency, independent of the voltage level. The other is the low – frequency pattern rotation scheme (LFRS), where the switching pattern is only changed when the voltage level changes, just like YMM. We will show the features of each of these two rotation schemes and adopt one of them for SMM. The SMM for a 4-level SCMMC is shown in Fig. 5 (a) with the HFRS, and in Fig. 5 (b) with the LFRS. In the first stage, nearest level control is used to obtain the voltage level from the reference voltage. Note that selected harmonic elimination (SHE) or any other method where the switching angles are calculated to minimize the total harmonic distortion can be used to get the reference staircase voltage level. Afterwards, the matrix pointer selects the gating pattern to be applied for the detected level from the unique switching matrix proposed in III.B. Unlike other pattern swapping methods [14], [15], SMM is used with the SCMMC only, and utilizes selected switching states that make up a full rank matrix, making it extendable to hundreds of levels.
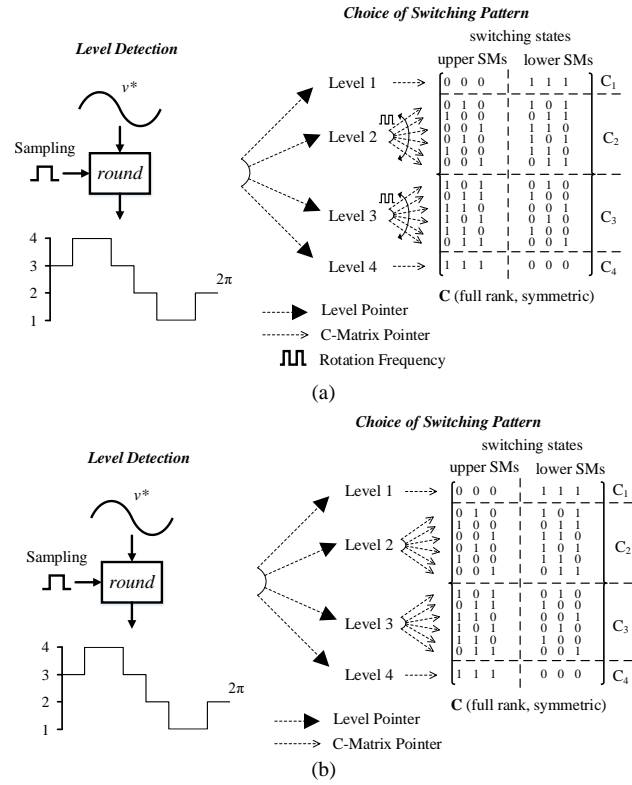
Fig. 5. SMM for 4-Level SCMMC with (a) high-frequency rotation scheme (HFRS) (b) low-frequency rotation scheme (LFRS)

A. SMM Rotation Scheme (HFRS)

i) SMM High – Frequency Rotation Scheme (HFRS)

We have shown in section II.C. that in YMM, the matrix pointer is only updated when the voltage level changes, which causes the SM voltages to deviate if the PWM frequency is low, and potentially leads to SM voltage unbalance for YMM. To limit the voltage deviation, we propose a modified, high – frequency rotation scheme (HFRS) for SMM where the matrix pointer is updated periodically at a specific rotation frequency f_{rot}, and instantly when the voltage level changes. This rotation scheme allows rotating among the switching patterns even when the voltage level has not changed. The choice of f_{rot} determines how long a certain switching pattern is applied; i.e., how long the capacitor voltages will deviate. The shorter the $1/f_{rot}$ cycle, the smaller the capacitor voltage deviation, and eventually, the smaller capacitor voltage ripple. Hence, the $1/f_{rot}$ cycle reflects the length of the voltage balancing cycle. To achieve switching cycle-by-cycle voltage balancing, f_{rot} must satisfy the condition given in (4):

$$\frac{1}{R_{arm}C_{SM}} < f_{rot} < \frac{R_{arm}}{2L_{arm}}, \qquad (4)$$

where R_{arm} represents the converter arm losses, C_{SM} is the SM capacitance, and L_{arm} is the arm inductance. The left-side condition $(f_{rot} > \frac{1}{R_{arm}C_{SM}})$ sets the lower limit on the rotation frequency. Below this frequency, the time the same switching state is applied to a certain SM becomes long

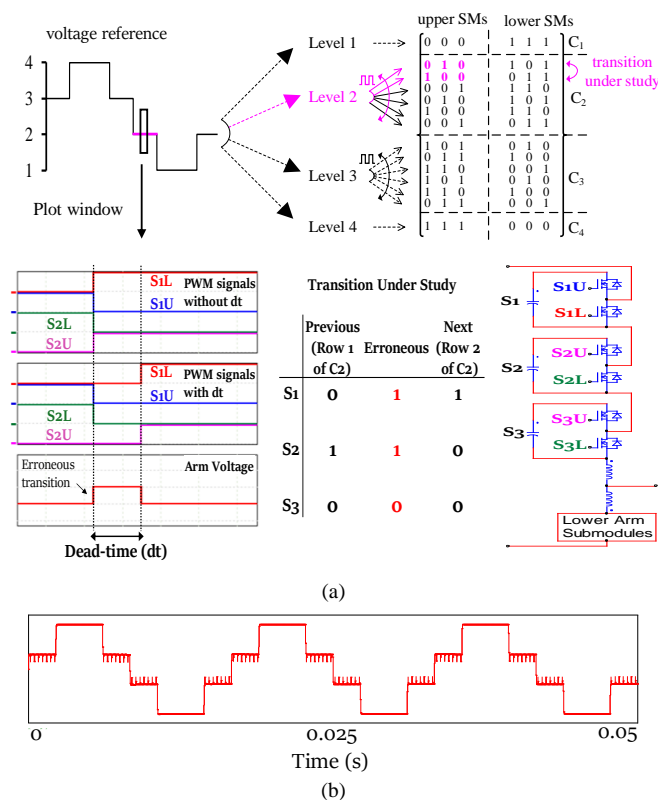Fig. 6. Dead-time effect with the high-frequency rotation scheme (HFRS) on a 4-level SCMMC (a) phenomenon (b) resulting distortions in ac voltage

enough to deviate its capacitor voltage from its present value during the switching cycle. The expression $R_{arm}C_{SM}$ represents the charging time constant of the SM capacitors, which should be shorter than the damping transient $\frac{2L_{arm}}{R_{arm}}$ of the RLC circuit formed by the SM capacitance, arm resistance, and arm inductance shown on the right side. The right-side condition $(f_{rot} < \frac{R_{arm}}{2L_{arm}})$ is the same condition applied to the YMM [24], and it sets the upper limit on the arm inductance, beyond which the negligible arm inductor voltage drop assumption of matrix modulation no longer holds and voltage balancing is lost.

Despite the shorter capacitor voltage deviation period offered by the HFRS, several downsides exist. Those downsides were not addressed when the HFRS was initially proposed with SMM in [27]. The first downside being the higher switching frequency of the resulting SMM due to the frequent switching pattern rotation. The higher switching frequency tarnishes the low-switching loss advantage of staircase modulation [28]. Another more serious issue resulting from the HFRS is that updating the switching pattern when the voltage level has not changed causes erroneous voltage transitions due to the dead-time effect. The phenomenon can be explained by Fig. 6. The voltage level is at 2 and the initial switching pattern for the upper SM is [010]. The matrix pointer changes and the next switching pattern [100] needs to be applied. To change the switching pattern, Submodule S1 which was inserted needs to be bypassed (its upper and lower switches need to flip their state),

and S2 which was bypassed needs to be inserted. However, since the upper and lower switches of S1 and S2 do not change their state at the same time due to the dead-time effect, the bypassing of S1 does not happen at the same time as the insertion of S2, which causes an erroneous voltage transition in the arm voltage. To elaborate, in the dead-time window, all the 4 switches of the two modules that change their state are off, and the insertion / bypassing of the modules depend on the direction of the arm current through the freewheeling diode. If the arm current is negative, both modules become bypassed, and the intermediate state [000] gets applied in the dead-time window, leading to an erroneous transition to a lower voltage level in the arm voltage. On the other hand, if the arm current is positive, both modules get inserted, and the intermediate state [110] gets applied, leading to an erroneous transition to a higher voltage level in the arm voltage. The effect on the ac voltage is shown in Fig. 6 (b) for the latter case, where S2 gets inserted before S1 gets bypassed.

ii)   SMM Low – Frequency Rotation Scheme (LFRS)

Since the dead-time effect deteriorates the staircase voltage waveform with the HFRS, this scheme, initially proposed to shorten the capacitor voltage deviation time is not favored practically. Instead, a rotation scheme where the switching pattern is updated only when the voltage level changes should be used. This rotation scheme is the same one used for YMM, and will be referred to as the low-frequency rotation scheme (LFRS). Nevertheless, with SMM, the LFRS is used with a unique switching matrix different from that used with YMM, which allows sensor-less voltage balancing with low-switching frequencies and a staircase output voltage.

B.   The SMM Symmetric Switching Matrix

i)   Matrix Features

The switching matrix comprises $N + 1$ submatrices, where each submatrix contains selected switching patterns for a certain voltage level. When forming the switching matrix **Y** for YMM in [23], only the rank of the matrix was assessed. It was shown that if **Y** has a full rank of $2N$, the capacitor voltages have unique solution, and they are balanced at V_{dc}/N.

Nevertheless, even with a full rank matrix, we showed in section II.C. that the capacitor voltages would not be balanced with YMM when a staircase output voltage is required. With the LFRS of YMM, the same loading condition is applied on each SM for a fraction of the fundamental cycle. With such a long time where the same pattern is applied on a certain SM, its corresponding capacitor voltage starts to diverge from its nominal value. To keep the capacitor voltages from diverging, it is necessary that the next switching state of a certain SM should be complimentary to the previous one and applied for an equal duration. This condition guarantees that the charge absorbed/released from the SM capacitor in one switching cycle is released/absorbed in another one, which will eventually balance the charging and discharging cycles of the SM capacitors and balance their voltage. Note that a
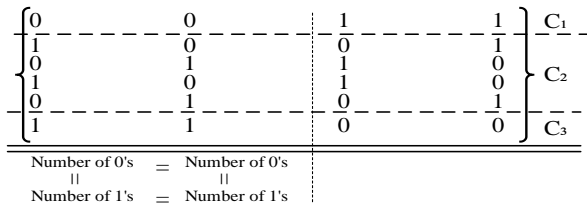
Fig. 7. Symmetry features of the switching matrix $\mathbf{C}$ of a 3-level MMC

Fig. 8. Structure of the intermediate switching matrix $\mathbf{C}'$ for (a) even level SCMMC (b) odd level SCMMC

complimentary state means that the corresponding $1's$ / $0's$ representing bypass and insertion states are flipped to $0's$ / $1's$. As a result, the switching matrix of SMM has to be symmetric in its distribution of $1's$ / $0's$.

Similarly, under SMM with the HFRS, even though the capacitor voltage deviation period is shortened due to the high frequency pattern rotation, the symmetric switching matrix is also required. Under SMM with the HFRS, the switching patterns are rotated periodically at a fixed rotation frequency f_{rot}. Hence, each pattern (each matrix row) is applied for an equal duration, $1/f_{rot}$. Since the patterns represent SM insertion and bypass states ($1's$ and $0's$), ensuring equal insertion and bypass times require the switching matrix used with SMM to be symmetric in the distribution of its $1's$ and $0's$.

Therefore, while the rotation scheme determines whether the voltage balancing cycle is short (high – frequency) or long (low – frequency), the symmetry feature of the switching matrix of SMM is inevitable for voltage balancing. Nevertheless, the most important feature that has to be preserved is the full rank feature, which is necessary to ensure the self-voltage balancing feature of the SCMMC [22]. Hence, we propose a new switching matrix $\mathbf{C}$ for SMM that keeps the full rank requirement of $\mathbf{Y}$, but possesses the following two symmetry features:

1) The number of $1's$ in each column of $\mathbf{C}$ is equal to the number of $0's$. This feature will be referred to as the insertion/bypass symmetry

2) The number of $1's$ and $0's$ in each column from columns 1 to N (i.e. for each upper arm SM) matches respectively the number of $1's$ and $0's$ of every other respective column (i.e. of every other upper arm SM). This conditions also applies for columns N+1 to 2N corresponding to the lower arm SMs. It holds true for the whole matrix $\mathbf{C}$ and for all submatrices. This feature will be referred to as the SM symmetry.

Fig. 7 illustrates the symmetry features of the C-matrix $\mathbf{C}$ for a 3-level SCMMC. The insertion/bypass symmetry feature of the switching matrix allows balancing the insertion and bypassing times of each SM, and the SM symmetry feature exposes all SM to the same loading conditions. These mechanisms work together to achieve capacitor voltage balancing with the proposed SMM. A switching matrix, which satisfies both symmetry features is necessary to achieve voltage balancing with the proposed SMM.

ii) Matrix Generation

A key contribution of the proposed SMM is the simplicity of generating its unique switching matrix $\mathbf{C}$. Fig. 8(a) shows the structure of $\mathbf{C}'$ (an intermediate matrix from which $\mathbf{C}$ is derived) for an even level (N is odd) SCMMC and Fig. 8(b) shows the structure of $\mathbf{C}'$ for an odd level (N is even) SCMMC. The number of columns is $2N$ corresponding to the number of SMs, and the number of submatrices is $N+1$, corresponding to the number of levels. The first and the last row of $\mathbf{C}$ and $\mathbf{C}'$ are the submatrices C_1 and C_{N+1} comprising the switching patterns for levels 1 and $N+1$ respectively. C_1 and C_{N+1} are same as Y_1 and Y_{N+1} of the Y-matrix [23]. To generate submatrices $C_2, \dots, C_N$, only the set of matrices A_k and B_k need to be generated. A_k and B_k are $2N \times N$ matrices constituting respectively the upper arm and lower arm switching patterns for level k, where $k = 1, \dots, \frac{N-1}{2}$ for even level MMC and $k = 1, \dots, \frac{N}{2}$ for odd level MMC. $\left[A_{N/2}\right]^C$ denotes the complementary of matrix of $A_{N/2}$; i.e., the ones/zeros of $A_{N/2}$ are flipped into zeros/ones in $\left[A_{N/2}\right]^C$. The sequence of generating A_k is described as follows:
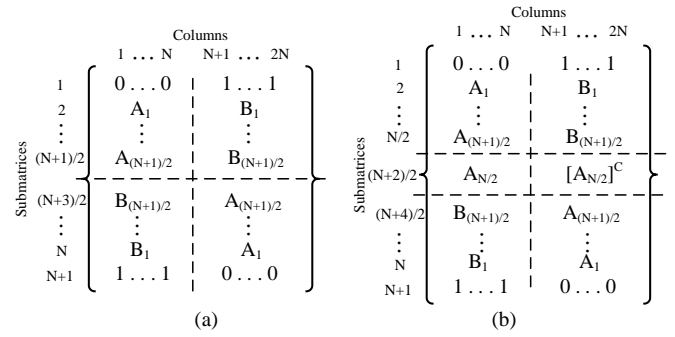
1) The first row of A_k is formed by filling the first k columns by $1's$, and the rest (columns $k+1$ to N) by $0's$.

2) The mth row of A_k ($m = 2, \dots, N$) is the $(m-1)^{th}$ row of A_k, with each row entry circularly shifted right by 1 position.

3) The set of rows from $N+1$ to $2N$ of A_k are the same as the first N rows of A_k.

The sequence of generating B_k is described as follows:

1) The first N rows of B_k are the same as the first N rows of A_k, but with ones/zeros of A_k flipped to zeros/ones in B_k

2) The set of rows from $N+1$ to $2N$ of B_k are the same as the first N rows of B_k, but in reverse order (i.e. row $N+1$ is row N, row $N+2$ is row $N-1$, …, and row $2N$ is row 1).

After generating A_k and B_k, an intermediate matrix $\mathbf{C}'$ is generated by grouping the matrices A_k and B_k as shown in Fig. 8. Finally, to achieve even switching among the SMs, the C-matrix $\mathbf{C}$ is generated from the intermediate matrix $\mathbf{C}'$ as follows.

1) Swap the first and second row of submatrix C_2

2) Swap the $(N+1)^{th}$ and the $(N+2)^{th}$ row of submatrix C_2

3) Circular shift downwards rows $N+1$ to $2N$ by $N-1$ positions of each of the submatrices $C_3, \dots, C_{N-1}$

4) Swap the first and second row of submatrix C_N

```
C₁   000 111        C₁   0000 1111        0111 1000
                                          1011 0100
     100 011             1000 0111        1101 0010
     010 101             0100 1011   C₄   1110 0001
C₂   001 110             0010 1101        1110 1000
     100 110        C₂   0001 1110        1101 0100
     010 101             1000 1110        1011 0010
     001 011             0100 1101        0111 0001
                         0010 1011
     011 100             0001 0111   C₅   1111 0000
     101 010
C₃   110 001             1100 0011
     110 100             0110 1001
     101 010             0011 1100
     011 001        C₃   1001 0110
                         1100 0110
C₄   111 000             0110 1100
                         0011 1001
                         1001 0011
        (a)                      (b)
```
Fig. 9. Intermediate matrix $\mathbf{C'}$ of the proposed SMM (a) 4-level (b) 5-level

```
C₁   000 111        C₁   0000 1111        1011 0100
                                          0111 1000
     010 101             0100 1011        1101 0010
     100 011             1000 0111   C₄   1110 0001
C₂   001 110             0010 1101        1101 0100
     010 101        C₂   0001 1110        1110 1000
     100 110             0100 1101        1011 0010
     001 011             1000 1110        0111 0001
                         0010 1011
     101 010             0001 0111   C₅   1111 0000
     011 100
C₃   110 001             1100 0011
     101 010             0110 1001
     110 100             0011 1100
     011 001        C₃   1001 0110
                         0110 1100
C₄   111 000             0011 1001
                         1001 0011
                         1100 0110
        (a)                      (b)
```
Fig. 10. C-matrix $\mathbf{C}$ of the proposed SMM (a) 4-level (b) 5-level

5) Swap the $(N + 1)^{th}$ and the $(N + 2)^{th}$ row of submatrix C_N

Besides possessing the symmetry feature, the proposed matrix $\mathbf{C}$ keeps the full – rank requirement and the size advantage of the Y-matrix. $\mathbf{C}$ has a full rank of 2N, and each submatrix is $2N \times 2N$, making it very compact and easy to implement. Moreover, the method described above for generating the resulting full rank symmetric matrix $\mathbf{C}$ by rotating the states is much more resource efficient than the method described for the full rank non-symmetric Y-matrix [23]. Generating $\mathbf{C}$ for a 433-level MMC takes only 28 seconds with a MATLAB script compared to 12 hours for the Y-matrix as reported in [29]. Note that the total number of switching patterns that can exist for just one voltage level k for an $(N + 1) -$ level MMC is $C_N^{k-1}C_N^{N+1-k}$[23], where C is the combination (binomial) operator; hence, using selected states only is crucial or else the matrix modulation techniques will not be practical to implement due to the enormous number of switching patterns. The compact, easy to generate, full rank, and symmetric matrix $\mathbf{C}$ is the main novelty of SMM. The intermediate matrix $\mathbf{C'}$ from which $\mathbf{C}$ is derived and the C-matrix $\mathbf{C}$ of the 4-level and 5-level SCMMC are given in Fig. 9 and 10, respectively.

C. Theoretical Proof on Symmetry for SMM

This section provides the mathematical proof that the number of ones in each submatrix column must match the number of zeros in every other column for upper arm submodules to achieve voltage balancing. This proof can be

$$\Delta Q = i_C \times \Delta t = C_{SM}\Delta V_{SM}S \tag{5}$$

$$\begin{cases} Q = C_{SM}V_{SM} & \text{for } S = 0 \\ Q = C_{SM}V_{SM} + \ C_{SM}\Delta V_{SM} & \text{for } S = 1 \end{cases} \tag{6}$$

$$Q = C_{SM}V_{SM} + C_{SM}\Delta V_{SM}S \tag{7}$$

$$
\mathbf{C} = \begin{bmatrix} \mathbf{C_1} \\ \mathbf{C_2} \\ \mathbf{C_3} \\ \mathbf{C_4} \end{bmatrix} =
\begin{bmatrix}
000 & 111 \\
010 & 101 \\
100 & 011 \\
001 & 110 \\
010 & 101 \\
100 & 110 \\
001 & 011 \\
101 & 010 \\
011 & 100 \\
110 & 001 \\
101 & 010 \\
110 & 100 \\
011 & 001 \\
111 & 000
\end{bmatrix}
=
\begin{bmatrix}
S_{11_1} & S_{21_1} & S_{31_1} & S_{41_1} & S_{51_1} & S_{51_1} \\
S_{11_2} & S_{21_2} & S_{31_2} & S_{41_2} & S_{51_2} & S_{61_2} \\
S_{12_2} & S_{22_2} & S_{32_2} & S_{42_2} & S_{52_2} & S_{62_2} \\
S_{13_2} & S_{23_2} & S_{33_2} & S_{43_2} & S_{53_2} & S_{63_2} \\
S_{14_2} & S_{24_2} & S_{34_2} & S_{44_2} & S_{54_2} & S_{64_2} \\
S_{15_2} & S_{25_2} & S_{35_2} & S_{45_2} & S_{55_2} & S_{65_2} \\
S_{16_2} & S_{26_2} & S_{36_2} & S_{46_2} & S_{56_2} & S_{66_2} \\
S_{11_3} & S_{21_3} & S_{31_3} & S_{41_3} & S_{51_3} & S_{61_3} \\
S_{12_3} & S_{22_3} & S_{32_3} & S_{42_3} & S_{52_3} & S_{62_3} \\
S_{13_3} & S_{23_3} & S_{33_3} & S_{43_3} & S_{53_3} & S_{63_3} \\
S_{14_3} & S_{24_3} & S_{34_3} & S_{44_3} & S_{54_3} & S_{64_3} \\
S_{15_3} & S_{25_3} & S_{35_3} & S_{45_3} & S_{55_3} & S_{65_3} \\
S_{16_3} & S_{26_3} & S_{36_3} & S_{46_3} & S_{56_3} & S_{66_3} \\
S_{11_4} & S_{12_4} & S_{13_4} & S_{14_4} & S_{15_4} & S_{16_4}
\end{bmatrix}
\tag{8}
$$

$$
\Delta[v_1\ v_2\ v_3\ v_4\ v_5\ v_6] = \Delta
\begin{bmatrix}
V_{11_1} & V_{21_1} & V_{31_1} & V_{41_1} & V_{51_1} & V_{61_1} \\
V_{11_2} & V_{21_2} & V_{31_2} & V_{41_2} & V_{51_2} & V_{61_2} \\
V_{12_2} & V_{22_2} & V_{32_2} & V_{42_2} & V_{52_2} & V_{62_2} \\
V_{13_2} & V_{23_2} & V_{33_2} & V_{43_2} & V_{53_2} & V_{63_2} \\
V_{14_2} & V_{24_2} & V_{34_2} & V_{44_2} & V_{54_2} & V_{64_2} \\
V_{15_2} & V_{25_2} & V_{35_2} & V_{45_2} & V_{55_2} & V_{65_2} \\
V_{16_2} & V_{26_2} & V_{36_2} & V_{46_2} & V_{56_2} & V_{66_2} \\
V_{11_3} & V_{21_3} & V_{31_3} & V_{41_3} & V_{51_3} & V_{61_3} \\
V_{12_3} & V_{22_3} & V_{32_3} & V_{42_3} & V_{52_3} & V_{62_3} \\
V_{13_3} & V_{23_3} & V_{33_3} & V_{43_3} & V_{53_3} & V_{63_3} \\
V_{14_3} & V_{24_3} & V_{34_3} & V_{44_3} & V_{54_3} & V_{64_3} \\
V_{15_3} & V_{25_3} & V_{35_3} & V_{45_3} & V_{55_3} & V_{65_3} \\
V_{16_3} & V_{26_3} & V_{36_3} & V_{46_3} & V_{56_3} & V_{66_3} \\
V_{11_4} & V_{21_4} & V_{31_4} & V_{41_4} & V_{51_4} & V_{61_4}
\end{bmatrix}
\tag{9}
$$

extended to lower arm submodules as well, and to other submatrices.

Consider the half bridge SM shown in Fig. 2; for a state $S = 0$ in a submatrix, the corresponding submodule is bypassed (SU open, SL closed), and the submodule capacitor does not gain or dissipate any charge (except the charge in the bleeding resistor across the submodule capacitor (not shown) which is negligible). For a state $S = 1$ in a submatrix, the corresponding submodule is inserted (SU closed, SL open), and the submodule capacitor gains or dissipates charge depending on the arm current direction. The charge gain/loss ΔQ during a switching state S is given by (5), where i_C is the capacitor current, Δt is the switching period, and ΔV_{SM} is the change in the capacitor voltage. From (5), the total charge on a given submodule capacitor during a switching state S can be given as shown in (6), and (6) can be rewritten in terms S as shown in (7).

$$\Delta Q_{pq_m} = C_{SM_p} \Delta V_{pq_m} S_{pq_m} \qquad (10)$$

$$\Delta Q_{p_m} = \frac{1}{2N} C_{SM_p} \sum_{q=1}^{2N} \Delta V_{pq_m} S_{pq_m} \qquad (11)$$

$$\Delta V_{p_m} = \frac{\Delta Q_{p_m}}{C_{SM_p}} = \frac{1}{2N} \sum_{q=1}^{2N} \Delta V_{pq_m} S_{pq_m} \qquad (12)$$

$$\Delta Q_{1_2} = \frac{1}{6} C_{SM_1} \sum_{q=1}^{6} \Delta V_{1q_2} S_{1q_2}$$
$$\Delta Q_{2_2} = \frac{1}{6} C_{SM_2} \sum_{q=1}^{6} \Delta V_{2q_2} S_{2q_2} \qquad (13)$$
$$\Delta Q_{3_2} = \frac{1}{6} C_{SM_3} \sum_{q=1}^{6} \Delta V_{3q_2} S_{3q_2}$$

$$\Delta V_{1_2} = \frac{\Delta Q_{1_2}}{C_{SM_1}}$$
$$\Delta V_{2_2} = \frac{\Delta Q_{2_2}}{C_{SM_2}} \qquad (14)$$
$$\Delta V_{3_2} = \frac{\Delta Q_{3_2}}{C_{SM_3}}$$

Similar to (7), the charge equation for all submodule capacitors can be expressed in terms of the instantaneous submodule voltage changes and the switching states of the C-matrix $\mathbf{C}$. Let us take the C-matrix of a 4-level SCMMC as an example to develop the equations; the analysis applies to any SCMMC voltage level. The C-matrix $\mathbf{C}$ of the 4-level SCMMC is given in (8), where S_{pq_m} corresponds to the switching state of the pth submodule at the qth row of the submatrix $\mathbf{C_m}$ corresponding to level m. Also, the instantaneous change in the capacitor voltages $\Delta[v_1 \ v_2 \ v_3 \ v_4 \ v_5 \ v_6]$ are given in (9) during each switching state, where ΔV_{pq_m} corresponds to the change in the capacitor voltage of the pth submodule when the switching state S_{pq_m} is applied. From the definitions in (6) and (7), the charge gain/loss ΔQ_{pq_m} on any given submodule capacitor p during a switching state S_{pq_m} can be expressed in terms of its capacitance C_{SM_p}, instantaneous voltage change ΔV_{pq_m}, and switching sate S_{pq_m} as given in (10).

From (10), the average charge gain/loss ΔQ_{p_m} on the pth capacitor during level m can be derived as shown in (11), and the average SM capacitor voltage change ΔV_{p_m} for the pth capacitor during level m becomes as shown in (12). Note that (10)-(12) apply to any SCMMC voltage level.

Now, let us consider a specific example for a 4-level SCMMC ($N = 3$), when the voltage reference is at level 2. From the general expressions given in (11) and (12), the average charge gain/loss on the three upper arm SM capacitors during level 2 are given in (13), and the average deviation in SM capacitor voltages for the upper arm submodules during level 2 are given in terms of the average charge gain/loss as shown in (14).

$$\sum_{q=1}^{6} \Delta V_{1q_2} S_{1q_2} = \sum_{q=1}^{6} \Delta V_{2q_2} S_{2q_2} = \sum_{q=1}^{6} \Delta V_{3q_2} S_{3q_2} \qquad (15)$$

$$\Delta V_{1_2} = \frac{\sum_{q=1}^{6} \Delta V_{1q_2}}{6} = \frac{\sum_{q=1}^{6} \Delta V_{1q_2} S_{1q_2}}{\sum_{q=1}^{6} S_{1q_2}}$$

$$\Delta V_{2_2} = \frac{\sum_{q=1}^{6} \Delta V_{2q_2}}{6} = \frac{\sum_{q=1}^{6} \Delta V_{2q_2} S_{2q_2}}{\sum_{q=1}^{6} S_{2q_2}} \qquad (16)$$

$$\Delta V_{3_2} = \frac{\sum_{q=1}^{6} \Delta V_{3q_2}}{6} = \frac{\sum_{q=1}^{6} \Delta V_{3q_2} S_{3q_2}}{\sum_{q=1}^{6} S_{3q_2}}$$

$$\frac{\sum_{q=1}^{6} \Delta V_{1q_2} S_{1q_2}}{\sum_{q=1}^{6} S_{1q_2}} = \frac{\sum_{q=1}^{6} \Delta V_{2q_2} S_{2q_2}}{\sum_{q=1}^{6} S_{2q_2}} = \frac{\sum_{q=1}^{6} \Delta V_{3q_2} S_{3q_2}}{\sum_{q=1}^{6} S_{3q_2}} \qquad (17)$$

$$\sum_{q=1}^{6} S_{1q_2} = \sum_{q=1}^{6} S_{2q_2} = \sum_{q=1}^{6} S_{3q_2} \qquad (18)$$

For balanced SM voltages, the average change in capacitor voltages is equal across the submodules $\Delta V_{1_2} = \Delta V_{2_2} = \Delta V_{3_2}$; hence, the relationship in (15) can be developed. However, the average change in SM capacitor voltages for the upper arm submodules during level 2 can also be expressed from the submatrix $\mathbf{C_2}$ as given in (16). For balanced SM voltages, $\Delta V_{1_2} = \Delta V_{2_2} = \Delta V_{3_2}$; hence, the relationship in (17) can be developed.

From (15) and (17), equation (18) becomes true. Equation (18) indicates that the summation of $1's$ and $0's$ in a certain submatrix column corresponding to an upper arm switch is equal to the summation of $1's$ and $0's$ in every other respective column. The same analysis applies for the lower arm switches (columns N+1 to 2N in each submatrix), and for other submatrices (all other levels).

Since (18) is true if and only if the SM voltages are balanced, therefore, for voltage balancing to be achieved with the proposed SMM, equal distribution between $1's$ and $0's$ in each column and across all C-matrix columns is required.

D. Switching Frequency Comparison: Low – Frequency vs High – Frequency Rotation Scheme

Two pattern rotation schemes have been introduced earlier for SMM. The first being the HFRS, which achieves low capacitor voltage ripple, but suffers from higher switching frequency and is prone to dead-time noise. The second is the LFRS, which is implemented with low switching frequency and is immune to dead-time noise, but has a slightly higher capacitor voltage ripple. The LFRS is the one to be used with SMM as it achieves the demanded staircase voltage. In this subsection, we compare the resulting switching frequency under the two rotation schemes. To quantify the switching frequency, let us examine the C-matrices shown in Fig. 10. One feature of the C-matrix that can be seen is that regardless of the voltage level, each of the submatrices $C_2 \dots C_N$ always has four switching state transitions per module; i.e., the
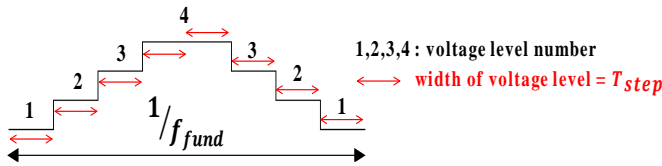
This article has been accepted for publication in IEEE Open Journal of Power Electronics. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2024.3417825

> REPLACE THIS LINE WITH YOUR PAPER IDENTIFICATION NUMBER (DOUBLE-CLICK HERE TO EDIT) <   9

Fig. 11. Staircase output phase voltage waveform of 4-level SCMMC

number of times the $1's$ are switched to $0's$ (and vice versa) per submatrix column (starting from a certain row and going back to it). This feature is very helpful in quantifying the switching frequency for SMM with both rotation schemes, which is presented next. The switching frequency is quantified theoretically for LFRS and HFRS for one SM, and can be multiplied by $2N$ to get the switching frequency of the whole converter.

i)   Switching Frequency for LFRS

For LFRS, the switching state only changes when the voltage level is changed. Consider the staircase multilevel voltage waveform shown in Fig. 11, the transition to each of the voltage levels 2 to N occurs twice every fundamental cycle ($1/f_{fund}$), and the transition to voltage levels 1 and N+1 occurs once. For submatrices C_2 to C_N, each 2N rows (2N voltage level transitions) feature 4 switching transitions. Therefore, for each of voltage levels 2 to N, there are $\frac{4f_{fund}}{N}$ switching transitions due to voltage level transition every second. As for levels 1 and N+1, the transition to both of these levels feature 1 switching state transition in a fundamental cycle. Hence, the switching frequency per module for SMM under LFRS can be derived as given in (19). Note that $f_{sw_{LFRS}}$ is the highest switching frequency possible in the LFRS. Any switching frequency above that given in (19) indicates the switching patterns are rotated within the same voltage level, which corresponds to the operation in the HFRS.

$$f_{sw_{LFRS}} = \frac{4f_{fund}}{N}(N-1) + f_{fund} \qquad (19)$$

ii)   Switching Frequency for HFRS

Similar to LFRS, the switching state under HFRS changes when the voltage level is changed. However, under HFRS, the switching states of the submatrix are also rotated at the rotation frequency f_{rot}. Hence, the total switching frequency is the number of switching state transitions due to voltage transitions (same as $f_{sw_{LFRS}}$ calculated in (19)) plus the number of switching transitions that occur due to pattern rotation. To quantify the latter, consider the C-matrices of Fig. 10. Each matrix row (each pattern) is applied for the rotation period $\frac{1}{f_{rot}}$. Since 4 transitions occur within a certain submatrix, and since each submatrix has 2N rows, then 4 transitions occur within $T_{rot} = \frac{2N}{f_{rot}}$ for each submatrix except C_1 and C_{N+1}, which have one switching pattern only. Assuming the staircase steps are almost equal in length as shown in Fig. 11, the period of time spent on each voltage level in one fundamental period is twice the width of each step, and is given in (20).

Table II. 11-level SCMMC Simulation Model Parameters

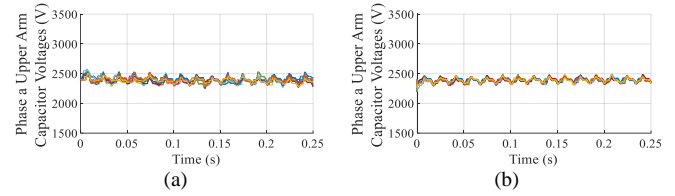| Parameters	Value	Parameters	Value
Rated Power	1 MVA	AC-side (open-loop)	RL load (190Ω, 10mH)
ac Voltage	13.8 kV	AC-side (closed-loop)	AC grid (f$_{fund}$ = 60 Hz)
dc Voltage	24 kV	SM Capacitance	120µF ± 20% (8.6 p.u.)
Arm Resistance	1.5 Ω	Arm Inductance	100 µH (0.015 %)

Fig. 12. Phase a upper arm capacitor voltages with SMM (a) LFRS (b) HFRS $f_{rot} = 6kHz$

Table III. Open-Loop Simulation Events Description

Time Stamp	Annotation on plot	Event
0.083 s	1o	Change MI from 0.94 to 0.7
0.15s	2o	Connect 3-phase unbalanced load

Table IV. Closed-Loop Simulation Events Description

Time Stamp	Annotation on plot	Event
0.05s	1c	Trigger external disturbance on SM capacitors
0.1s	2c	Change reference power set points (P*: 900kW → -800kW; Q*: 435kVAR → -600kVAR
0.15s	3c	Simulate unbalanced grid voltages

$$T_{voltage\_level} = 2T_{step} = \frac{1}{N+1} \times \frac{1}{f_{fund}} \qquad (20)$$

Hence, the period of time during which each submatrix is used can be approximated by $T_{voltage\_level}$. Hence, the number of transitions occurring for each matrix in a fundamental period due to pattern rotation can be derived as shown in (21)

$$Transitions_{t_{fund}} = 4 \times T_{voltage\_level} \times \frac{1}{T_{rot}} = \frac{2}{N(N+1)} \frac{f_{rot}}{f_{fund}} \qquad (21)$$

Since the switching pattern is changed for $N-1$ matrices only (matrices C_1 and C_{N+1} have only one switching state and do not undergo any pattern rotation), then the switching frequency per module for SMM under HFRS can be derived as given in (22).

$$f_{sw_{HFRS}} = \frac{2(N-1)}{N(N+1)} f_{rot} + \frac{4f_{fund}}{N}(N-1) + f_{fund} \qquad (22)$$

IV. SIMULATION RESULTS

To validate the operation of SMM, a simulation model of a 3-phase, 11-level SCMMC was developed and tested in both open-loop and closed-loop conditions. The model parameters are shown in Table II. The SM capacitors are subjected to 20% tolerance. To study the effect of the pattern rotation schemes on voltage balancing, Fig. 12 shows the SM capacitor voltages with the LFRS and with the HFRS. Since the symmetric full rank matrix **C** is used, voltage balancing can be achieved with both rotation schemes. However, under LFRS, there is a slightly higher capacitor voltage ripple due
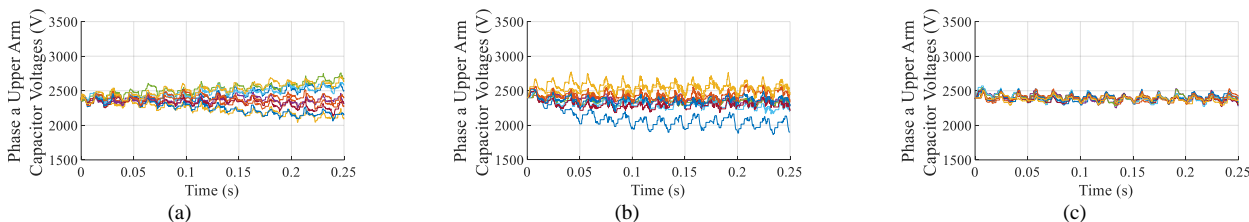
Fig. 13. Phase a upper arm capacitor voltages with (a) non-full rank symmetric matrix (b) full rank non symmetric Y-matrix **Y** (c) full rank symmetric C-matrix **C** (proposed)
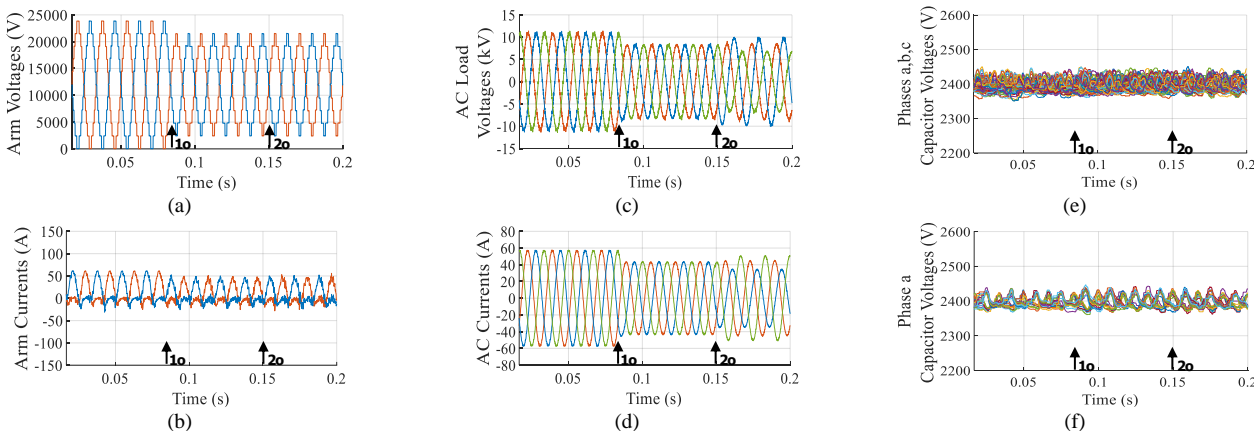

Fig. 14. Open loop simulation results of SMM with LFRS; the arrows annotate the simulated events presented in Table III (a) Phase a arm voltages (b) Phase a arm currents (c) AC load voltages (d) AC currents (e) All SM capacitor voltages (f) Phase a capacitor voltages
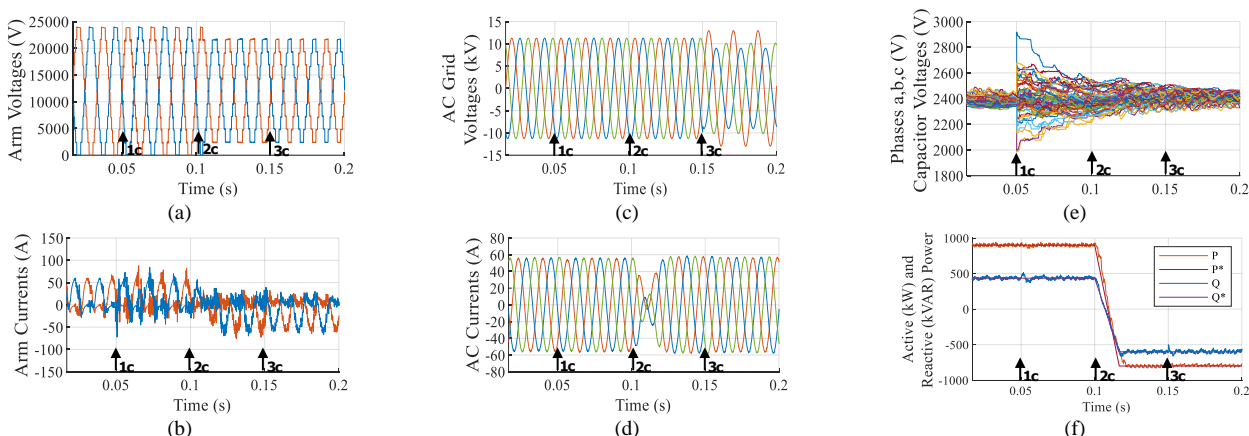

Fig. 15. Closed loop grid connected mode simulation results of SMM with LFRS; the arrows annotate the simulated events presented in Table IV (a) Phase a arm voltages (b) Phase a arm currents (c) AC grid voltages (d) AC currents (e) All SM capacitor voltages (f) Active and Reactive Powers

to the longer voltage balancing period. With HFRS, the ripples in the capacitor voltages are minimized if a minimum f_{rot} or higher, satisfying (4) (6kHz) is used.

Fig. 13 shows the SM voltages with the LFRS but with different switching matrices. Three switching matrices are considered; a non-full rank symmetric matrix in Fig.13(a), the full rank non-symmetric Y-matrix of [23] in Fig. 13(b), and the proposed full rank symmetric matrix **C** in Fig.13(c). The results show that voltage balancing can only be achieved if the proposed matrix **C** is used, since the symmetry and full rank features are both required. Therefore, the full rank symmetric matrix is crucial for voltage balancing with SMM.

Next, the robustness of SMM with the LFRS is tested in transient conditions with both open-loop and closed-loop conditions.

Table III shows the events simulated for the open-loop

case, and Fig. 14 shows the corresponding results. The SCMMC is connected to a 3-phase balanced load first, Then, the proposed SMM is tested under a modulation index (MI) change event where the MI is changed from 0.94 to 0.7. The results show that SMM maintains voltage balancing during transient conditions. Next, the RL load is replaced with a 3-phase unbalanced load at t=0.15s. The results show that all SM voltages of all phases remain balanced at their nominal value in unbalanced 3-phase system as well. The average SM switching frequency under LFRS is ~ 275 Hz, matching with (19), and the standard deviation of the SM switching frequencies is 10 Hz. Thus, SMM achieves even switching and loss distribution among SMs.

Table IV shows the events simulated for the closed-loop case, and Fig. 15 shows the corresponding results. The 11-level SCMMC is connected to the grid and a state-of-the-art

Table V. 4-level (3SMs/arm) SCMMC Prototype Parameters

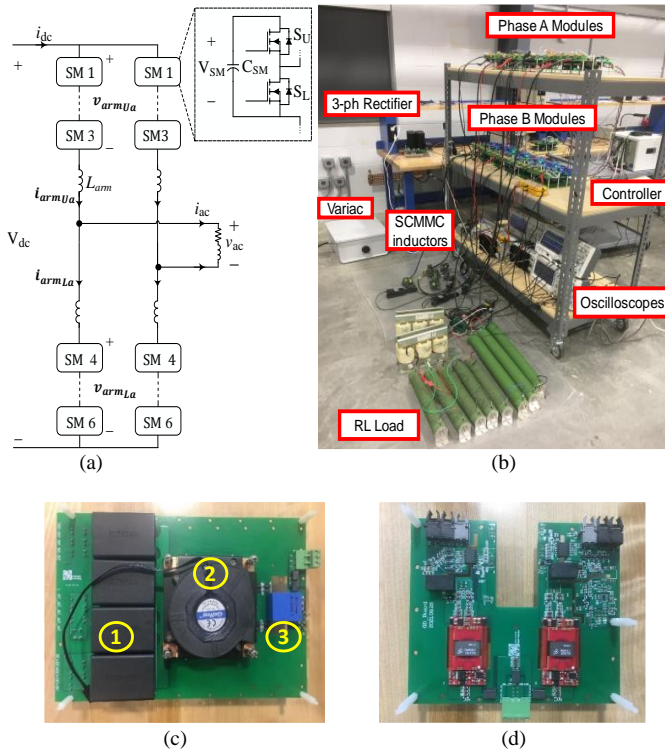| Parameters	Value	Parameters	Value
Rated Power	2 kW	Fundamental Frequency	60 Hz
ac Voltage	425 V	Load (R,L)	91 Ω, 1.4 mH
dc Voltage	600 V	SM Capacitance	120µF (4.7 p.u.)
SM Voltage	200 V	Arm Inductance	100 µH (0.042 %)

Fig. 16. 2- Phase leg, 4-level SCMMC prototype setup (a) circuit diagram (b) experimental setup (c) SM power board; 1: SM capacitors, 2: SiC module with cooling fan and heat sink, 3: voltage monitoring, d) gate-driver board

active-reactive power flow control (PQ-control) is used. The active and reactive power commands are set to 900kW, 435kVAR initially. Then, we simulated an external disturbance to the SM capacitors at t=0.05s (event 1c). We abruptly changed the SM capacitor voltages to random set points between $0.85V_{SM_{nominal}}$ to $1.2V_{SM_{nominal}}$. The results show that the SM capacitor voltages converge back to their nominal voltage value following the disturbance, which proves the robustness of the proposed SMM. The spikes witnessed in the arm currents at t=0.05s are inevitable due to the forced, sudden capacitor voltage disturbance. Next, the active and reactive power set points are changed to -800kW, -600kVAR, and the SM voltages remain balanced. Finally, we tested another unbalance condition, this time with the closed loop system, where we simulated unbalanced grid voltages. The SM capacitor voltages of all phases have been plotted, and the results show that the SM voltages are balanced.

V. EXPERIMENTAL VERIFICATION

To demonstrate the validity and the features of the proposed SMM, a 2kW, 425Vrms single phase (full-bridge)
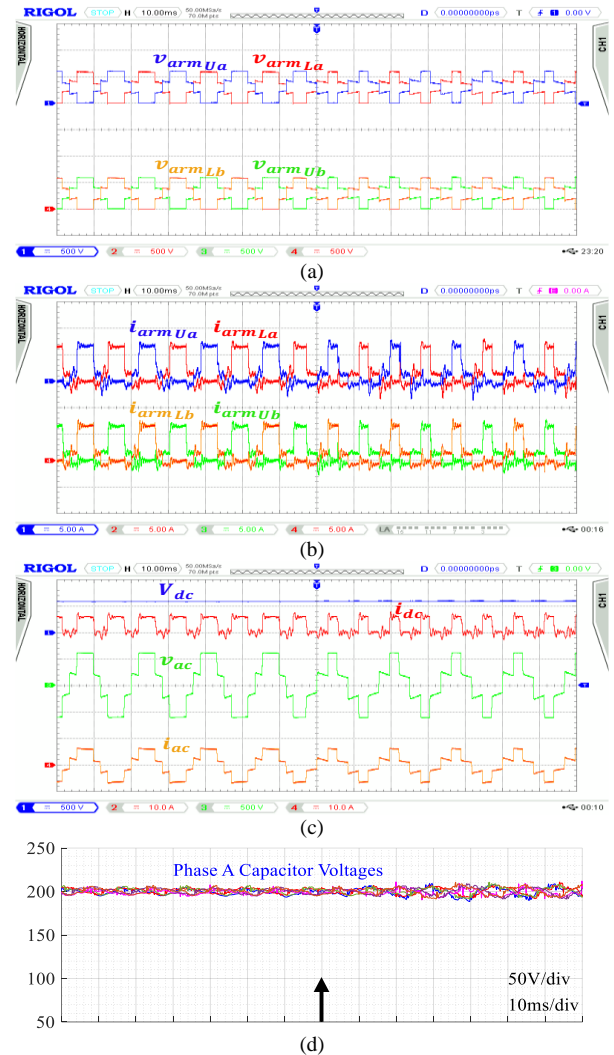
Fig. 17. 2-ph 4-level SCMMC experimental results under SMM with LFRS (arrow indicates modulation index change from 1 to 0.7) (a) Arm voltages (b) Arm currents (c) ac and dc voltage and currents (d) capacitor voltages
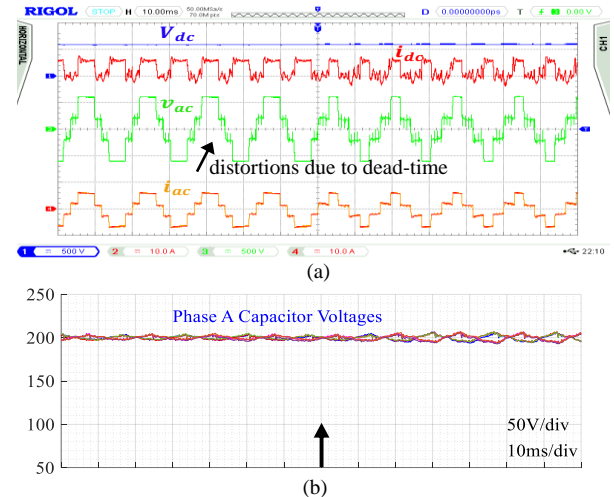
Fig. 18. 2 – ph 4 – level SCMMC experimental results under SMM with HFRS (arrow indicates modulation index change from 1 to 0.7) (a) ac and dc voltages and currents (b) capacitor voltages

4-level SCMMC prototype is developed in the laboratory.

A. Experimental Setup

The prototype parameters are shown in Table V, and the circuit and the experimental setup are shown in Fig. 16. The SCMMC is ideally comprised of switches and capacitors only and has no discrete arm inductor. In practice, however, the charging and discharging currents due to switching action gives rise to inrush currents in the converter arm, which can damage the switches, cause faults, or false-trigger gate-driver desaturation protection. For this reason, a 100μH arm inductor with the toroidal ferrite core 5952003821 from Fair-Rite has been designed to limit those currents. The minimum required inductance to limit the inrush currents is given by:

$$L_{min} = v_L \frac{dt}{di} \, , \qquad (23)$$

where v_L is the arm inductor voltage drop, di is the maximum allowable current spike, and dt is the switching period. The switches use the FF45MR12W1M1B11BOMA1 1.2kV SiC MOSFET from Infineon, and the gate driver board is based on the UCC21710QDWRQ1 gate driver IC from TI.

B. Experimental Results

The proposed SMM have been tested with RL load, where the modulation index (MI) is first set at 1 and then changed to 0.7. The MYWAY PE-Expert control system is used to generate the switching signals. The SM voltages were monitored on the controller's PE-ViewX software and the self – voltage balancing capabilities of the matrix modulation techniques of the SCMMC are assessed.

The SCMMC is first run under SMM with the LFRS, as it is the rotation scheme that generates the required staircase output voltage. The full rank symmetric switching matrix **C** presented earlier in Fig. 10.a) is used. The experimental waveforms are shown in Fig. 17. It can be seen that the ac voltages are of staircase nature. The arm current spikes are limited by the use of a small arm inductor. Finally, the capacitor voltages are balanced every fundamental cycle, and remain balanced in transient conditions when the modulation index is changed. The peak-to-peak capacitor voltage ripple is 5% with unity modulation index and 10% at MI = 0.7.

To verify the analysis of the SMM with HFRS, pattern rotation independent of the voltage level is introduced at f_{rot} = 4kHz. Fig. 18 (a) shows the ac and dc voltages and currents, and Fig. 18(b) shows the capacitor voltages under SMM with HFRS. The influence of dead-time on the staircase waveform due to pattern rotation can be clearly seen. Nevertheless, the voltage ripple on the SM capacitors is slightly smaller than that of the LFRS due to the shorter voltage balancing cycle as discussed in section III.A. The peak-to-peak capacitor voltage ripple is 3% with unity modulation index and 6% at MI = 0.7. The experimental results are hence consistent with the analysis and simulation results, and verify the operation of the SCMMC under SMM.

VI. DISCUSSION AND SUMMARY

Table VI shows the SCMMC characteristics under the proposed SMM with LFRS for both the 11-level and 4-level

Table VI. SCMMC characteristics under SMM with LFRS

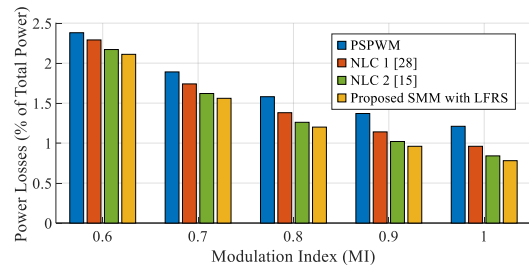| Converter at unity modulation index (MI=1)	SM Capacitor Voltage Ripple	Phase Voltage THD	Switching Frequency
4-level SCMMC	5%	18%	220 Hz
11-level SCMMC	3%	6.5%	275 Hz

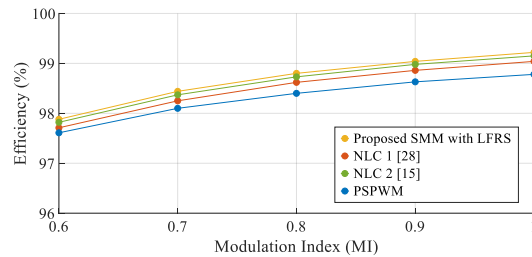Fig. 19. Power loss comparison versus modulation index

Fig. 20. Efficiency comparison versus modulation index

converters. The proposed SMM with LFRS achieves capacitor voltage ripple <5% in normal operating conditions. Moreover, with the LFRS, there are no high-frequency switching distortions due to dead-time effect as the case of HFRS. Therefore, the THD of the output voltage for SMM with LFRS will only be due to its staircase nature, and will be dependent on the discretized multilevel voltage reference (stage 1 of the SMM). In the paper, nearest level modulation (NLC) was used to discretize the voltage reference. However, selective harmonic elimination (SHE) could have been used to calculate the switching angles so that harmonic performance is optimized. This stage of discretizing the voltage reference is independent of the voltage balancing performance of the proposed SMM, and any state-of-the-art voltage reference generation can be used to improve the output voltage and current quality. The THD values of the output voltage obtained for the simulation and experimental results are documented in Table VI.

Moreover, the proposed SMM with LFRS results in very low switching losses; the switching frequency of the proposed SMM with LFRS does not go above $5f_{fund}$, even with very large number of converter voltage levels. The reason is that the term $\frac{N-1}{N}$ in the fsw_{LFRS} formula of (19) converges to 1 with very high number of submodules N. Therefore, the proposed SMM with the LFRS does not compromise efficiency due to its low switching frequency operation. A comparison in overall power losses and efficiency between the proposed SMM with LFRS and state-of-the-art methods is given in Fig. 19 and Fig. 20, respectively.

Finally, the proposed SMM with LFRS does not require

sensing the SM voltages or arm currents to achieve voltage balancing. The ability to eliminate the bulky and expensive voltage and current transducers simplifies the hardware and software implementation of SMM, and brings significant cost reduction and power density improvements, given the large number of submodules used in MMC.

VII. CONCLUSION

In this paper, a staircase matrix modulation (SMM) technique has been proposed for the SCMMC. The proposed SMM achieves sensor-less submodule capacitor voltage balancing with a staircase output voltage for the SCMMC, and is extendable to high converter voltage levels with its simple matrix generation. The proposed SMM utilizes the self-voltage balancing feature of the SCMMC, and solves the voltage unbalance limitations caused by applying YMM at low PWM frequencies. To solve these limitations, the paper proposes a compact, easy to generate, switching matrix **C**, which has both, full rank and symmetry features. A theoretical proof on the symmetry requirement has been presented. Moreover, the structure of the proposed matrix and a simple process of populating its entries in seconds for hundreds of converter voltage levels have been proposed. Two switching pattern rotation schemes were developed for SMM. The first being the high – frequency pattern rotation scheme (HFRS) proposed in [27], and the other being the low – frequency pattern rotation scheme (LFRS). HFRS features a smaller capacitor voltage ripple, but results in higher switching frequency and unneeded voltage transitions due to the dead-time effect, whereas the LFRS generates a slightly higher voltage ripple but achieves the required staircase voltage. The resulting switching frequency of the SCMMC under SMM with both rotation schemes is analyzed, and the LFRS is adopted for SMM. Finally, open and closed-loop simulations for an 11-level SCMMC under SMM are provided, and experimental results on a single-phase, 2kW, 425V, 4-level SCMMC prototype are presented to illustrate the voltage balancing capability of the proposed SMM under steady state and transient conditions. The proposed SMM with LFRS achieves <3% power losses and <5% voltage ripple without compromising the harmonic performance.
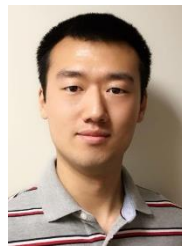
REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,* Jun. 2003, p. 6 pp. Vol.3-. doi: 10.1109/PTC.2003.1304403.

[2] H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011, doi: 10.1109/TPEL.2011.2143431.

[3] K. Sharifabadi, L. Harnefors, H. P. Nee, S. Norrga, and R. Teodorescu, *Design, control and application of modular multilevel converters for HVDC transmission systems*. Chichester, West Sussex, United Kingdom: John Wiley & Sons, Inc, 2016.

[4] S. Du, A. Dekka, B. Wu, and N. Zargari, *Modular multilevel converters: analysis, control, and applications*. in IEEE Press series on power engineering, no. 67. Piscataway, NJ : Hoboken, New Jersey: IEEE Press ; Wiley, 2018.

[5] F. Z. Peng, J.-S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate DC sources for static var generation," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130–1138, 1996.

[6] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, 1999.

[7] S. Yang, Y. Liu, X. Wang, D. Gunasekaran, U. Karki, and F. Z. Peng, "Modulation and Control of Transformerless UPFC," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1050–1063, Feb. 2016, doi: 10.1109/TPEL.2015.2416331.

[8] X. Qin, W. Hu, Y. Tang, Q. Huang, Z. Chen, and F. Blaabjerg, "An improved modulation method for modular multilevel converters based on particle swarm optimization," *Int. J. Electr. Power Energy Syst.*, vol. 151, p. 109136, 2023.

[9] Q. Wang, K. Liu, K. Wang, L. Qin, J. Zhang, and Q. Pu, "Fast capacitor voltage balancing strategy based on system history operation information for MMC," *IET Gener. Transm. Amp Distrib.*, vol. 13, no. 7, pp. 1104–1109, Jan. 2019, doi: 10.1049/iet-gtd.2018.6227.

[10] P. Hu, R. Teodorescu, S. Wang, S. Li, and J. M. Guerrero, "A Currentless Sorting and Selection-Based Capacitor-Voltage-Balancing Method for Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1022–1025, Feb. 2019, doi: 10.1109/TPEL.2018.2850360.

[11] Y. Okazaki, H. Matsui, M. M. Muhoro, M. Hagiwara, and H. Akagi, "Capacitor-Voltage Balancing for a Modular Multilevel DSCC Inverter Driving a Medium-Voltage Synchronous Motor," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4074–4083, Sep. 2016, doi: 10.1109/TIA.2016.2558638.

[12] M. D. Islam, R. Razzaghi, and B. Bahrani, "Arm-Sensorless Sub-Module Voltage Estimation and Balancing of Modular Multilevel Converters," *IEEE Trans. Power Deliv.*, vol. 35, no. 2, pp. 957–967, Apr. 2020, doi: 10.1109/TPWRD.2019.2931287.

[13] Y. Liao *et al.*, "A Novel Voltage Sensorless Estimation Method for Modular Multilevel Converters with a Model Predictive Control Strategy," *Energies*, vol. 17, no. 1, Art. no. 1, Jan. 2024, doi: 10.3390/en17010061.

[14] A. Ghazanfari and Y. A.-R. I. Mohamed, "A Hierarchical Permutation Cyclic Coding Strategy for Sensorless Capacitor Voltage Balancing in Modular Multilevel Converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 2, pp. 576–588, Jun. 2016, doi: 10.1109/JESTPE.2015.2460672.

[15] H. B. Gobburi, Vijay. B. Borghate, and P. M. Meshram, "A Level Enhanced Nearest Level Control for Modular Multilevel Converter without Using Sensors," *IEEE Trans. Ind. Appl.*, pp. 1–12, 2023, doi: 10.1109/TIA.2023.3270113.

[16] A. Elserougi, M. I. Daoud, A. M. Massoud, A. S. Abdel-Khalik, and S. Ahmed, "Investigation of sensorless capacitor voltage balancing technique for modular multilevel converters," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2014, pp. 1569–1574. doi: 10.1109/IECON.2014.7048711.

[17] A. A. Elserougi, A. M. Massoud, and S. Ahmed, "Modular Multilevel Converter-Based Bipolar High-Voltage Pulse Generator With Sensorless Capacitor Voltage Balancing Technique," *IEEE Trans. Plasma Sci.*, vol. 44, no. 7, pp. 1187–1194, Jul. 2016, doi: 10.1109/TPS.2016.2575861.

[18] Z. Li, R. Lizana F., S. Sha, Z. Yu, A. V. Peterchev, and S. M. Goetz, "Module Implementation and Modulation Strategy for Sensorless Balancing in Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8405–8416, Sep. 2019, doi: 10.1109/TPEL.2018.2886147.

[19] N. Tashakor, M. Kılıçtaş, J. Fang, and S. M. Goetz, "Switch-Clamped Modular Multilevel Converters With Sensorless Voltage Balancing Control," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9586–9597, Oct. 2021, doi: 10.1109/TIE.2020.3028814.

[20] Y. Pang, G. Ma, X. Liu, X. Xu, and X. Zhang, "A New MMC Sub-Module Topology with DC Fault Blocking Capability and Capacitor Voltage Self-Balancing Capability," *Energies*, vol. 14, no. 12, Art. no. 12, Jan. 2021, doi: 10.3390/en14123409.

[21] J. Huang, K. Li, Y. Ye, and X. Wang, "Self-Balanced Clamp-Double Submodule for Modular Multilevel Converter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 6, pp. 7249–7260, Dec. 2022, doi: 10.1109/JESTPE.2022.3197607.

[22] Y. Liu and F. Z. Peng, "A modular multilevel converter with self-voltage balancing part I: Mathematical proof," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 2, pp. 1117–1125, 2019.

[23] Y. Liu and F. Z. Peng, "A modular multilevel converter with self-voltage balancing part II: Y-matrix modulation," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 2, pp. 1126–1133, 2019.

[24] Y. Liu, F. Z. Peng, and L. M. Tolbert, "Arm Inductance Quantification for Y-Matrix Modulated Modular Multilevel Converter," in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, IEEE, pp. 3499–3504.

[25] R. F. Yehia, K. Schoder, R. B. Gonzatti, M. Steurer, and F. Z. Peng, "Startup of the Switched-Capacitor Modular Multilevel Converter with Middle Submodule," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2022, pp. 01–07. doi: 10.1109/ECCE50734.2022.9947644.

[26] R. F. Yehia, "Switched-Capacitor Modular Multilevel Converter To Achieve Inductor-less, Filter-less, and Transformer-less Medium-Voltage Power Conversion For High Power Density Applications," Ph.D. Dissertation, Florida State University, Tallahassee, FL, USA, 2023.

[27] R. F. Yehia and F. Z. Peng, "Staircase Matrix Modulation for the Switched-Capacitor Modular Multilevel Converter with Sensor-less Voltage Balancing," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2023, pp. 2839–2844. doi: 10.1109/APEC43580.2023.10131172.

[28] G. Konstantinou, J. Pou, S. Ceballos, R. Darus, and V. G. Agelidis, "Switching frequency analysis of staircase-modulated modular multilevel converters and equivalent PWM techniques," *IEEE Trans. Power Deliv.*, vol. 31, no. 1, pp. 28–36, 2015.

[29] Y. Liu, "A Modular Multilevel Converter With Self Voltage Balancing," PhD Dissertation, Michigan State University, East Lansing, Michigan, 2019. [Online]. Available: https://d.lib.msu.edu/etd/48028/datastream/OBJ/view

Zhehui Guo (Member, IEEE) received the B.S. and M.S. degrees from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2015 and 2018, respectively, and the Ph.D. degree from Florida State University, Tallahassee, FL, USA, in 2022, all in electrical engineering. He is currently a Member of R&D Staff with Milan M. Jovanović Power Electronics Laboratory, Delta Electronics (Americas) Ltd., Research Triangle Park, NC, USA. From 2022 to 2023, he was a Postdoctoral Research Scholar with the Center for Advanced Power System, Florida State University. His research interests include wide bandgap power devices and their applications, power factor correction rectifier, high-voltage and high-power power electronics systems.

Hui Li (Fellow, IEEE) received the B.S. and M.S. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 1992 and 1995, respectively, and the Ph.D. degree from the University of Tennessee, Knoxville, TN, USA, in 2000, all in electrical engineering. She is currently a Professor with the Electrical and Computer Engineering Department, Florida A&M University–Florida State University College of Engineering, Tallahassee, FL, USA. Her research interests include PV converters, energy storage applications, and smart grid.
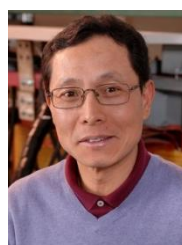
Rami F. Yehia (Member, IEEE) received his B.E. degree from the Notre Dame University-Louaize, Zouk Mosbeh, Lebanon in 2018 and his M.S. and Ph.D. degrees from the Florida State University, Tallahassee, FL, USA, in 2021 and 2023, respectively, all in electrical engineering. During his Ph.D., he has been a graduate research assistant in Dr. Fang Z. Peng's research group at the Center for Advanced Power Systems, Florida State University, where he worked on the control and modulation of the switched-capacitor modular multilevel converter (SCMMC) for renewable energy applications. In August 2023, he joined the Vehicle Electrification Systems team at Aptiv PLC as a lead power electronics hardware engineer, where he is working on circuit design of power electronic converters for electric vehicles, including on-board chargers (OBC), dc-dc converters, and back-up energy storage modules.

Fang Z. Peng (Fellow, IEEE) received the B.S. degree from Wuhan University, Wuhan, China, in 1983, and the M.S. and Ph.D. degrees from the Nagaoka University of Technology, Nagaoka, Japan, in 1987 and 1990, respectively, all in electrical engineering. From 1990 to 1992, he was a Research Scientist with Toyo Electric Manufacturing Company, Ltd., Tokyo, Japan, where he was engaged in the research, development, and commercialization of active power filters, flexible ac transmission system (FACTS) applications, and motor drives. From 1992 to 1994, he was with the Tokyo Institute of Technology, Tokyo, as a Research Assistant Professor, where he initiated a multilevel inverter program for FACTS applications and speed sensorless vector control of motors. From 1994 to 2000, he was with the Oak Ridge National Laboratory, Oak Ridge, TN, USA, where he became the Lead (Principal) Scientist for the Power Electronics and Electric Machinery Research Center from 1997 to 2000. From 2000 to 2018, he was with Michigan State University, East Lansing, MI, USA, where he was promoted to a Full Professor in 2006 and designated as a University Distinguished Professor in 2012. Since 2018, he has been with the Center for Advanced Power Systems, Florida State University, Tallahassee, FL, USA, as the inaugural Distinguished Professor of Engineering. His multilevel inverter research and development have benefited the power industry and promoted grid-scale applications around the world.