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A Double-Sided Cooling Approach of Discrete SiC MOSFET Device Based on Press-Pack Package

RAN YAO [1] (Member, IEEE), ZHEYAN ZHU [2] (Student Member, IEEE), HUI LI [1] (Member, IEEE), WEI LAI [1] (Senior Member, IEEE), XIANPING CHEN [3] (Senior Member, IEEE), FRANCESCO IANNUZZO [4] (Senior Member, IEEE), RENKUAN LIU [5] (Member, IEEE), AND XIAORONG LUO [5,6] (Senior Member, IEEE)

[1]State Key Laboratory of Power Transmission Equipment, School of Electrical Engineering, Chongqing University, Chongqing 400044, China
[2]College of Electrical Engineering, Zhejiang University, Hangzhou 310058, China
[3]College of Optoelectronic Engineering, Chongqing University, Chongqing 400044, China
[4]Department of Energy Technology, Aalborg University, DK- 9220 Aalborg, Denmark
[5]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China
[6]College of Microelectronics, Chengdu University of Information Technology, Chengdu 610225, China

CORRESPONDING AUTHORS: ZHEYAN ZHU; HUI LI (e-mail: zjusyusan@zju.edu.cn; cqulihui@cqu.edu.cn).

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ABSTRACT The conventional TO-247-3 packages with single-sided cooling limit the thermal and electrical performances of discrete SiC MOSFET devices. In this paper, a double-sided cooling press-pack (PP) packaging approach for the discrete SiC MOSFET device is proposed to optimize its thermal and electrical performances. First, a double-sided cooling PP structure for the discrete SiC MOSFET devices is designed with a copper foam gate pin and an embedded fixture. Then, based on finite element simulations, the steady-state thermal and electrical performances of the discrete SiC MOSFET device with the double-sided cooling PP package are analyzed, and the parasitic inductance of the designed SiC MOSFET device is extracted by the ANSYS Q3D software. Finally, a prototype of the double-sided cooling PP SiC MOSFET device is fabricated, and test platforms are established to verify its performance. The research findings demonstrate that the designed double-sided cooling PP SiC MOSFET device can reduce thermal resistance and switching loss by 47.4 % and 42.3%, respectively.

INDEX TERMS Double-sided cooling, press-pack package, discrete SiC MOSFET device, finite element modeling, performances optimization.

I. INTRODUCTION

SiC MOSFETs, renowned for their high switching speed, high junction temperature operation capacity, and high blocking voltage, are widely applied in electric vehicles, aerospace, and photovoltaic inverter, etc. [1], [2]. When SiC MOSFET devices are used in charging stations and photovoltaic inverters, they face many challenges. 1) With the development of electric vehicles, charging stations require higher efficiency. SiC MOSET devices require higher switching frequencies and voltages, which poses challenges to the parasitic inductance and packaging structure in the SiC MOSET device design [3], [4]. 2) When the SiC MOSET devices operate in photovoltaic inverters, the SiC MOSET devices face high-temperature conditions, with operating temperatures possibly exceeding 125 °C, which poses a challenge to the heat dissipation in the SiC MOSET device design [5], [6], [7].

Currently, the voltage levels of industrial discrete SiC MOSFET devices are mainly 650 V, 750 V, and 1200 V, and they are packaged with a TO-247-3 and TO-247-4 structure as shown in Fig. 1. However, compared to the TO-247-3 and

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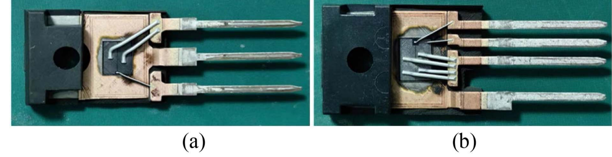


FIGURE 1. Internal structure. (a) TO-247-3; (b) TO-247-4.

TO-247-4 SiC MOSFET devices, the TO-247-4 SiC MOSFET devices have added Kelvin source pins, which are used to decouple the drive circuit from the power circuit and improve the switching speed. However, the power circuits of the TO-247-3 and TO-247-4 devices are the same, and the inductance of the power circuit has not been optimized. Conventional TO-247 discrete SiC MOSFET device packaged with wire-bonded and single-sided cooling, resulting in limited heat dissipation capability and high parasitic inductance. Poor heat dissipation capability can lead to high junction temperature (T_j), increasing the on-voltage (V_{ds}), and conduction loss of the discrete SiC MOSFET [8]. Additionally, the inductance of the power circuit introduced by the bonding wires in the package can lead to overshoot and ringing during rapid switching, adversely impacting the high-frequency switching characteristics of the discrete SiC MOSFET devices [9], [10]. Therefore, it is necessary to optimize the electrical and thermal performance of SiC MOSFET devices.

The SiC MOSFET with double-sided cooling (DSC) package has two heat dissipation paths from SiC MOSFET chip to the top surface and bottom surface, which increases the heat dissipation efficiency and reduces the thermal resistance of the SiC MOSFET device [11]. Reference [12] uses DBC substrates for electrical connection on both sides of the SiC MOSFET device and then welds it onto a liquid cooling plate, reducing the thermal resistance by 38%. Reference [13] compared the thermal resistance of the SiC MOSFET operating with single-sided cooling and DSC, and the results show that the thermal resistance of the SiC MOSFET under DSC is about 25% lower than that under single-sided cooling.

On the other hand, the DSC package can change the planar commutation path to a direction perpendicular to the SiC MOSFET chip, reducing the parasitic inductance of the package. The reference [14] embeds fuzz buttons into a low-temperature co-fired ceramic (LTCC) layer, and the whole is laminated on the upper surface of the SiC MOSFET chips as an intermediary to achieve electrical connection. An external fixture is used to achieve suitable pressure contact on the surface of the chips, and the parasitic inductance of its power circuit is only 4.3 nH. Reference [15] embeds SiC MOSFET chips in copper busbars by combining stacking technology to reduce package size and parasitic inductance. The busbars are insulated with polyethylene terephthalate films, and the PEEK bolts are used around the chips to achieve uniform pressure distribution. The parasitic inductance of the power circuit is 8.7 nH. However, the above proposed DBC packaging methods for the SiC MOSFET device are complex and need some special packaging materials, which are not suitable for commonly discrete SiC MOSFET devices.

Press-Pack (PP) packaging is a simple DSC method that has been widely used for a high-power density (3300 V/3000 A) Si IGBT device [16]. The PP packaging uses contact pressure to achieve parallel connections of multiple large dies instead of bonding wires and soldering to realize thermal and electrical connections, resulting in lower thermal resistance and parasitic inductance [17]. However, the electron velocity of the SiC is 3 times higher than the Si [18]. At the same voltage and current level, the area of the SiC MOSFET chip is about 17% smaller than that of the Si IGBT chip, and the gate area of the SiC MOSFET chip is 1/3 smaller than that of the Si IGBT chip. The smaller size of the SiC MOSFET chip makes it complex and difficult to directly apply with the existing PP structures.

This paper proposes a DSC method for discrete SiC MOSFET devices based on the PP package to optimize electrical and thermal performances. In Section II, a double-sided cooling PP package with a foam copper gate pin and a DSC structure is designed for a discrete SiC MOSFET device. Then, according to COMSOL Multiphysics and Ansys Q3D simulation results, the electrical and thermal performances and parasitic inductance distribution of the SiC MOSFET device are analyzed in Section III. In Section IV, the experimental platforms are built to evaluate and verify the performances of the proposed PP SiC MOSFET package, and the experiment results on the proposed and the TO-247-3 SiC MOSFET are compared. Section V concludes this paper.

II. STRUCTURE OF PP DISCRETE SIC MOSFET DEVICE

A. THE STRUCTURE OF PROPOSED PP SIC MOSFET DEVICE

The structure of the double-sided cooling PP packaging for the discrete SiC MOSFET device is shown in Fig. 2.

The SiC MOSFET chip is BC1M032120 (1200 V 32 mΩ) from the BASiC Semiconductor. The size of the SiC MOSFET chip is 6.5 mm × 4.5 mm × 0.39 mm. Two molybdenum plates are chosen as the buffer material placed on both sides of the chip to reduce the thermal-mechanical stress on both surfaces of the SiC MOSFET chip during power cycling because the Young's modulus and the coefficient of thermal expansion (CTE) of the molybdenum are close to the SiC material. The thickness of two molybdenum plates is 0.4 mm, and the corners of the molybdenum plate are rounded with a radius of 0.2 mm to prevent damage to the SiC MOSFET chip under uneven or excessive pressure. The area of the source pad on the SiC MOSFET chip is about 22 mm^2, which is very small. To prevent failure caused by excessive stress on the source pad of the SiC MOSFET chip, a soft silver shim of 0.1 mm thickness is placed between the SiC MOSFET chip and the source molybdenum plate to balance the pressure.

The PEEK frame plays a constraint role in the double-sided cooling PP package, which is used to constrain the position of the source molybdenum plate, the silver shim, the SiC MOSFET chip, and the drain molybdenum plate.

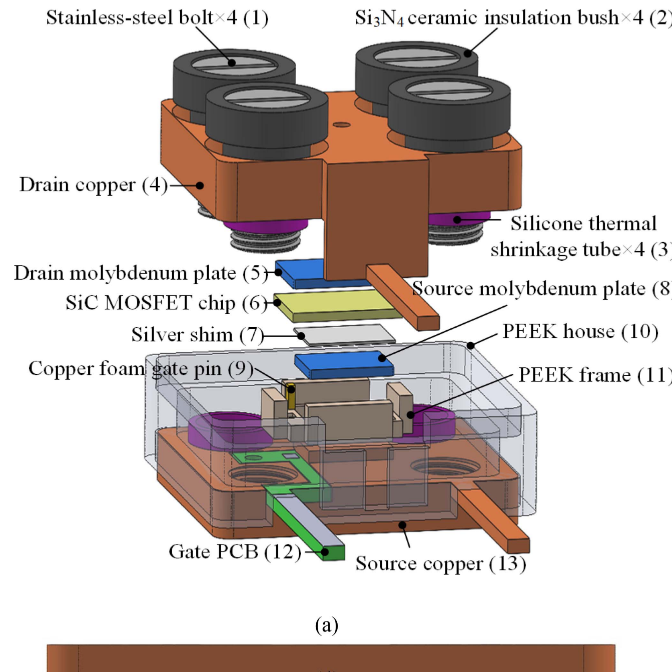


FIGURE 2. **The structure of proposed double-sided cooling PP SiC MOSFET. (a) Explosion view. (b) Perspective view from the front.**

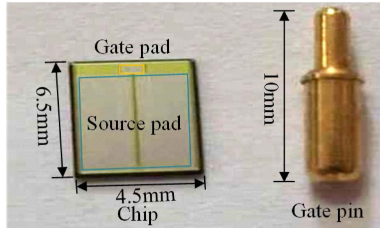


FIGURE 3. **the SiC MOSFET chip and conventional gate pin for PP IGBT.**

B. GATE PIN

As shown in Fig. 3, due to the limited gate contact area of the SiC MOSFET chip, the area of the gate pad is only 0.48 mm × 0.8 mm on the source pad of the SiC MOSFET chip. The conventional spring gate pin used for the PP IGBT device is challenging to directly apply to the PP SiC MOSFET device. Moreover, the conventional gate pin is relatively long and requires a tall post to match it, significantly increasing the device's heat dissipation and current paths.

Copper foam is a porous material characterized by electrical conductivity comparable to copper and excellent elasticity,

TABLE 1. **Material Properties of Copper Foam [20]**

Parameters	Value	Parameters	Value
Electrical Conductivity ($\times 10^6$ S/m)	58	Thermal Capacity (J/kg·K)	385.2
Density (g/cm^3)	3.75	Young's Modulus (MPa)	16.9
Thermal Conductivity (W/m·K)	0.4	Poisson's Ratio (1)	0.32

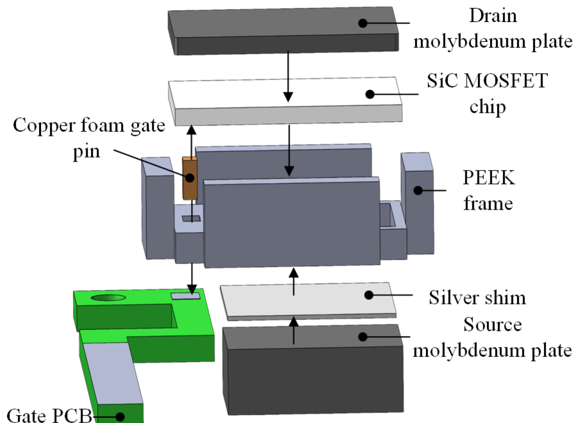


FIGURE 4. **A exploded view for the installation of the copper foam gate pin in the PEEK frame.**

making it suitable for fabrication into a gate pin [19]. The material properties of copper foam are shown in Table 1 [20].

To fit the small gate pad of the SiC MOSFET chip, the copper foam with a porosity of 95% is shaped into a rectangular gate pin with the length of 0.6 mm, the width of 0.4 mm, and the height of 1.2 mm. The exploded view for the installation of the copper foam gate pin, SiC MOSFET chip, drain molybdenum plate, silver shim, and source molybdenum plate in the PEEK frame is shown in Fig. 4. The drain molybdenum plate is placed on top of the SiC MOSFET chip, both are placed inside PEEK frame and fixed by four pillars. The copper foam gate pin connects the gate pole of the SiC MOSFET chip and the gate PCB through the small hole inside the PEEK frame. The small hole is specially processed based on the position of the SiC MOSFET chip gate pole. The source molybdenum plate is placed under the silver shim, and both are placed in a big hole of the PEEK frame and connected to the source surface of the SiC MOSFET chip.

The actual diagram of the copper foam gate pin and the source molybdenum plate placed in the PEEK frame is shown in Fig. 5(a). The deformation of the copper foam gate pin under vertical pressure is shown in Fig. 5(b).

C. DISTRIBUTED PRESSURE CONTACT

The pressure of the package is important for the thermal, and electrical contact characteristics of the PP SiC MOSFET. The distributed clamping method is used to achieve even pressure distribution on the SiC MOSFET chip surfaces and reduce

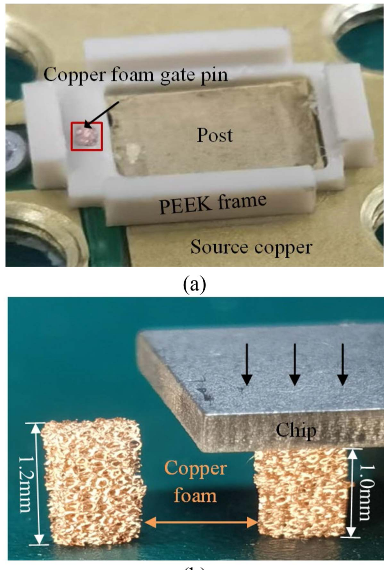


FIGURE 5. The actual diagram of the copper foam gate pin in the PEEK frame. (a) A copper foam gate pin in the Peek frame. (b) Enlarged view of copper foam gate pins.

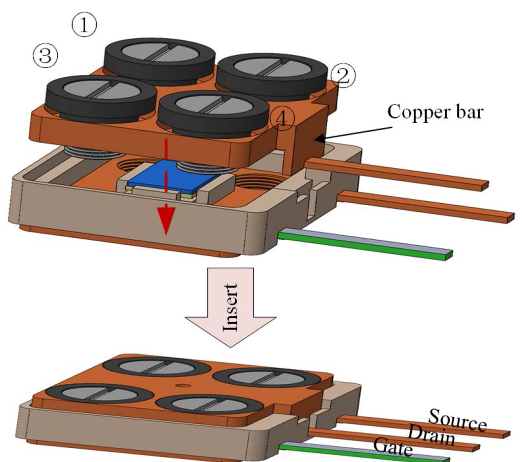


FIGURE 6. Tightening process of stainless-steel bolts.

package volume [21]. To ensure good electrical contact with the SiC MOSFET chip, the surface pressure of the chip should be between 10–20 MPa [22]. In the proposed PP discrete SiC MOSFET device package, the pressure is generated by the combined tightening force of 4 stainless-steel bolts with a thread diameter of 4 mm and a thread length of 5 mm. The 4 bolts are arranged at the corners of the proposed PP discrete SiC MOSFET device, as shown in Fig. 6.

Fuji pressure measurement films, with a maximum pressure range of 2 to 12 MPa, are utilized to assess the pressure distribution on the source and drain faces of the SiC MOSFET chip, as shown in Fig. 7. By referencing a corresponding color sample tested under identical conditions, the average pressure on the most areas of the source and drain surfaces of the SiC

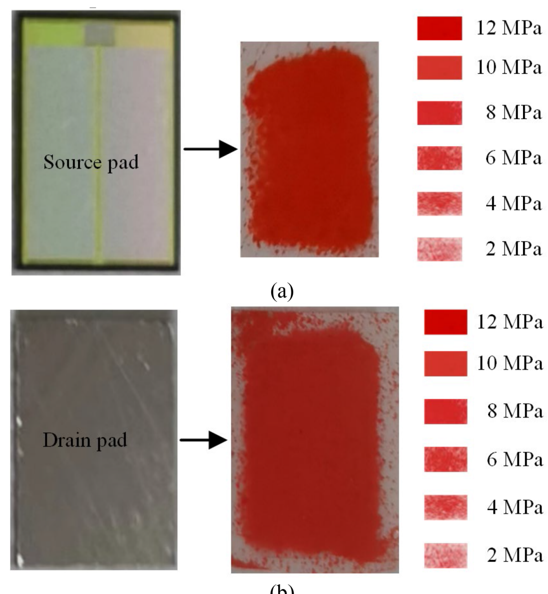


FIGURE 7. Pressure distribution. (a) Source surface. (b) Drain surface.

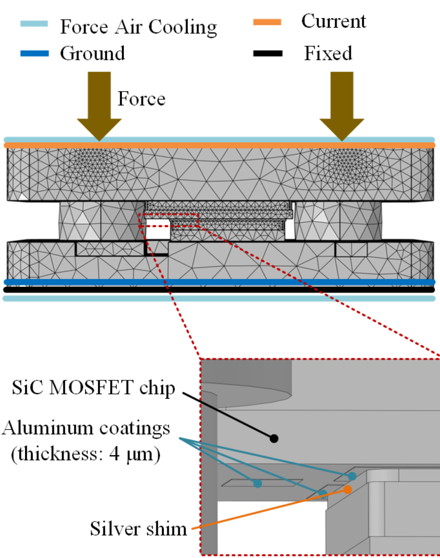


FIGURE 8. The finite element model and boundary conditions of the proposed PP SiC MOSFET device.

MOSFET chip are about 10 MPa. The pressure test results indicate that the distributed clamping method can provide sufficient pressure and ensure uniform pressure distribution on the surface of the SiC MOSFET chip.

III. FINITE ELEMENT SIMULATION ANALYSIS

A. STEADY-STATE FINITE ELEMENT SIMULATION

The finite element model of the proposed double-sided cooling PP SiC MOSFET device is established by COMSOL Multiphysics software, as shown in Fig. 8. The aluminum coatings on the source surface of the SiC MOSFET chip are

TABLE 2. Material Parameters Set in the Simulation

Parameters	Cu	Mo	Ag	SS	SiC	Si_3N_4	Al	Solder
CTE (10^{-6}/K)	17	4.8	18.9	17.2	4.3	3.0	23.6	23
Young's Modulus (GPa)	110	312	83	193	410	300	70	40
Poisson's Ratio (1)	0.35	0.3	0.37	0.29	0.45	0.24	0.32	0.4
Thermal Conductivity (W/m·K)	400	138	429	16.3	490	30	200	50
Thermal Capacity (J/kg·K)	385	250	235	500	800	710	880	150
Density (kg/m^3)	8960	10220	10500	7930	3210	3220	2700	7440

TABLE 3. Parameters of Boundary Conditions Set in the Simulation

Parameters	Value	Parameters	Value
Force (N)	75	Room temperature (°C)	25
Current (A)	20	Forced Air cooling (W/(m^2·K))	450

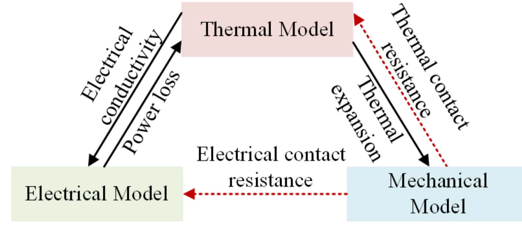


FIGURE 9. Multiphysics coupling relationship of SiC MOSFET.

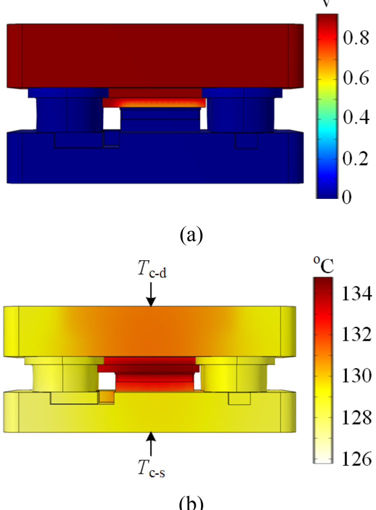


FIGURE 10. Steady-state simulation results of the PP SiC MOSFET device. (a) Voltage. (b) Temperature.

considered in the finite element model. The threaded parts of stainless-steel bolts are simplified as cylindrical bodies. The clamping force and the conducting current are applied on the drain copper, the mechanical fixed, the force air cooling and the ground are set on the source copper.

The material parameters used in the simulation are shown in Table 2 [23]. The parameters of boundary conditions set in the simulation are listed in Table 3. The electrical conductivity of the SiC MOSFET chip can be calculated based on its relationship with T_j by the datasheet.

The electrical, thermal, and mechanical coupling relationship of the PP SiC MOSFET device in the finite element simulation is shown in Fig. 9.

In the finite element simulation for the PP SiC MOSFET device, the clamping force will affect the electrical and thermal contact resistance between contact surfaces of adjacent materials. In this case, electrical and thermal contact should be added in COMSOL. The thermal contact resistance can be estimated by (1) [24]:

$$\begin{cases} R_{\text{thermal}} = 1/(A \cdot h_c) \\ h_c = 1.25 \cdot k_s \cdot (m/\sigma) \cdot (P/H_c)^{0.95} \end{cases} \tag{1}$$

where A is the nominal contact area, h_c refers to the thermal contact conductance, k_s represents the mean thermal conductivity, m is the mean absolute slope of the interface, σ indicates the effective root mean square of surface roughness, P is the contact pressure of the joint, and H_c is the hardness of the soft material.

The electrical contact resistance can be calculated as follows [24]:

$$R_{\text{electrical}} = (\rho_1 + \rho_2)/2 \cdot \sqrt{\pi \cdot H_c/P} \tag{2}$$

where ρ_1 and ρ_2 denote the electrical resistivity of two contact layers, respectively.

The steady-state simulation results of electrical and thermal performances for the PP SiC MOSFET device are shown in Fig. 10. The V_{ds} of the PP SiC MOSFET device is only 0.94 V. Compared with the V_{ce} of the same SiC MOSFET chip with the TO package in the datasheet (B2M032120Y), the PP packaging for the SiC MOSFET device reduces the V_{ce} by about 0.1 V [25]. The T_j of the PP SiC MOSFET device is about 134 °C. The case temperatures of the drain surface and the source surface are 131.7 °C and 128.4 °C, respectively.

The steady-state R_{th} of the PP SiC MOSFET devices can be calculated based on the finite element simulation results. The PP package has two heat dissipation paths. Its thermal resistance (R_{th_double}) can be calculated by [26]:

$$R_{th_double} = \frac{(T_j - T_{c-d})(T_j - T_{c-s})}{P_{loss}\left(T_j - \frac{2T_{c-d} \cdot T_{c-s}}{T_{c-d} + T_{c-s}}\right)} \tag{3}$$

where P_{loss} is the conduction loss of the device, T_j is the junction temperature of the device, T_{c-d} and T_{c-s} are the case temperatures of the drain and source of the device, respectively.

The thermal resistance of the PP SiC MOSFET device calculated by (3) is 0.221 K/W. Compared with the thermal

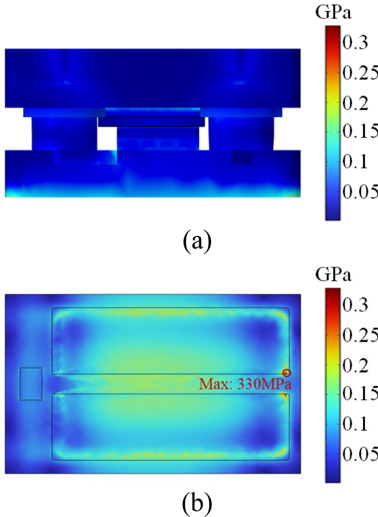


FIGURE 11. von Mises stress distribution of the PP SiC MOFSET device. (a) The device. (b) The source pad.

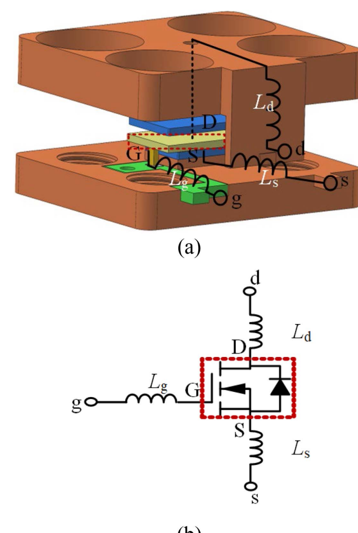


FIGURE 12. The parasitic inductance distribution of the PP SiC MOSFET device. (a) The device. (b) Schematic.

resistance of the same SiC MOSFET chip packaging with the TO-247-4 in the datasheet, the PP packaging for the SiC MOSFET device reduces the thermal resistance by about 0.18 K/W [25].

The steady-state simulation results of von Mises stress distribution for the PP SiC MOSFET are shown in Fig. 11. Given that the source surface of the SiC MOSFET chip is the most vulnerable part in the device during operation, the source surface is extracted and analyzed [22]. As shown in Fig. 8, the stress in the PP package is concentrated at the contact edge between the source surface of the SiC MOSFET chip and the silver shim. The maximum stress at the corner of the aluminum coating on the source surface of the chip is 330 MPa.

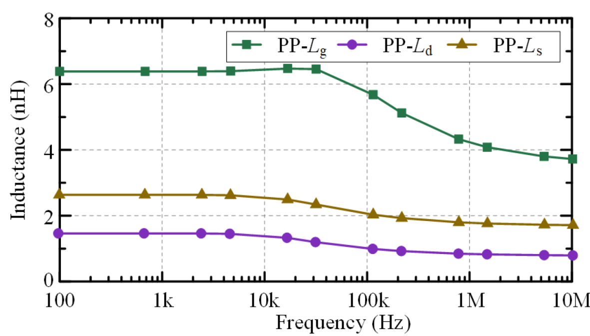


FIGURE 13. Parasitic inductance simulation results of the PP SiC MOSFET device with different frequencies.

B. PARASITIC INDUCTANCE

The parasitic inductance of the PP SiC MOSFET device without leads is extracted by the ANSYS Q3D software. The parasitic inductance distribution in the PP SiC MOSFET device is shown in Fig. 12.

The parasitic inductance of the PP SiC MOSFET device is extracted from 100 Hz to 10 MHz, as shown in Fig. 13. Before 10 kHz, the parasitic inductances of L_g, L_d, and L_s in the PP SiC MOSFET are about 6.2 nH, 2.7 nH, and 1.5 nH, respectively. When the frequency increases from 10 kHz to 1 MHz, the parasitic inductances of the PP SiC MOSFET decrease rapidly. When the frequency is 10 MHz, the parasitic inductances of L_g, L_d, and L_s in the PP SiC MOSFET are about 3.9 nH, 1.8 nH, and 0.9 nH, respectively.

The parasitic inductance of the TO-247-3 device without leads is analyzed by the ANSYS Q3D software to verify the optimization of the parasitic inductance of the proposed PP SiC MOSFET device, as shown in Fig. 14(a). With the same simulation condition of the PP SiC MOSFET device, the parasitic inductance of the TO-247-3 SiC MOSFET device is shown in Fig. 14(b). Before 10 kHz, the parasitic inductances of L_g, L_d, and L_s in the TO-247-3 SiC MOSFET are about 9 nH, 5.9 nH, and 1.6 nH, respectively. When the frequency is beyond 1 MHz, the parasitic inductances of L_g, L_d, and L_s in the TO-247-3 SiC MOSFET are about 7.2 nH, 4.3 nH, and 1 nH, respectively.

The comparison of the parasitic inductance between TO-247-3 and PP SiC MOSFET device is shown in Fig. 15. The three equivalent parasitic inductances L_g, L_d, and L_s of the PP SiC MOSFET device are significantly reduced compared to the TO-247-3 device. Among them, a 54.2% decrease in L_d has the most significant improvement effect. Compared with the TO-247-3 device, the parasitic inductance L_{gs} of the drive circuit and the parasitic inductance L_{ds} of the power circuit in the PP SiC MOSFET device decreased by 27.3% and 44%, respectively.

The magnetic field simulations are conducted on the power circuits of two SiC MOSFET devices by using COMSOL multi-physics simulation software. In order to ignore the influence of the leads on the inductance of the TO-247-3 and the

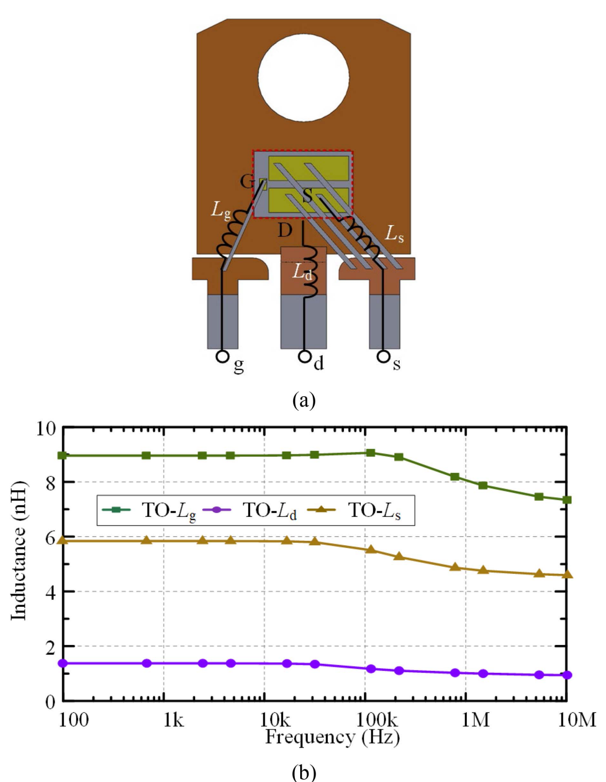


FIGURE 14. Parasitic inductance analysis of the TO-247-3 SiC MOSFET device. (a) The parasitic inductance distribution; (b) Simulation results.

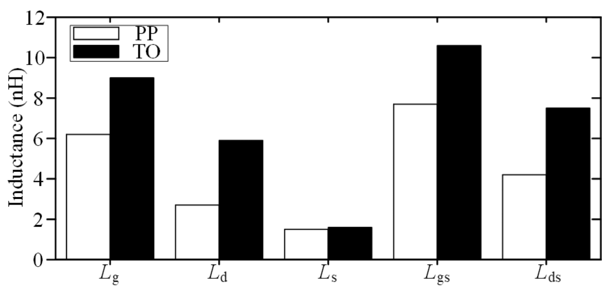


FIGURE 15. Parasitic inductance analysis of the TO-247-3 SiC MOSFET device. (a) The parasitic inductance distribution; (b) Simulation results.

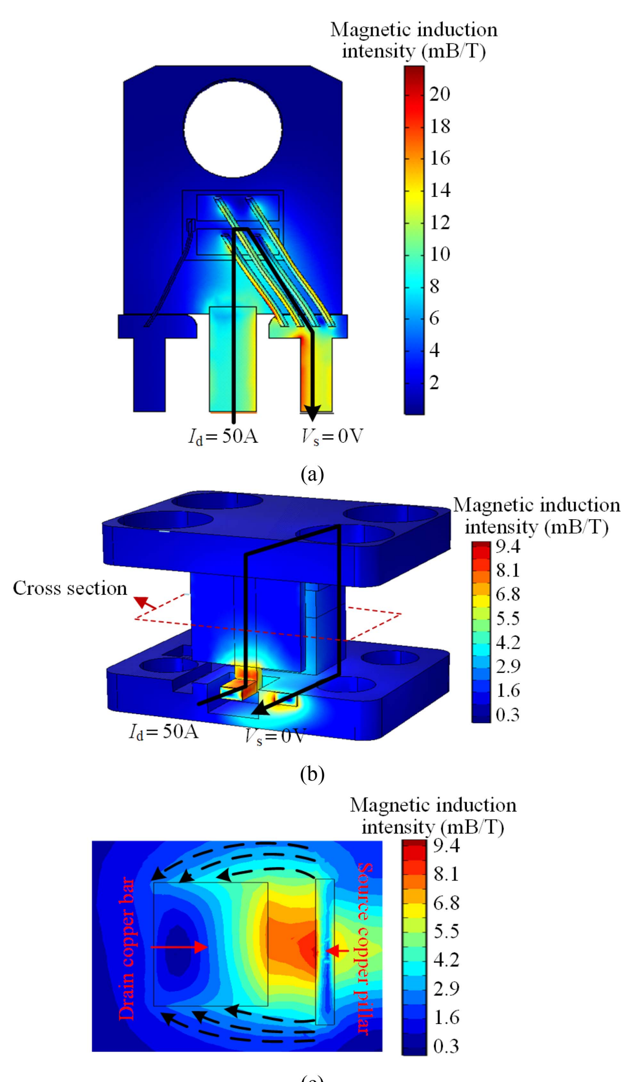


FIGURE 16. The magnetic field distribution. (a) TO-247-3 SiC MOSFET device; (b) PP SiC MOSFET device; (c) Cross section view of the PP device.

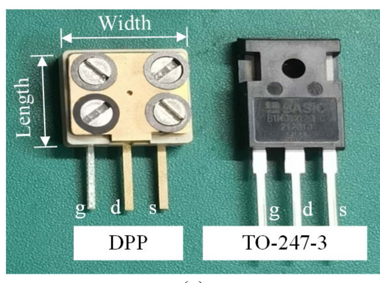
PP SiC MOSFET device, only the internal inductance simulations of the two devices are conducted. The drain current I_d is set to 50 A, and the external environment of the devices is air. The simulation results are shown in Fig. 16.

The magnetic field distribution of the TO-247-3 SiC MOSFET is concentrated at the source, bonding wire, and drain, as shown in Fig. 16(a). In the PP SiC MOSFET device, the power circuit is a vertical commutation circuit, the drain copper bar is adjacent to the source copper pillar, and the magnetic field concentrated between the drain copper bar and the source copper pillar, as shown in Fig. 16(b). Because the current flowing through the drain copper bar and the source copper pillar are equal in magnitude and opposite in direction, the generated magnetic flux can cancel each other out. The magnetic induction line between the drain copper bar and the source copper pillar is shown in Fig. 16(c). The power circuit design of the PP SiC MOSFET device utilizes the principle of magnetic field cancellation [27], [28]. The maximum power circuit magnetic field distribution of the PP SiC MOSFET device is less than half that of the TO-247-3 device.

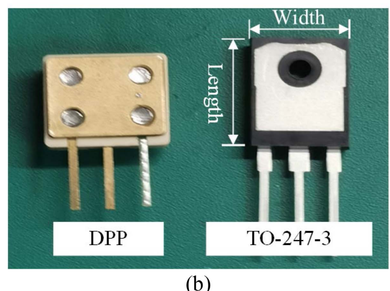
IV. EXPERIMENTAL VERIFICATIONS

The prototype of the PP SiC MOSFET device is fabricated, as shown in Fig. 17. The comparison of the dimensions between the PP package and the TO-247-3 package with the same SiC MOSFET chip is shown in Table 4. The tested TO-247-3 SiC MOSFET is B1M032120HC (1200 V 32 mΩ) from the BASiC Semiconductor.

The dimension of the PP SiC MOSFET device and the TO-247-3 SiC MOSFET device is shown in Table 4. The volume of the proposed PP SiC MOSFET device is 100 mm^3 smaller



(a)



(b)

FIGURE 17. Prototype of the PP SiC MOSFET compared with TO-247-3 device. (a) Front view. (b) Back view.

TABLE 4. Dimension Comparisons of the Two Packages

Parameters	TO-247-3	PP
Length (mm)	20.95	14.83
Width (mm)	16.10	17.92
Thickness (mm)	5.19	6.21
Volume (mm^3)	1750.56	1650.33

than that of the TO-247-3 SiC MOSFET device, which is more favorable for improving the power density of the SiC MOSFET device.

A. STEADY-STATE ELECTRICAL AND THERMAL PERFORMANCE TEST

A steady-state test platform is established to evaluate and compare the steady-state electrical and thermal performances of the PP and the TO-247-3 SiC MOSFET device, as shown in Fig. 18.

A programmable current source, controlled by LabVIEW on the PC, is utilized to supply a constant current I_d. Two powerful air-cooling fans are set at symmetrical positions on both sides of the SiC MOSFET device, which is used to control the case temperature of the device. NI signal acquisition card cards are used to collect voltage and temperature signals separately during the test process.

The installation diagram of the PP SiC MOSFET device on the heatsink is shown in Fig. 19(a). Two heatsinks are connected to the PP SiC MOSFET by silicon grease, and the PP SiC MOSFET device is fully inserted into the terminal to reduce the impact of lead inductance on the device. Compared with the installation of the TO-247-3 SiC MOSFET devices, as shown in Fig. 19(b), the proposed device has the same number of pins and can dissipate heat on both sides, which has enabled the replacement of the TO-247-3 SiC MOSFET devices.

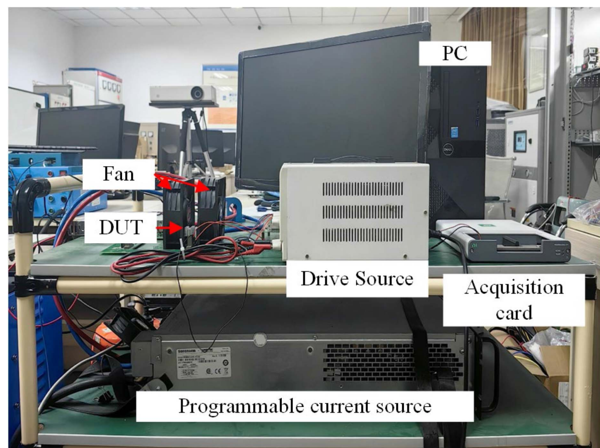
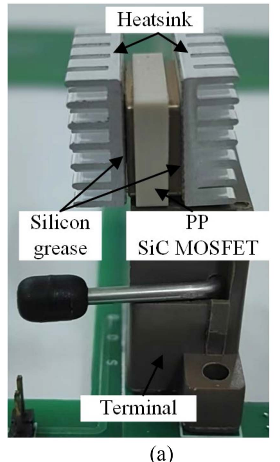


FIGURE 18. Steady-state test platform.



(a)

(b)

FIGURE 19. The installation of the SiC MOSFET device on the heatsink. (a) The PP SiC MOSFET device; (b) The To-247-3 SiC MOSFET device.

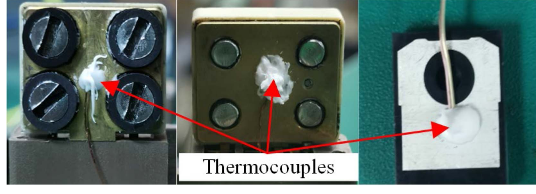


FIGURE 20. The installation of the thermocouples on the SiC MOSFET.

Thermocouples are attached to the drain and source surfaces of the device to measure their T_c, as shown in Fig. 20. Considering the linear relationship between V_{ds} and T_j of the SiC MOSFET device, V_{ds} serves as a temperature-sensitive electrical parameter to measure the T_j of the SiC MOSFET device without damaging their cases. The relationships between V_{ds} and T_j of the PP and TO SiC MOSFET device are

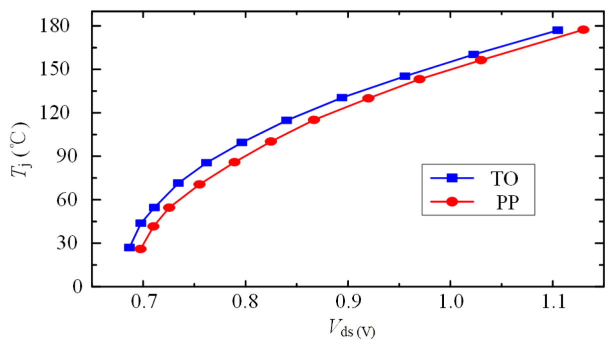


FIGURE 21. The relationships between V_{ds} and T_j of the DUTs.

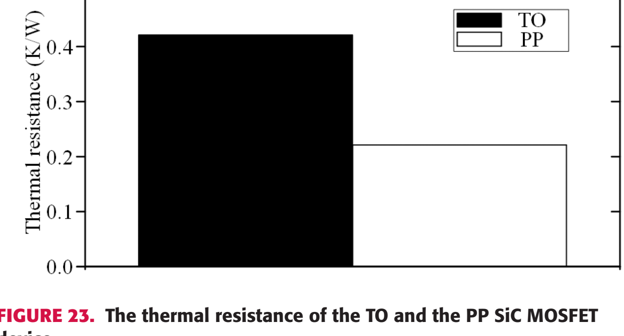


FIGURE 23. The thermal resistance of the TO and the PP SiC MOSFET device.

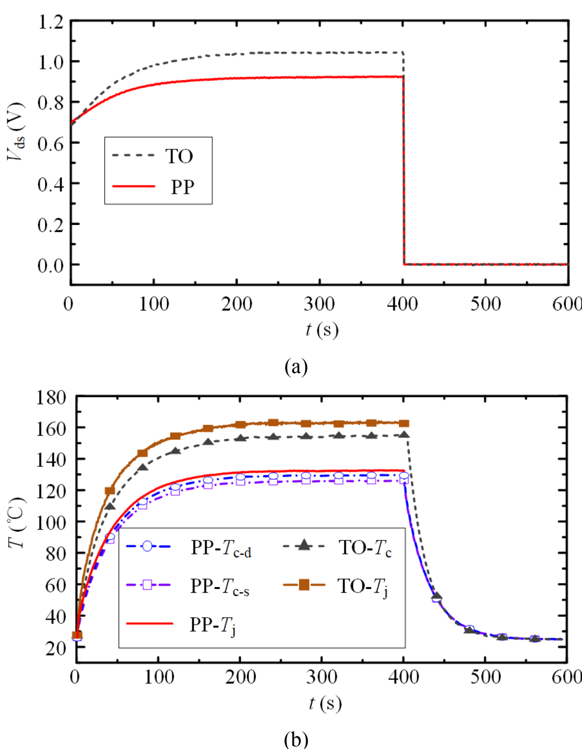
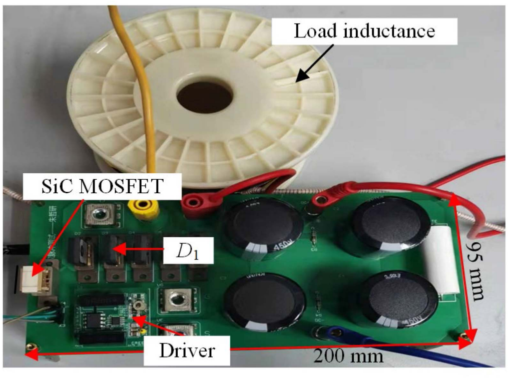


FIGURE 22. Voltage, temperature, and thermal resistance variations of DUTs. (a) Voltage variation. (b) Temperature variation.



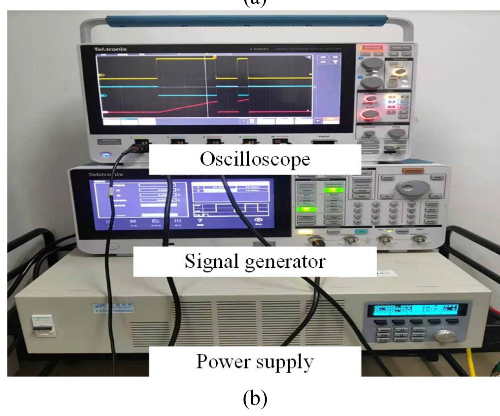


FIGURE 24. Double pulse test platform. (a) Test broad. (b) Measuring equipment.

determined by using the method mentioned in reference [29], and the result is shown in Fig. 21.

The voltage and temperature variations over time are shown in Fig. 14 for $I_d = 20$ A, heating time = 400 s, and cooling time = 200 s. Under the same external cooling system, the voltage and temperature of the PP SiC MOSFET device reach a steady state after being heated by about 200 s, whereas the TO device requires about 250 s. As shown in Fig. 22(a), the initial V_{ds} of the two devices is about 0.69 V, and the steady-state V_{ds} of the two devices are 1.04 V and 0.923 V, respectively. The V_{ds} variation of the PP device is 33.4% less than that of the TO device. In Fig. 22(b), the temperature variation of the PP device is also significantly smaller than that of the TO device, the difference of T_j and T_c between the two devices is around 30 °C.

From the steady state experimental results, the thermal resistance of the PP SiC MOSFET device can be calculated by (3). The thermal resistance of the TO-247-3 SiC MOSFET device can be calculated by (4).

$$R_{th} = \frac{T_j - T_c}{P_{loss}} \tag{4}$$

The thermal resistance of the PP and TO-247-3 SiC MOSFET device is shown in Fig. 23. When both SiC MOSFET devices operate, reaching a steady state, the thermal resistance of the TO-247-3 SiC MOSFET device is about 0.42 K/W,

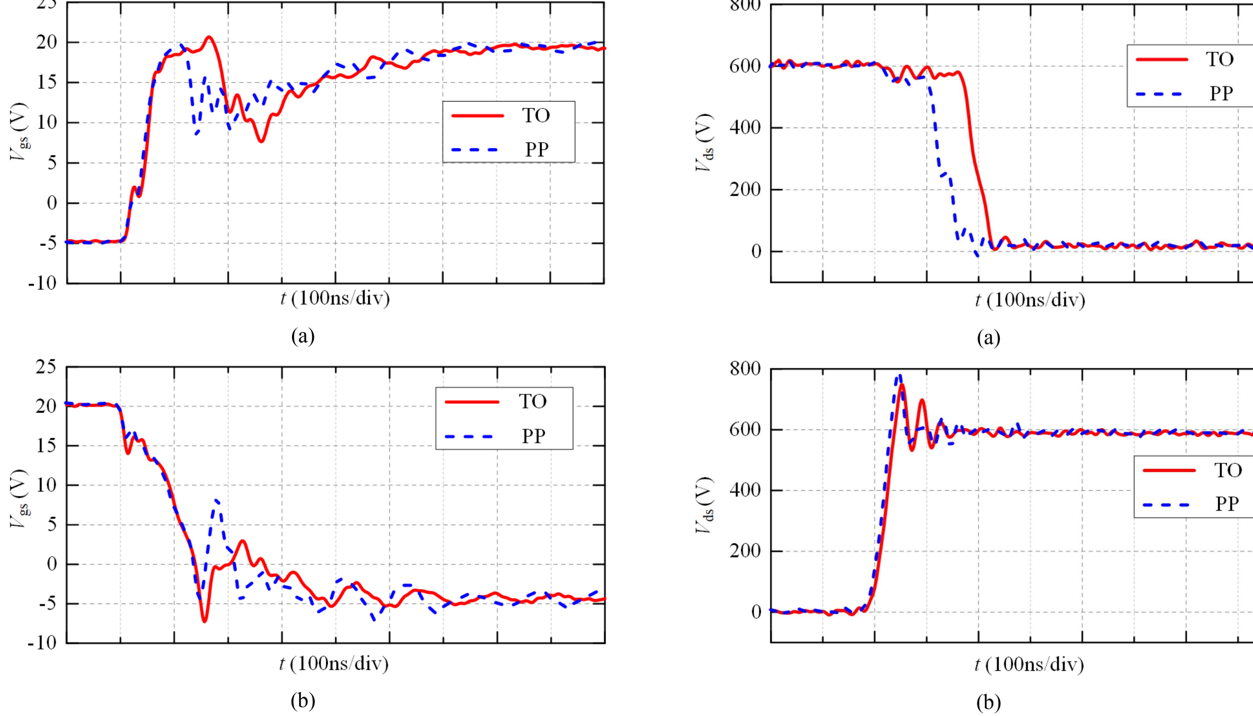


FIGURE 25. Experimental results of V_{gs} waveform. (a) Turn-on; (b) Turn-off.

FIGURE 26. Experimental results of V_{ds} waveform. (a) Turn-on; (b) Turn-off.

and the thermal resistance of the PP SiC MOSFET device is 0.22 K/W. Compared with the TO-247-3 SiC MOSFET device, the thermal resistance of the PP SiC MOSFET devices has been reduced by 47.4%, demonstrating the effectiveness of the proposed PP SiC MOSFET device for optimizing thermal performance.

B. SWITCHING CHARACTERISTIC TEST

To compare the switching characteristics of the proposed PP SiC MOSFET device and TO-247-3 SiC MOSFET device, an inductance clamping double pulse test platform is built, as shown in Fig. 24. As shown in Fig. 24(a), the area of the double pulse test platform is 95 mm × 200 mm, and the SiC MOSFET device and other components are concentrated on the DPT test platform, which minimizes the IC and RC values of the double pulse test platform.

The load inductance (L_{load}) is 550 μH. The bus voltage (V_{DC}) is set to 600 V provided by the power supply, with a parallel capacitance (C_{DC}). Diode D_1 maintains current when the device is turned off. Upon receiving the double pulse signal from the signal generator, the driver controls the devices to switch. Voltage and current probes are separately used to record the V_{gs}, V_{ds}, and I_d of the devices, with test waveforms displayed on the oscilloscope. The switching waveforms of the two devices under test conditions of $V_{ds} = 600$ V, $I_d = 55$ A are shown in Figs. 25–27.

The overshoot observed during the switching process of two SiC MOSFET devices is approximately equivalent. However, during the turn-on process, the rise time V_{gs} of the PP SiC MOSFET is reduced by about 38 ns, the drop time V_{ds} of

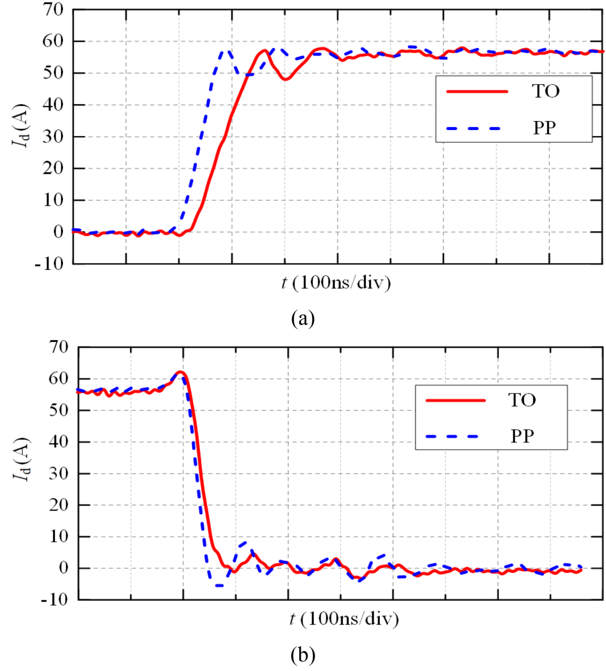


FIGURE 27. Experimental results of I_d waveform. (a) Turn-on; (b) Turn-off.

the PP SiC MOSFET device is reduced by about 38 ns, and the rise time I_d of the PP SiC MOSFET is reduced by about 34 ns. Similarly, during the turn-off process, the drop time V_{gs} of the PP SiC MOSFET is reduced by about 10 ns, and there is a reduction in the rise time of V_{ds} and the drop time of I_d

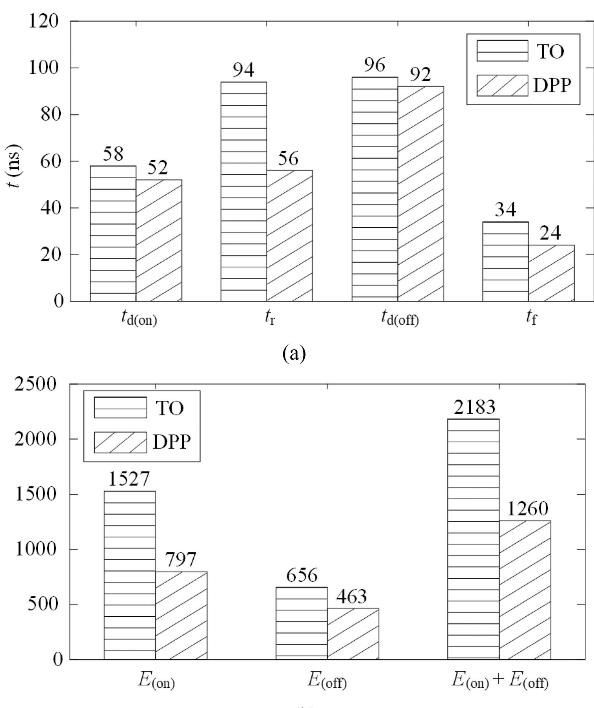


FIGURE 28. Comparisons of switching characteristic parameters of two devices. (a) switching time; (b) switching loss.

by approximately 10 ns and 28 ns of the PP SiC MOSFET device, respectively.

According to IEC 60747-8-2010, "Semiconductor devices-Discrete devices-Part 8: Field-effect transistors", the comparison of switching losses, turn-on, and turn-off time of the two devices is shown in Fig. 28. As shown in Fig. 28(a), compared with the TO-247-3 device, the PP SiC MOSFET device has lower switching delay and faster switching speed. As shown in Fig. 28(b), compared with the TO-247-3 device, the PP SiC MOSFET device can reduce the on-loss E_{on} and off-loss E_{off} by 47.8% and 29.4%, respectively, resulting in a total switching loss reduction by 42.3% under the test conditions of $V_{ds} = 600$ V, $I_d = 55$ A.

V. CONCLUSION

This paper proposes a DSC PP SiC MOSFET device using a copper foam gate pin and an embedded fixture. The electrical and thermal performances, and parasitic inductance of the proposed PP SiC MOSFET device are simulated. The steady-state electrical and thermal test, and switching characteristic test are used to verify the optimization of the proposed PP package compare to the TO package for the SiC MOSFET device. Compared with the TO-247-3 device, the proposed PP SiC MOSFET device with a double-sided cooling structure can reduce the steady-state V_{ds} variation by 33.4% and the T_j by 30 °C under the same operating conditions. The proposed package can also effectively reduce the parasitic inductance of the power circuit by about 44%, reducing the switching loss by about 42.3% under the same conditions. The proposed DSC packaging approach may be suitable for a high-voltage multi-chip SiC MOSFET device, which will guide the future design of higher-voltage SiC MOSFET modules. By optimizing the driving circuit of the proposed PP SiC MOSFET device, it is possible to compare its switching characteristic optimization with TO-247-4 SiC MOSFET devices in the future.

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