IEEE Open Journal of
Power Electronics

Received 24 July 2024; accepted 9 August 2024. Date of publication 16 August 2024;
date of current version 12 September 2024. The review of this article was arranged by Associate Editor Lijun Hang.

Digital Object Identifier 10.1109/OJPEL.2024.3445313

Modelling and Optimal Design of a Multifunctional Single-Stage Buck-Boost Differential Inverter

RAJESH RAJAMONY[1], SHENG WANG [2,3] (Member, IEEE), AND WENLONG MING [2,3] (Member, IEEE)

[1]Jaguar Land Rover, CV4 7AL Coventry, U.K.
[2]School of Engineering, Cardiff University, CF24 3AA Cardiff, U.K.
[3]Compound Semiconductor Applications Catapult, NP10 8BE Newport, U.K.

CORRESPONDING AUTHOR: WENLONG MING (e-mail: wenlongming@ieee.org).

This work was supported in part by Engineering and Physical Sciences Research Council EPSRC, U.K., under Grant EP/N509449/1, and in part by Innovate U.K., under Grant 511068.

ABSTRACT In this paper, a single-stage buck-boost differential inverter is optimally designed for applications with varying input DC voltage (e.g., photovoltaics and fuel cell systems). The designed inverter has multiple functionalities, including power decoupling and AC output filtering, and it can operate with a wide DC voltage range without adding extra power conversion stages or filters. Hence, it is naturally compact and highly efficient. To fully exploit its benefits, the proposed inverter operating principle and mathematical model were first developed to form the foundation of an optimal design. The criteria for selecting the inverter's key components have been presented. This ensures that the developed inverter meets the aforementioned functional requirements without being overly sized. A digital design procedure based on artificial neural networks is followed for further multiple objective optimization, targeting high efficiency, high power density and low cost. A 1.8kW prototype of the inverter was fabricated through the digital design. The inverter's operating functionality with varying DC voltage, power decoupling, and filtering was demonstrated by both simulation studies and experimental tests on the prototype. The accuracy of the optimal design was also validated.

INDEX TERMS Single-stage differential inverter, power decoupling, optimal design, improvement of efficiency, power density and cost.

I. INTRODUCTION

The DC link of single-phase inverters consists of both constant and second-order ripple power [1]. This ripple power creates extra power losses and deficient performance in operating at low-power regions [2]. Differential inverters can eliminate such second-order ripple power. Their inherent output capacitor is used for power decoupling; hence, additional components such as switch, inductor, and capacitor can be avoided [3]. This will also simplify the control as fewer components are used [4]. Power decoupling methods are also developed to minimize the DC capacitors, which sacrifices the inverter's overall efficiency and power density [5].

Existing differential inverters can be classified into the buck, boost, or buck-boost types combined by two identical DC-DC converters [6]. In [7], a buck-type differential inverter was used to reduce the second-order ripple from the DC-link by more than seven times, using a decoupling control method. The same inverter was used for grid-connected photovoltaic (PV) systems by applying a common-mode conducting loop to minimize the second-order pulsating power without using extra active components [8]. In [9], a common-mode control was further presented to reduce the impact caused by the mismatch of the inverters' decoupling capacitors. In [10], a waveform control-based ripple mitigation method was introduced for a differential boost inverter to improve the stability of a fuel-cell system. In [11] and [12], the waveform control method was improved using rule-based and feedback current controllers for battery storage systems. The buck and boost type differential inverters are a good option for applications where the DC-link voltage is higher and lower than the output

voltage. For a residential PV application, the input voltage could vary between higher or lower than the DC-link voltage. Therefore, a DC-DC converter is needed between the source and the DC-link to step up or step down the DC-link voltage. Such DC-DC converter requires a high current inductor and high voltage switches, which increases the additional losses, volume, and design costs. Meanwhile, an additional control is required to drive the switches. Therefore, a high-efficiency and high-power density single-stage buck-boost differential inverter is required. In [13], an energy-based power decoupling control method was introduced for a buck-boost inverter to mitigate the second-order low-frequency ripple in the input DC current. Consequently, the required capacitance at the DC side is significantly reduced, allowing small film capacitors to replace bulky electrolytic capacitors. However, the efficiency and power density of differential inverters have not been investigated in detail.

The differential inverters are suitable for applications where the DC-link voltage operates at constant values. For applications with varying DC input voltages lower than the inverter AC voltage (e.g., PV and fuel cell systems), a DC-DC converter is typically required to form a two-stage inverter thus to step up and regulate a DC-link voltage higher than AC [14]. Using extra DC-DC converters complicates the topology, resulting in more power losses, volume, and costs.

An effective approach is to use single-stage inverters, which avoids extra DC-DC converters. In [15], a single-stage buck-boost inverter using an LC resonant tank was proposed mainly for improving efficiency by soft switching. In [16], another single-stage inverter was introduced to reduce PV applications' switching and conduction losses. Reference [17] also focuses on using single-stage buck-boost inverters for PV systems but with a detailed discussion on improving the lifetime by eliminating common-mode leakage current. In [14] and [18], an alternative buck-boost inverter was introduced to eliminate the common-mode leakage current and improve the power quality of the AC output during unbalanced input voltages.

The above research focuses on realizing the different functions of single-stage buck-boost inverters, while an optimal design of a multifunctional inverter with a wide input voltage range and power decoupling and filtering features has yet to be presented. To close the gap, this paper presents a single-stage buck-boost differential inverter that utilizes its capacitors for power decoupling and AC filtering. Therefore, no extra DC-DC converters and L-C filtering circuits are needed, resulting in improved efficiency and power density. On this basis, criteria for optimal component selection are provided. An artificial neural network (ANN)-based digital design was adopted to target high efficiency, high power density and cost reduction, considering the prototyping of a 1.8 kW bespoke inverter, which was then used in terms to verify all the functionalities of the inverter and the accuracy of the design.

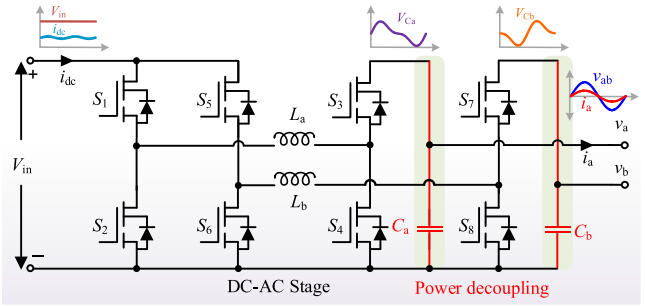

FIGURE 1. Proposed single-stage buck-boost inverter.

II. INVERTER TOPOLOGY AND OPERATION

Fig. 1 shows the configuration of the proposed inverter. The topology is formulated by integrating two identical non-inverting buck-boost DC-DC converters. It consists of two inductors (L_a, L_b), two capacitors (C_a, C_b), and eight switches (S_1–S_8). Switches S_1, S_2, S_5 and S_6 are for buck operation; S_3, S_4, S_7, and S_8 are for boost operation. Although the inverter has eight switches, four can be operated at low voltage stress. The denotation is the input DC voltage (V_{in}) and current (i_{dc}), output AC voltage (v_{ab}) and current (i_a). The voltage v_{ab} is generated by the subtraction of two capacitors' voltages ($V_{Ca} - V_{Cb}$).

Fig. 2 shows the key waveform of the buck-boost inverter. The inverter operates to generate two sinusoidal capacitors with the same DC offset (see V_{Ca} and V_{Cb} in Fig. 2), represented as:

$$V_{Ca} = \frac{V_{ab}}{2}(1 + \sin \omega t) + v_{comp} \tag{1}$$

$$V_{Cb} = \frac{V_{ab}}{2}(1 + \sin(\omega t + \pi)) + v_{comp} \tag{2}$$

where V_{ab} is the amplitude of the output voltage and v_{comp} is the second-order ripple compensated voltage.

In (1) and (2), the term $1 + \sin \omega t$ is used to generate offset voltage, which helps maintain positive voltage across the capacitors. The peak value of the capacitor voltage is equal to the peak value of the inverter output voltage. Also, the v_{comp} is the second-order ripple compensated voltage, which is not added to the peak voltage (see Figs. 2 and 13). Therefore, no voltage stress was created in the design due to the term $1 + \sin \omega t$. From (1) and (2), the output voltage of the inverter can be written as,

$$v_{ab} = V_{Ca} - V_{Cb}$$

$$v_{ab} = \frac{V_{ab}}{2}(1 + \sin \omega t) + v_{comp} - \frac{V_{ab}}{2}(1 + \sin(\omega t + \pi)) - v_{comp}$$

$$v_{ab} = \frac{V_{ab}}{2}(\sin \omega t - \sin(\omega t + \pi))$$

$$v_{ab} = V_{ab} \sin \omega t \tag{3}$$

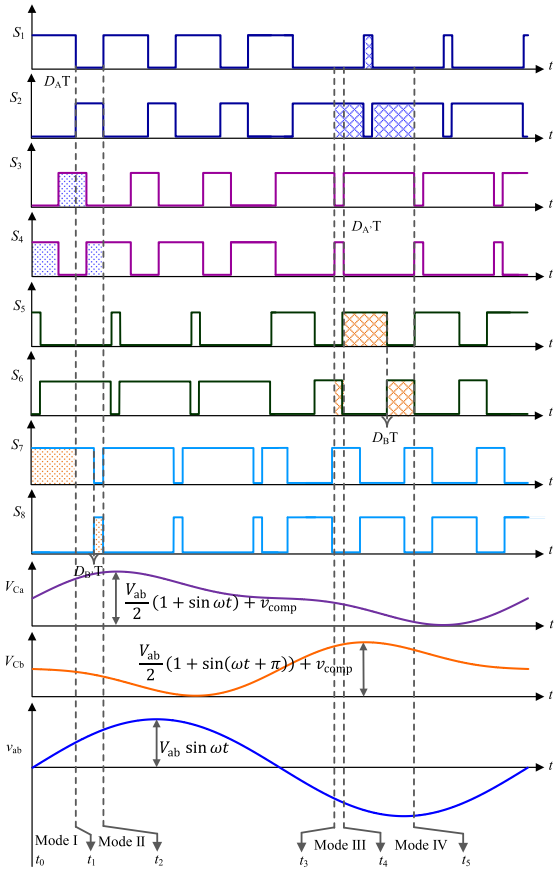

FIGURE 2. Key waveforms of inverter operating.

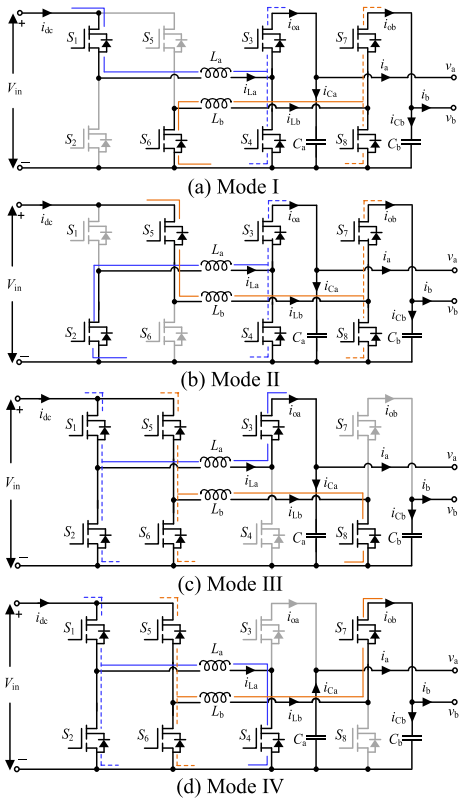

FIGURE 3. Operating modes.

It can be seen that the output voltage is purely sinusoidal due to the differential feature, and the second-order ripple components will be captured in the capacitors.

The proposed inverter has four operation modes, as shown in Fig. 3, which corresponds to the duration and switch patterns in Fig. 2. The modulation signals generation logics of $S_1 - S_8$ can be realized from the four modes of the inverter. In each leg, upper and lower switches are operated as complementary. When S_1 and S_4 are in ON states, the current through the inductor L_a increases linearly. When S_2 and S_3 are in ON states, the inductor current is reduced, which flows through the input of the inverter. Similarly, the switches S_5, S_6, S_7 and S_8 are operated. The modulation of S_1, S_2, S_3 and S_4 occurs based on a sinusoidal signal with a required offset. The modulation of S_5, S_6, S_7 and S_8 8 occurs based on a 180-degree phase-shifted sinusoidal signal with a required offset.

In Mode I $[t_0 - t_1]$: switch S_1 is ON, the inductor L_a current increases rapidly, and the current flows through S_3 and S_4 which switches according to the duty cycle $(D_{A'})$ for boost operation. The change of inductor current ΔL_a in one switching cycle is balanced and represented as:

$$\Delta I_{La} = \frac{V_{in}}{L_a} D_{A'} + \left(\frac{V_{in} - V_{Ca}}{L_a}\right)(1 - D_{A'}) = 0 \qquad (4)$$

In Mode II $[t_1 - t_2]$, switch S_3 is ON, the inductor L_a current flows through the AC side. Then, based on the duty cycle (D_A) of S_1 and S_2, the buck operation can be achieved. The change of inductor ΔI_{La} current is then as follows:

$$\Delta I_{La} = \left(\frac{V_{in} - V_{Ca}}{L_a}\right) D_A - \frac{V_{Ca}}{L_a}(1 - D_A) = 0 \qquad (5)$$

In Mode III $[t_3 - t_4]$, switch S_5 is ON, the inductor L_b current increases rapidly and the current flows through S_7 and S_8 according to their duty cycle $(D_{B'})$ for boost operation. The change of current ΔI_{Lb} is given by:

$$\Delta I_{Lb} = \frac{V_{in}}{L_b} D_{B'} + \left(\frac{V_{in} - V_{Cb}}{L_b}\right)(1 - D_{B'}) = 0 \qquad (6)$$

In Mode VI $[t_4 - t_5]$, switch S_7 is ON, the inductor L_b current flows through the AC side. Then, based on the duty cycle (D_B) of switches S_5 and S_6, the buck operation can be achieved. The change of ΔI_{Lb} in this mode is,

$$\Delta I_{Lb} = \left(\frac{V_{in} - V_{Cb}}{L_b}\right) D_B - \frac{V_{Cb}}{L_b}(1 - D_B) = 0 \qquad (7)$$

By operating with four modes, the inverter output voltage v_{ab} is calculated by combining (4) to (7), as,

$$v_{ab} = \frac{D_A D_B V_{in}}{(1 - D_{A'})(1 - D_{B'})} \qquad (8)$$

III. MODELLING OF OPTIMAL DESIGN

In order to optimally design the inverter, detailed power loss, volume, and cost models of the differential buck-boost inverter will need to be developed based on the required functions. These models are the foundations for determining the efficiency, power density, and specific cost of a designed inverter. The input design variables, including switching frequency f_{sw}, inductor ripple Δi_L, power switch's area A_{sw} and junction temperature ΔT_j are used to calculate the power loss and volume. Then, the component costs are modelled based on the created power loss and volume models.

A. POWER GAN FETS

GaN FETs are ideal switches for designing high-efficiency and high-power-density inverters [19]. Compared to Si devices, GaN FETs have better switching and conduction performance over a wide range of temperatures than Si-based devices. For instance, they have faster switching speeds, lower switching losses, higher breakdown voltages and higher operating temperatures. In single-phase inverters, the GaN FETs improve performance over Si under wide load, temperature and switching frequency conditions. Using these advantages, the cost of other components, such as inductors, capacitors, and heat sinks, can be reduced, significantly reducing the total component cost of the inverter.

The power losses of GaN FETs are generated by their on-state resistance $R_{DS,on}$, output capacitance C_{oss} and thermal junction-to-case resistance $R_{\theta JC}$. These variables are scaled by their datasheet values to the area of the switch. The switching losses of the inverter are the sum of the switching losses of all switches [20]. Those of the buck side switches S_1, S_2, S_5 and S_6 are,

$$P_{sw,\ buck} = f_{sw} \times \left\{ \left(I_a \sin(\omega t) - \frac{\triangle\, i_{L_a}}{2} + i_{comp} \right) (V_{in} t_{on} + V_{SD} t_{off}) + \left(I_a \sin(\omega t) + i_{comp} + \frac{\triangle\, i_{L_a}}{2} \right) (V_{in} t_{off} + V_{SD} t_{on}) \right\} \quad (9)$$

Those of the boost side switches S_3, S_4, S_7 and S_8 are,

$$P_{sw,\ boost} = f_{sw} \times \left\{ \left(I_a \sin(\omega t) + i_{comp} + \frac{\triangle\, i_{L_a}}{2} \right) (V_{Ca} t_{on} + V_{SD} t_{off}) + \left(I_a \sin(\omega t) + i_{comp} - \frac{\triangle\, i_{L_a}}{2} \right) (V_{Ca} t_{off} + V_{SD} t_{on}) \right\} \quad (10)$$

where i_{comp} is the second-order current component. t_{on} and t_{off} are the ON and OFF time of the switches. The total switching losses $P_{tot,sw}$ of the inverter is the sum of $P_{sw,\ buck}$ and $P_{sw,\ boost}$.

The conduction loss depends on the RMS current flowing through the switch, which further relates to I_a and I_b, $R_{DS,on}$ and $\triangle\, T_j$. It varies according to the switches' duty cycle. The total conduction loss $P_{tot,cond}$ can is derived as,

$$P_{tot,cond} = 2 \left(\frac{R^*_{DS,on} A^*_{sw}}{A_{sw}} \right) (1 + \triangle\, T_j) \times \left\{ \left(I_a^2 \sin^2(\omega t) + i_{comp}^2 + \frac{\triangle\, i_{L_a}^2}{12} \right) + \left(I_a^2 \sin^2(\omega t + \pi) + i_{comp}^2 + \frac{\triangle\, i_{L_b}^2}{12} \right) \right\} \quad (11)$$

The power losses of the C_{oss} ($P_{tot,C_{oss}}$) is a function of the input voltage and switching frequency,

$$P_{tot,C_{oss}} = \left(\frac{C^*_{oss} A_{sw}}{A^*_{sw}} \right) (2V_{in}^2 + V_{Ca}^2 + V_{Cb}^2)\, f_{sw} \quad (12)$$

The reverse recovery losses occur during the body diode transitions from on-state to off-state. For cascode GaN FETs, a small number of reverse recovery losses ($P_{tot,rr}$) occurs in the lower side switches, given as,

$$P_{tot,rr} = \left(\frac{Q^*_{rr} A_{sw}}{A^*_{sw}} \right) (2V_{in} + V_{Ca} + V_{Cb})\, f_{sw} \quad (13)$$

The gate losses depend on f_{sw}, the gate-source voltage V_{GS} and the gate charge Q_g. The total gate loss of all switches $P_{tot,g}$ is calculated as,

$$P_{tot,g} = 8 \left(\frac{Q^*_g A_{sw}}{A^*_{sw}} \right) V_{GS} f_{sw} \quad (14)$$

In cascode GaN FETs, the body diode of the lower side switches incurred by the conduction loss during the reverse recovery time t_{rr} [20]. The total power loss of the body diodes ($P_{tot,bd}$) can be written as,

$$P_{tot,bd} = 4V_{SD} f_{sw} t_{rr} \left(I_{out} (\sin(\omega t) + \sin(\omega t + \pi)) + 2 i_{comp} \right) \quad (15)$$

The volume of the switches is calculated as,

$$vol_{sw} = 8 h_{sw} A_{sw} \quad (16)$$

where h_{sw} is the height of the switch package.

The total cost of the switches is calculated [21] as,

$$\Sigma_{switch} = n_{switch} \left(a_1 + b_1 I_{sw,\ rated} \right) \quad (17)$$

where n_{switch} is the total number of switches, a_1 is the cost per switch £, b_1 is the cost per rated ampere (£/A) and $I_{sw,\ rated}$ is the rated current of the switch (A).

B. INDUCTORS

The inductor power losses consist of the core losses, the AC and DC resistance losses [22],

$$P_{ind} = a_{L1} f_{sw}^{\alpha} \Delta i_L^{\beta} + a_{L2} f_{sw} \Delta i_L^{\gamma} + a_{L3} I_a^2 \Delta i_L^{\lambda} \quad (18)$$

where a_{L1}, α, and β are the Steinmetz coefficients; a_{L2} and a_{L3} are the constants, which are used to approximate the values of DC winding resistance; γ and λ are the real values, which are used to reduce the non-linearity.

The approximated inductor volume is calculated as,

$$vol_{\text{ind}} = a_{\text{L4}} L \left(I_{\text{peak,a}}^2 + I_{\text{peak,b}}^2\right) + a_{\text{L5}} L \left(I_{\text{peak,a}} + I_{\text{peak,b}}\right) + a_{\text{L6}} \left(I_{\text{peak,a}} + I_{\text{peak,b}}\right) \tag{19}$$

$$I_{\text{peak,a}} = I_{\text{out}} \sin(\omega t) + i_{\text{comp}} + \frac{\Delta i_{\text{L}_\text{a}}}{2} \tag{20}$$

$$I_{\text{peak,b}} = I_{\text{out}} \sin(\omega t + \pi) + i_{\text{comp}} + \frac{\Delta i_{\text{L}_\text{b}}}{2} \tag{21}$$

where a_{L4}, a_{L5}, and a_{L6} are the polynomial coefficients and are positive values. L is the inductor value ($L = L_{\text{a}} = L_{\text{b}}$). $I_{\text{peak,a}}$ and $I_{\text{peak,b}}$ are the peak currents of the inductors.

The total cost of the inductors is calculated [21] as,

$$\Sigma_{\text{inductor}} = a_2 + b_2 I_{\text{ind, rated}} \tag{22}$$

where a_2 is the constant cost £, b_2 is the cost per volume (£/cm^3) and $I_{\text{ind, rated}}$ is the rated current of the inductor.

C. POWER DECOUPLING CAPACITORS

The power loss of the inverter's capacitor is calculated as,

$$P_{\text{cap}} = \frac{I_{\text{RMS,C}}^2 \tan\delta}{2\pi f_{2\omega} C} \tag{23}$$

where $I_{\text{RMS,C}}$ is the RMS current flow through the capacitor, $\tan\delta$ is the loss factor, $f_{2\omega}$ is the frequency of the second-order ripple power and C is the value of the capacitance.

In a practical design, the volume of capacitors varies from different manufacturers. An approximated model is thus used. The total box volume of the capacitors vol_{cap} are calculated as,

$$vol_{\text{cap}} = a_{\text{C1}} C \left(V_{\text{C}_\text{a}}^2 + V_{\text{C}_\text{b}}^2\right) + a_{\text{C2}} C \left(V_{\text{C}_\text{a}} + V_{\text{C}_\text{b}}\right) + a_{\text{C3}} \left(V_{\text{C}_\text{a}} + V_{\text{C}_\text{b}}\right) \tag{24}$$

where a_{C1}, a_{C2}, and a_{C3} are the polynomial coefficients of the capacitor which must be positive. C is the output capacitance ($C = C_{\text{a}} = C_{\text{b}}$). The output capacitor selection is the biggest challenge, which has a trade-off between the second-order ripple, power loss and volume.

The total cost of the decoupling capacitors is calculated [21] as,

$$\Sigma_{\text{capacitor}} = a_3 + b_3 V_{\text{rated}} + c_3 C_{\text{rated}} \tag{25}$$

where a_3 is the constant cost £, b_3 is the cost per rated voltage (£/V), c_3 is the cost per capacitance (£/μF) and C_{rated} is the rated value of capacitance (μF).

D. HEAT SINKS

The volume of the heat sinks is calculated as [23],

$$vol_{\text{heat sink}} = \frac{V_{\theta\text{SA}}}{P_{\text{D}}} \left(\Delta T_{\text{j}} - P_{\text{D}} \left(R_{\theta\text{JC}} + R_{\theta\text{CS}}\right)\right) \tag{26}$$

where $V_{\theta\text{SA}}$ is the volumetric resistance, P_{D} is the total power dissipation of switches, ΔT_{j} is the temperature difference between the junction and the ambient, $R_{\theta\text{JC}}$ is the switches' junction-to-case thermal resistance, and $R_{\theta\text{CS}}$ is the switches' case-to-mounting-surface thermal resistance. The values of $R_{\theta\text{JC}}$ and $R_{\theta\text{CS}}$ are obtained from the manufacturer's datasheet.

The total cost of the heat sinks is calculated [21] as,

$$\Sigma_{\text{heat sink}} = a_4 + b_4 vol_{\text{heat sink}} \tag{27}$$

where a_4 is the constant cost (£), b_4 is the cost per volume (£/cm^3) and $vol_{\text{heat sink}}$ is the volume of the heat sink.

IV. OPTIMAL SELECTION OF COMPONENTS

The optimal selection of key components are critical for optimal design. It is important that the selected GaN FETs can withstand maximum voltage and current stress while not being oversized. Similarly, proper sizing of inductors and capacitors should be done according to the requirement for limiting second-order ripple components.

A. VOLTAGE AND CURRENT STRESS OF GAN FETS

The evaluation of GaN FETs' voltage and current stress is used to select their optimal power rating. The voltage and current stress are calculated individually for switches operating in the buck and boost modes. The maximum voltage stress of S_1, S_2 S_5, S_6 ($V_{\text{sw,max,buck}}$) depends on the input voltage, and the maximum duty cycles $D_{\text{A,max}}$ and $D_{\text{B,max}}$ for buck operation as,

$$V_{\text{sw,max,buck}} = \begin{cases} V_{\text{in}} D_{\text{A,max}} & \in S_1, S_2 \\ V_{\text{in}} D_{\text{B,max}} & \in S_5, S_6 \end{cases} \tag{28}$$

The maximum voltage stress of S_3, S_4, S_7, S_8 in boost mode ($V_{\text{sw,max,boost}}$) depends on both the voltage of output capacitors and maximum duty cycles ($D_{\text{A}',\text{max}}$ and $D_{\text{B}',\text{max}}$) for boost operation as,

$$V_{\text{sw,max,boost}} = \begin{cases} D_{\text{A}',\text{max}} \left(\frac{V_{\text{ab,max}}}{2} (1 + \sin\omega t) + v_{\text{comp}}\right) & \in S_3, S_4 \\ D_{\text{B}',\text{max}} \left(\frac{V_{\text{ab,max}}}{2} (1 + \sin(\omega t + \pi)) + v_{\text{comp}}\right) & \in S_7, S_8 \end{cases} \tag{29}$$

where $V_{\text{ab,max}}$ is the maximum peak voltage. It is found that the maximum voltage stress is obtained when the corresponding duty cycles reach their peak values. However, the maximum voltage stress of S_1, S_2 S_5, S_6 are half of that of S_3, S_4 S_7, S_8.

The current stress depends on the maximum switching current flowing through the switches which differs between the buck and boost modes. The maximum switching currents of the buck ($I_{\text{sw,max, buck}}$) and boost ($I_{\text{sw,max,boost}}$) modes are calculated as,

$$I_{\text{sw,max, buck}} = \begin{cases} \frac{V_{\text{Ca}}(1-D_{\text{A}})}{2 f_{\text{sw}} L_{\text{a}}} + I_{\text{a}} \\ \frac{V_{\text{Cb}}(1-D_{\text{B}})}{2 f_{\text{sw}} L_{\text{b}}} + I_{\text{b}} \end{cases} \tag{30}$$

$$I_{\text{sw,max, boost}} = \begin{cases} \frac{V_{\text{in}} D_{\text{A}'}}{2 f_{\text{sw}} L_{\text{a}}} + \frac{V_{\text{Ca}} I_{\text{a}}}{V_{\text{in}}} \\ \frac{V_{\text{in}} D_{\text{B}'}}{2 f_{\text{sw}} L_{\text{b}}} + \frac{V_{\text{Cb}} I_{\text{b}}}{V_{\text{in}}} \end{cases} \tag{31}$$

where I_a and I_b are the same output currents but measured at the phase line and neutral line. It can be seen that the maximum switching currents depend on the maximum inductor ripple current and the output current.

The voltage and current rating of the GaN FETs can then be selected to withstand the maximum voltage and current stress.

B. INDUCTOR SELECTION

The inductors should be selected to handle the dc ripple current and produce pure output currents. However, a lower inductor value helps to reduce the design size. This trade-off should be optimized during the design.

In buck mode, the selected inductor should satisfy,

$$L_a > \frac{D_A\,(V_{in} - V_{Ca})}{0.25 f_{sw} I_a} \tag{32}$$

$$L_b > \frac{D_B\,(V_{in} - V_{Cb})}{0.25 f_{sw} I_b} \tag{33}$$

In boost mode, the inductor should satisfy,

$$L_a > \frac{(1 - D_{A'})^2\,(V_{Ca} - V_{in})}{0.25 f_{sw} I_a} \tag{34}$$

$$L_b > \frac{(1 - D_{B'})^2\,(V_{Cb} - V_{in})}{0.25 f_{sw} I_b} \tag{35}$$

For the given topology, the inductor current ripple is allowed between 20% to 35% of the maximum output current [19]. The current flow through the inductor contains a switching ripple due to the switches ON and OFF. This ripple current can be reduced by increasing the value of the inductor. However, the preferred solution of the inductor is a lower value and smaller size. To decrease the inductance value, the switching frequency needs to be optimized accordingly. Based on these conditions, the inductor value is selected as 440 μH.

C. CAPACITOR SELECTION

The output capacitor selection is one of the challenges, which requires a trade-off to be made between the second-order ripple, power loss and volume. The output capacitor needs to handle the second-order ripple components diverted from the input DC side of the inverter.

In buck mode, the required capacitor is calculated as,

$$C_a = \frac{0.5(xI_a)^2 L_a}{D_A V_{in} \Delta V_{Ca}} \tag{36}$$

$$C_b = \frac{0.5(xI_b)^2 L_b}{D_B V_{in} \Delta V_{Cb}} \tag{37}$$

In boost mode, the required capacitor is calculated as,

$$C_a = \frac{I_a\,(V_{Ca} - V_{in})}{2 f_{sw} V_{Ca} \Delta V_{Ca}} \tag{38}$$

$$C_b = \frac{I_b\,(V_{Cb} - V_{in})}{2 f_{sw} V_{Cb} \Delta V_{Cb}} \tag{39}$$

where x is the coefficient (0.2 to 0.4) that determines the amount of ripple presented in the output current. Based on these conditions, the capacitor value is selected as 80μF. The 80μF capacitor is selected to handle the output and second-order ripple compensation voltage. This value is obtained based on the analysis of the trade-off between the second-order ripple decoupling capacitance and the total power losses and power density of the inverter [19]. Otherwise, a large DC-link capacitor will be required to reduce the effect of second-order ripple, which is not required in the proposed inverter. MKP1848C series polypropylene film capacitors from Vishay BC Components were used, which are smaller than electrolytic capacitors and the overall power density of the inverter can be improved.

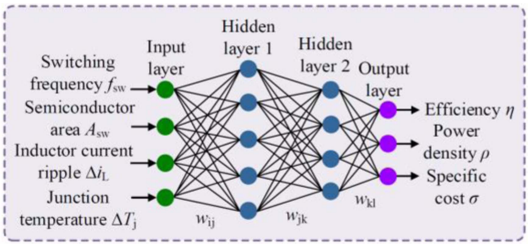

FIGURE 4. Structure of the ANN for the proposed design approach.

V. OPTIMAL DESIGN AND TEST VALIDATION

A. ANN BASED OPTIMAL DESIGN

Feedforward ANN is used to predict the performance of the inverter design. The structure of ANN that is used for the proposed design approach is given in Fig. 4. It consists of three layers: the input layer, the hidden layer, and the output layer. The layers are interconnected through artificial neurons, and the neuron is called a node or unit. The number of input and output nodes is selected based on the application. The design approach is developed using the mathematical models from the previous section. Initially, the datasets are generated using mathematical models to train the network. The complications are that using fewer hidden units will reduce the learning ability of the required function. However, this will significantly reduce the network's training time. Therefore, proper validation is required to ensure network accuracy. The connections between nodes are associated with a weight, which sets the threshold value of each node. The weights between the input and hidden layer are represented as w_{ij}, the weights between the hidden layers are represented as w_{jk}, and the weights between the hidden and the output layers are represented as w_{kl}. The initial value of the weight is selected randomly. It will then be changed during the training to reach the correct target. The switching frequency, area of the switch, inductor current ripple, and change of temperature are considered as the inputs. Efficiency and power density are considered targets. The switching frequency, area of the switch, inductor current ripple, and change of temperature are considered as inputs of the ANN. Efficiency, power density, and specific costs are considered targets. The detail design principle is referred to in [24].

TABLE 1 Design Constraints of the Inverter

Design variable	Min. value	Max. value
Switching frequency f_{sw}	10 kHz	200 kHz
Current ripple Δi_L	$0.1I_{out,max}$	$0.45I_{out,max}$
Switch area A_{sw}	$0.94A^*_{sw}$	$1.07A^*_{sw}$
Change in temperature ΔT_j	1°C	25°C

TABLE 2 Cost Coefficients of the Components

Switch		Inductor		Capacitor			Heat sink	
a_1	b_1	a_2	b_2	a_3	b_3	c_3	a_4	b_4
4.5	3.9	1.2	0.5	−7.6	0.5	0.0032	0.056	0.045

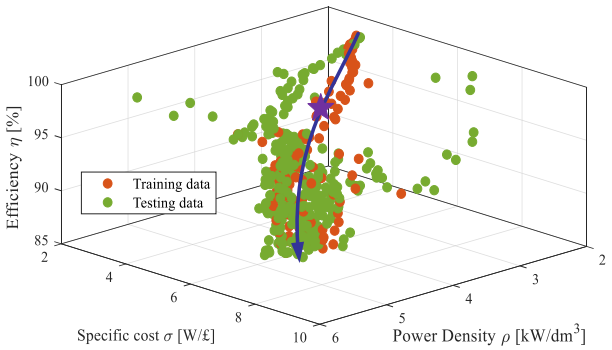

FIGURE 5. Pareto-front (efficiency η, power density ρ, and cost σ).

The proposed inverter was designed using an ANN-based multiple-objective optimization approach similar to [24], but with the inverter cost added as a new performance parameter. The inverter's power loss, volume and cost models developed in Sections III and IV is first programmed in MATLAB/Simulink to generate 2000 design data for training, testing and validating the ANN network, and accordingly obtaining 2000 data of the efficiency, power density and cost.

The inductor value can be optimized by changing the switching frequency and current ripple. For that, the switching frequency can be varied from 10 kHz to 200 kHz and the current ripple 10% to 45% of output current. The capacitor value can be optimized by changing the switching frequency and voltage ripple. The voltage ripple can be varied from 20% to 40% of the capacitor voltage. The minimum and maximum values of the design parameters are in Table 1. The coefficients of components' cost models are in Table 2. The design parameters are applied to the network and the corresponding performance parameters (i.e., efficiency η, power density ρ and cost σ) are mapped as the Pareto-front (purple curve) in a 3D space, which provides the best trade-off between the performance parameters, see Fig. 5.

In this paper, the final design is selected for PV applications. The outcome of the design is compared in both simulation and experimental, which is explained in Sections V-D and V-E. Any point located on the Pareto-front

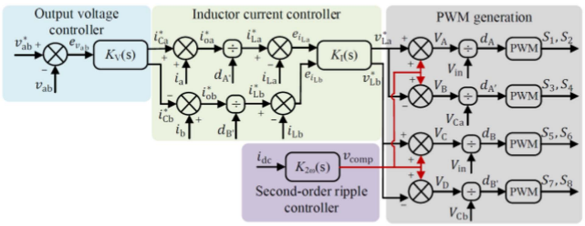

FIGURE 6. Control diagram of the buck-boost inverter.

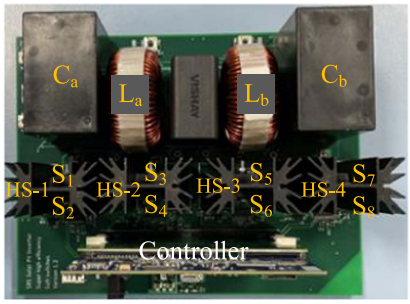

FIGURE 7. Prototype of the buck-boost inverter (1.8 kW).

provides the best combination of three performance parameters. To validate the proposed inverter, one design is selected (located at the star), targeting $\eta = 98.3\%$, $\rho = 4.36\,\text{kW/dm}^3$ and $\sigma = 6.98\ \text{W/£}$.

B. CONTROL STRATEGY OF THE PROPOSED INVERTER

Fig. 6 shows the control diagram of the buck-boost inverter. The controllers are classified into the voltage controller $K_V(s)$, inductor current controller $K_I(s)$, and second-order ripple controller $K_{2\omega}(s)$. PR controller is used to design the controllers. The detailed design of the PR controller is presented [1] and [8].

The output voltage controller is used to regulate the voltage across the load. The target frequency is selected to track the fundament frequency and eliminate the odd and even harmonics. The current controller is used to control the output current and the inductor current. The target frequency of the current controller is selected to track the fundament frequency and eliminate the odd harmonics. The second-order ripple controller acts as a decoupling controller, which controls the second-order ripple in the DC-link current. The ripple controller is used to reduce the second-order ripple and the residuals of the second-order ripple on the DC-link current. Therefore, the target frequency of the decoupling controller is selected to eliminate the even harmonics.

C. VERIFICATION USING A PROTOTYPED INVERTER

A 1.8 kW prototype of the proposed inverter was fabricated according to the optimal design conducted in Section V-A (see Fig. 7). To achieve the targeted performance parameters, the values of the inductor (L_a, L_b) and capacitor (C_a, C_b) are 440 μH and 80 μF, with switching frequency to be 50 kHz. Using the prototype, the ability of the inverter for operating

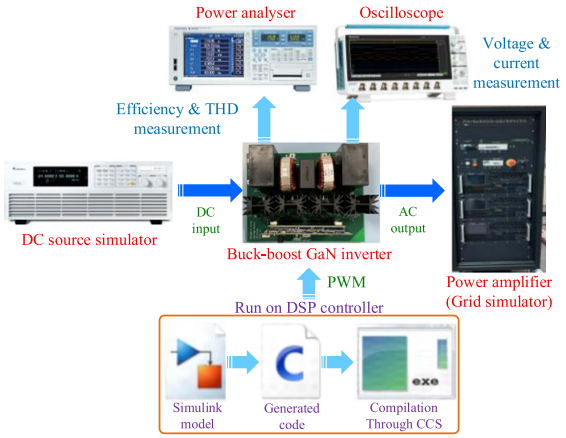

FIGURE 8. Overview of the experimental systems.

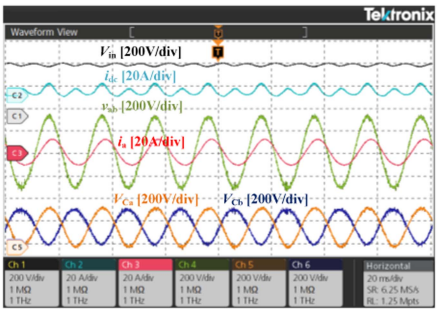

FIGURE 9. Results, without a second-order ripple controller.

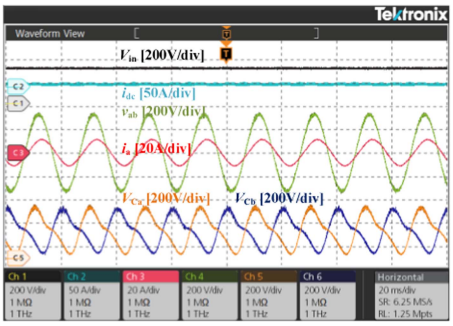

FIGURE 10. Results for input voltage 300 Vdc, with a second-order ripple controller.

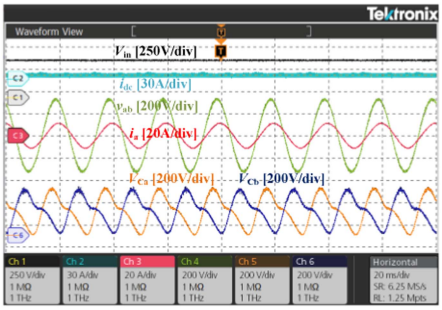

FIGURE 11. Results for input voltage 400 Vdc, with a second-order ripple controller.

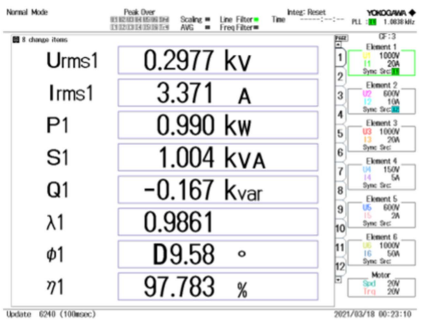

FIGURE 12. Maximum efficiency of the buck-boost inverter.

with wider DC voltage, power decoupling and filtering was experimentally demonstrated. Also, the accuracy of optimal design was validated through comparing actual efficiency, power density and cost to their target values.

Fig. 8 shows the experiment setup. The system consists of the designed inverter, which is controlled by a Delfino F2837xD unit, a DC source simulator (MODEL 62000H-S SERIES), a power amplifier (PA-3x3000-AB/260/2G), a power analyzer (Yokogawa WT1800) and oscilloscope (Tektronix 8-channel MSO58). The DC source simulator produces the input voltage to the inverter. The power amplifier emulates the grid that the inverter was connected to. The power analyzer is used to measure the inverter's efficiency and AC current harmonics.

D. EXPERIMENTAL ASSESSMENT OF DESIGNED INVERTER

The inverter was first operated at 300 Vdc and 230 Vac. Fig. 9 shows the results without enabling the second-order ripple controller; and Fig. 10 shows those with second-order ripple controller enabled. It can be seen that the second-order ripple in the DC-link current (blue curve i_{dc}) is reduced after enabling the ripple controller. Both results show smooth AC outputs, demonstrating the inherent filtering function.

The wide DC voltage operation of the inverter is then verified experimentally by varying the input voltage from 300 V, see Fig. 10 to 400 Vdc, see Fig. 11. When changing the input voltage, the inverter operated smoothly to the desired output. This confirms that the inverter performed well in both buck and boost modes, with different dc voltages (300 Vdc and 400 Vdc).

The efficiency of the inverter is calculated for different operating power. The maximum efficiency of the inverter is 97.78% at 990 W as shown in Fig. 12. Fig. 13 shows the efficiency of the inverter operated from 100 W to 1.8 kW. The measured maximum efficiency matches well with its target value (98.3%), with an error of only 0.5%. The measured power density is 4.36 kW/dm^3, which is actually higher than the target value of 3.5 kW/dm^3, and the cost is £253 which is of ANN difference compared to the designed value £257.9 (e.g., 1800/6.98). This verifies the accuracy of the optimal design of the proposed inverter.

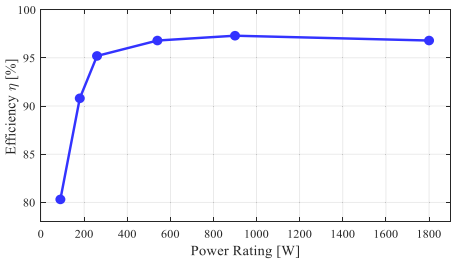

FIGURE 13. Efficiency of grid-connected inverters.

TABLE 3 Simulation Parameters

Parameters	Values
Input voltage V_{in}	250 - 300 V
Output voltage v_{ab}	230 V
Line frequency f	50 Hz
Switching frequency f_{sw}	100 kHz
Inductors L_{a} and L_{b}	150 μH
Capacitors C_{a} and C_{b}	60 μF

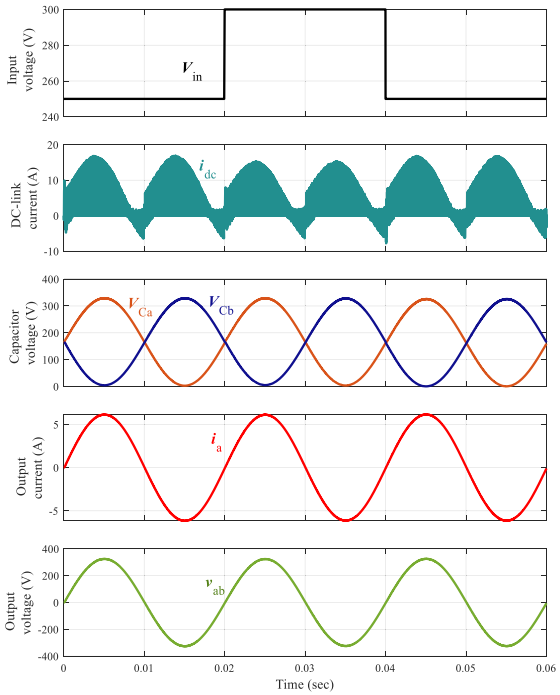

FIGURE 14. Operation without second-order ripple controller.

E. ADDITIONAL SIMULATION VERIFICATION

Simulation studies were performed to validate the operation of the proposed inverter with varying input DC voltage (V_{in}) and its functionality of power decoupling and filtering. The simulation parameters are given in Table 3. The inverter connects to a DC source, and outputs a 1 kW AC power. The simulation performance of the inverter is verified by changing the input voltage from 250 V to 300 V, which can be seen in the input voltage performance of Fig. 14. At 0.02 sec, the input voltage

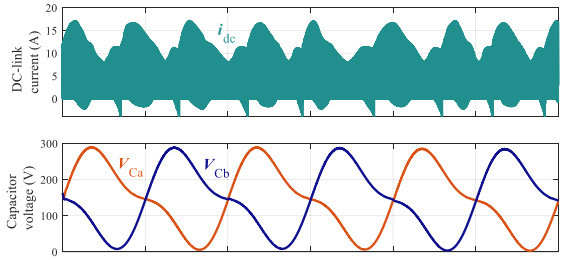

FIGURE 15. Operation with second-order ripple controller.

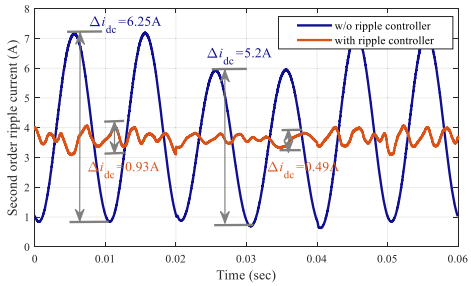

FIGURE 16. Effectiveness of ripple controller on DC-link current.

is changed to 300 V and then again changed back to 250 V at 0.04 sec. The power decoupling is achieved by enabling a second-order ripple controller based on proportional-resonant control blocks. The controller was initially disabled, and the results are given in Fig. 14. It is seen that the inverter can output smooth and sinusoidal AC outputs with V_{in} varying DC, without any extra DC/DC converters and AC filters. However, the 100 Hz components can be observed in the DC link current (i_{dc}).

In Fig. 15, the same test was conducted but with the ripple controller enabled. The 100 Hz components in i_{dc} were then eliminated and stored in the output capacitors. The ripple elimination capability is further compared by measuring the 100 Hz in Fig. 16. Fig. 16 shows the detailed comparison of the magnitude of the second-order ripple, observed through a low pass filter. It can be seen that the amplitude of second-order ripple in the DC-link current Δi_{dc} is 6.25 A and 5.2 A for inverter operating at 250 V and 300 V. This was significantly reduced to 0.93 A and 0.49 A after enabling the ripple controller, which is 7 and 11 times lower.

F. TOPOLOGY COMPARISON

The proposed buck-boost inverter is compared with other buck-boost inverter topologies in terms of the power rating, efficiency, type of switch, number of inductors, capacitors, diodes, and switches (L, C, D, S), (see Table 4).

The proposed inverter has the highest efficiency along with the highest power rating, and hence, the inverter would be suitable for relatively high-power applications. It can eliminate the DC-side second-order ripples and hence avoid using bulky DC links. The ripples are stored in its AC capacitors, which

TABLE 4 Comparison of Buck-Boost Inverters

Topology	Power rating (W)	Efficiency (%)	Type of Switch	No. of (L, C, D, S)
[13]	400	87	Si	2, 2, 0, 4
[14]	400	95.9	Si	1, 3, 0, 6
[15]	500	93	Si	3, 3, 0, 4
[16]	300	87	Si	3, 2, 2, 4
[17]	300	95.7	-	3, 3, 0, 4
[18]	800	95.7	Si & SiC	2, 1, 0, 6
[25]	170	87	Si	2, 2, 3, 5
[26]	500	96.5	Si	1, 2, 0, 8
[27]	500	95.5	Si	1, 2, 0, 6
[28]	300	94.5	-	3, 3, 0, 5
[29]	300	97.4	-	6, 3, 4, 4
[30]	800	94	-	2, 2, 3, 5
Proposed inverter	1800	97.8	GaN	2, 2, 0, 8

also act as part of L-C filters. Hence, no extra filters are required. Most of the other presented topologies can also reduce the DC-side second-order ripples by using large DC-link capacitors, which reduce the efficiency and power density of the inverters [14], [15], [18], and [29]. Moreover, most presented topologies use Si power switches. These switches' switching frequency and efficiency is lower than that of the GaN devices. The presented inverters also have fewer total number of inductors and capacitors compared to those in [14], [16], [17], [28], and [29]. The number of passive components makes a significant contribution to the total power losses and the inverter volume. Hence, the presented inverter is very competitive in terms of volume and power density. Arguably the main shortcoming of the presented in inverter is the usage of eight GaN based switches. This will slightly increase the overall costs. However, four of them are operated at low voltage stress and low-rating switches can be used. Also, in the long run, the inverter has the highest efficiency and hence results in a low cost of energy loss. Using these advantages, the cost of other components, such as the inductor, capacitor, and heat sink, can be reduced, significantly reducing the total component cost of the proposed inverter to £253. The proposed topology has the feature of second-order ripple reduction, which eliminates the need for a bulky DC-link capacitor and reduces the total component cost. However, in [26], the second-order ripple problem is not addressed, and the high filter inductor 1mH is required for a 500W power rating. The proposed inverter requires a total inductor of 0.88mH for a 1.8kW power rating. Therefore, the total cost of the proposed inverter can be reduced compared to [26].

Then, the performance of the proposed inverter topology was compared with conventional two stage and single-stage boost inverters. The comparison parameters are given in Table 5. When compared to [31] and [32], the buck-boost inverters have fewer passive components, high voltage gain, wide operating voltage, no separate output filter and balanced voltage/current stress. The maximum voltage stress of S_1, S_2 S_5, S_6 ($V_{\mathrm{sw,max,buck}}$) depends on the input voltage. The maximum voltage stress of S_3, S_4, S_7, S_8 in boost mode ($V_{\mathrm{sw,max,boost}}$) depends on the capacitor voltage. The current

TABLE 5 Comparison of Existing Boost Inverters

Attributes	Conventional two stage inverter [31]	Single state boost inverter [32]	Proposed buck-boost inverter
Number of stages	2	1	1
Switch count	5	5	8
Diode count	1	2	0
Inductor count	2	3	2
Capacitor count	2	3	2
Voltage gain	$\frac{1}{1-D}$	$\frac{1}{1-3D+D^2}$	$\frac{D_A D_B}{(1-D_{A'})(1-D_{B'})}$
Current mode	Continuous	Continuous	Continuous
Switch voltage stress	V_{out}	$\frac{(1-D)V_{in}}{1-3D+D^2} \in S_0$ $V_{out} \in S_{1-4}$	$V_{\mathrm{in}}D_{\mathrm{A,max}} \in S_1, S_2$ $V_{\mathrm{in}}D_{\mathrm{B,max}} \in S_5, S_6$ $D_{\mathrm{A',max}}V_{\mathrm{Ca}} \in S_3, S_4$ $D_{\mathrm{B',max}}V_{\mathrm{Cb}} \in S_7, S_8$
Switch current stress	$i_L \in S_0$ $I_{dc} \in S_{1-4}$	$\frac{(1-D)I_{dc}}{1-3D+D^2} \in S_0$ $\frac{(2-3D+D^2}{1-3D+D} \in S_{1-4}$	$\frac{V_{\mathrm{Ca}}(1-D_{\mathrm{A}})}{2f_{\mathrm{sw}}L_{\mathrm{a}}} + I_{\mathrm{a}} \in S_{1,2}$ $\frac{V_{\mathrm{Cb}}(1-D_{\mathrm{B}})}{2f_{\mathrm{sw}}L_{\mathrm{b}}} + I_{\mathrm{b}} \in S_{5,6}$ $\frac{V_{\mathrm{in}}D_{\mathrm{A'}}}{2f_{\mathrm{sw}}L_{\mathrm{a}}} + \frac{V_{\mathrm{Ca}}I_{\mathrm{a}}}{V_{\mathrm{in}}} \in S_{3,4}$ $\frac{V_{\mathrm{in}}D_{\mathrm{B'}}}{2f_{\mathrm{sw}}L_{\mathrm{b}}} + \frac{V_{\mathrm{Cb}}I_{\mathrm{b}}}{V_{\mathrm{in}}} \in S_{7,8}$

stress depends on the maximum switching current flowing through the switches which differs between the buck and boost modes, which are calculated based on (30) and (31). The details of voltage and current stress of the proposed inverter are discussed in Section IV-A. A sinusoidal PWM control strategy was presented to control the proposed inverter. However, the voltage and current stress can be reduced further by using discontinuous modulation control strategy.

VI. CONCLUSION

This paper presents the modelling and optimal design of a single-stage buck-boost inverter, which is suitable to operate with varying DC input voltages and simultaneously to provide power decoupling and filtering functions. The operating modes of the inverter were developed. Detailed mathematical modelling of the inverter components' power loss, volume, and cost was presented. This was used as the foundation for a digital multi-objective optimization design process. The criteria of component selection are then discussed, based on which components can be selected to achieve all required functionalities without being oversized. An ANN-based optimal design approach was used to design a 1.8 kW prototype of the single-stage buck-boost inverter, targeting high efficiency, high power density, and low cost. It has been demonstrated

through both experiment and simulation tests using the prototype that the inverter can operate smoothly with varying DC voltages. The power decoupling function of the inverter was achieved by enabling a ripple controller. The ripple in the DC-link current was significantly reduced by more than 10 times. Also, the inverter outputs sinusoidal AC currents with little harmonics without using extra filters.

The accuracy of the optimal design procedure was also validated. Experimental tests show the prototype operated with a maximum efficiency of 97.78%. The power density was measured to be 4.36 kW/dm^3 and the components cost of the prototype is £253. Compared to the outcome of the optimal design method, the errors of efficiency, power density and cost obtained are only 0.5%, 0.86kW/dm^3 and £4.9.

APPENDIX

The output capacitors stored the second order ripple component. The instantaneous power of the capacitors is equal to the ripple components, which can be written as follows:

$$V_{\mathrm{Ca}} i_{\mathrm{Ca}} + V_{\mathrm{Cb}} i_{\mathrm{Cb}} = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2} \cos(2\omega t + \varphi) \tag{A.1}$$

$$V_{\mathrm{Ca}} \left(\mathrm{Ca} \frac{dV_{\mathrm{Ca}}}{dt} \right) + V_{\mathrm{Cb}} \left(\mathrm{Cb} \frac{dV_{\mathrm{Cb}}}{dt} \right) = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2} \cos(2\omega t + \varphi) \tag{A.2}$$

$$\mathrm{Ca} \frac{d(V_{\mathrm{Ca}})^2}{dt} + \mathrm{Cb} \frac{d(V_{\mathrm{Cb}})^2}{dt} = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2} \cos(2\omega t + \varphi) \tag{A.3}$$

The value of output capacitors is equal i.e., Ca = Cb, Then, the above equation can be written as follows:

$$\frac{d(V_{\mathrm{Ca}})^2}{dt} + \frac{d(V_{\mathrm{Cb}})^2}{dt} = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2\mathrm{Ca}} \cos(2\omega t + \varphi) \tag{A.4}$$

Substitute (1) and (2) to (A.4),

$$\frac{d\left(\frac{V_{\mathrm{ab}}}{2}(1 + \sin \omega t) + v_{\mathrm{comp}}\right)^2}{dt} + \frac{d\left(\frac{V_{\mathrm{ab}}}{2}(1 + \sin(\omega t + \pi)) + v_{\mathrm{comp}}\right)^2}{dt} = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2\mathrm{Ca}} \cos(2\omega t + \varphi) \tag{A.5}$$

$$d\left\{ 2\left(\frac{V_{\mathrm{ab}}}{2} + v_{\mathrm{comp}}\right)^2 + \left(\frac{V_{\mathrm{ab}}}{2} \sin \omega t + \frac{V_{\mathrm{ab}}}{2} \sin(\omega t + \varphi)\right)^2 \right\} = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2\mathrm{Ca}} \cos(2\omega t + \varphi)\, dt \tag{A.6}$$

Integrating both the side of the (A.6),

$$2\left(\frac{V_{\mathrm{ab}}}{2} + v_{\mathrm{comp}}\right)^2 + \left(\frac{V_{\mathrm{ab}}}{2} \sin \omega t + \frac{V_{\mathrm{ab}}}{2} \sin(\omega t + \varphi)\right)^2 = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{4\omega \mathrm{Ca}} \sin(2\omega t + \varphi) + C$$

$$v_{\mathrm{comp}} = \sqrt{\left(-\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{8\omega \mathrm{Ca}} \sin(2\omega t + \varphi)\right)} - \sqrt{\left(\frac{V_{\mathrm{ab}}}{4} \sin \omega t + \frac{V_{\mathrm{ab}}}{4} \sin(\omega t + \varphi)\right)^2 + \frac{C}{2}} - \frac{V_{\mathrm{ab}}}{2} \tag{A.7}$$

where C is an integral constant which makes the values of square root to be positive. From (A.7), the compensated voltage v_{comp} can be determined. The required amplitude of ripple compensated voltage is generated by a second-order ripple controller.

REFERENCES

[1] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin, and P. Wang, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1855–1865, Apr. 2015.

[2] H. Zhou and L. He, "Impedance-edited multiple low-frequency harmonic current adaptive suppression," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7022–7033, Jun. 2023.

[3] H. Watanabe, T. Sakuraba, K. Furukawa, K. Kusaka, and J.-i. Itoh, "Development of DC to single-phase AC voltage source inverter with active power decoupling based on flying capacitor DC/DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4992–5004, Jun. 2018.

[4] J. Xu, T. B. Soeiro, F. Gao, H. Tang, and P. Bauer, "Minimum switching losses discontinuous PWM strategy for bidirectional single-phase AC–DC converter with active power decoupling circuit," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 6118–6132, May 2021.

[5] Y. Liu, W. Zhang, Y. Sun, M. Su, G. Xu, and H. Dan, "Review and comparison of control strategies in active power decoupling," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14436–14455, Dec. 2021.

[6] W. Yao, Y. Xu, Y. Tang, P. C. Loh, X. Zhang, and F. Blaabjerg, "Generalized power decoupling control for single-phase differential inverters with nonlinear loads," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1137–1151, Jun. 2019.

[7] Serban, "Power decoupling method for single-Phase H-bridge inverters with no additional power electronics," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4805–4813, Aug. 2015.

[8] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "highly reliable transformerless photovoltaic inverters with leakage current and pulsating power elimination," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 1016–1026, Feb. 2016.

[9] W. Yao, X. Wang, P. C. Loh, X. Zhang, and F. Blaabjerg, "Improved power decoupling scheme for a single-phase grid-connected differential inverter with realistic mismatch in storage capacitances," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 186–199, Jan. 2017.

[10] G. Zhu, S. Tan, Y. Chen, and C. K. Tse, "Mitigation of low-frequency current ripple in fuel-cell inverter systems through waveform control," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 779–792, Feb. 2013.

[11] D. B. W. Abeywardana, B. Hredzak, and V. G. Agelidis, "A rule-based controller to mitigate DC-side second-order harmonic current in a single-phase boost inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1665–1679, Feb. 2016.

[12] D. B. W. Abeywardana, B. Hredzak, and V. G. Agelidis, "An input current feedback method to mitigate the DC-side low-frequency ripple current in a single-phase boost inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4594–4603, Jun. 2016.

[13] S. Xu, R. Shao, L. Chang, and M. Mao, "Single-phase differential buck–boost inverter with pulse energy modulation and power decoupling control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 2060–2072, Dec. 2018.

[14] A. A. Khan et al., "Single-stage bidirectional buck-boost inverters using a single-inductor and eliminating common mode leakage current," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1269–1281, Feb. 2020.

[15] C. M. Wang, "A novel Single-stage full-bridge buck-boost inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 150–159, Jan. 2004.
[16] S. Jain and V. Agarwal, "A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1928–1940, Sep. 2007.
[17] A. Kumar and P. Sensarma, "A four-switch single-stage single-phase buck–boost inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5282–5292, Jul. 2017.
[18] C. N. M. Ho and K. K. M. Siu, "Manitoba inverter–single-phase single-stage buck-boost VSI topology," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3445–3456, Apr. 2019.
[19] R. Rajamony, S. Wang, R. Navaratne, and W. Ming, "Multi-objective design of single-phase differential buck inverters with active power decoupling," *IEEE Open J. Power Electron.*, vol. 3, pp. 105–114, 2022.
[20] A. Stupar, T. McRae, N. Vukadinovic, A. Prodic, and J. A. Taylor, "Multi-objective optimization of Multi-level DC–DC converters using geometric programming," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11912–11939, Dec. 2019.
[21] H. Wang, H. Wang, and F. Blaabjerg, "A cost-constrained active capacitor for a single-phase inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6746–6760, Jul. 2020.
[22] D. V. Malyna, J. L. Duarte, M. A. M. Hendrix, and F. B. M. van Horck, "Multi-objective optimization of power converters using genetic algorithms," in *Proc. IEEE Int. Symp. Power Electron., Elect. Drives, Automat. Motion*, 2006, pp. 713–717.
[23] N. Seshasayee, *Understanding Thermal Dissipation and Design of a Heatsink*. Dallas, TX, USA: Texas Instruments Incorporation, May 2011.
[24] R. Rajamony, S. Wang, G. Calderon-Lopez, I. Ludtke, and W. Ming, "Artificial neural networks-based multi-objective design methodology for Wide-bandgap power electronics converters," *IEEE Open J. Power Electron.*, vol. 3, pp. 599–610, 2022.
[25] H. Patel and V. Agarwal, "A single-stage single-phase transformer-less doubly grounded grid-connected PV interface," *IEEE Trans. Energy Convers.*, vol. 24, no. 1, pp. 93–101, 2009.
[26] Y. Tang, X. Dong, and Y. He, "Active buck–boost inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4691–4697, Sep. 2014.
[27] P. Chamarthi, M. Rajeev, and V. Agarwal, "A novel single stage zero leakage current transformer-less inverter for grid connected PV systems," in *2015 IEEE 42nd Photovoltaic Specialist Conf.*, 2015, pp. 1–5.
[28] V. Gautam and P. Sensarma, "Design of ćuk-derived transformerless common- grounded PV microinverter in CCM," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6245–6254, Aug. 2017.
[29] A. A. Khan and H. Cha, "Dual-buck-structured high-reliability and high-efficiency single-stage buck–boost inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3176–3187, Apr. 2018.
[30] K. Awad, O. Abdel-Rahim, and M. Orabi, "A new single-phase single-stage buck-boost inverter for grid connected PV applications," in *Proc. IEEE Conf. Power Electron. Renewable Energy*, 2019, pp. 32–37.
[31] H. Zhang, W. Li, H. Ding, C. Yi, and X. Wan, "Observer-pattern modeling and nonlinear modal analysis of two-stage boost inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6822–6836, Aug. 2018.
[32] P. Shaw, S.U. Hasan, M.N.H. Khan, and Y.P. Siwakoti, "A new single-stage continuous input current-based high gain boost inverter: Analysis and implementation," *Int. J. Circuit Theory Appl.*, vol. 49, no. 6, pp. 1659–1677, 2021.

RAJESH RAJAMONY received the M.S. (By Research) degree in electrical and electronics engineering from Anna University, Chennai, India, in 2015, and the Ph.D. degree in electrical and electronic engineering from Cardiff University, Cardiff, U.K., in 2022. He is currently a Senior Power Electronics Control Engineer with Jaguar Land Rover, Coventry, U.K. His research interests include wide-bandgap power converters, modelling, and design and control of power electronic systems.

SHENG WANG (Member, IEEE) received the B.Eng. degree from Cardiff University, Cardiff, U.K., and North China Electric Power University, Beijing, China, in 2011, and the Ph.D. degree from Cardiff University, in 2016. During 2013–2014, 2016–2018, and 2018–2020, he was a Research Assistant, Research Associate, and KTP Associate with Cardiff University. Since 2020, he has been a Lecturer with the School of Engineering, Cardiff University. His research interests include active gate drivers, power electronic devices, wide-bandgap semiconductors, control and protection of HVDC and MVDC. He is the Vice-Chair of IEEE PELS U.K. & I Chapter and Research Fellow with Compound Semiconductor Applications Catapult, Newport, U.K.

WENLONG MING (Member, IEEE) received the B.Eng. and M.Eng. degrees in automation from Shandong University, Jinan, China, in 2007 and 2010, respectively, and the Ph.D. degree in automatic control and systems engineering from the University of Sheffield, Sheffield, U.K., in 2015. He has been a Reader of semiconductor power electronics with Cardiff University, Cardiff, U.K., since August 2023, and a Senior Research Fellow funded by Compound Semiconductor Applications Catapult, Newport, U.K., for 5 years since April 2020. He was an Academic Visiting Scholar with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, in 2012. He has coauthored more than 60 papers published in leading journals or refereed IEEE conferences. His research interests focus on packaging, characterization, modeling, and applications of wide-bandgap compound semiconductor power devices. He was the recipient of the prestigious IET Control & Automation Doctoral Dissertation Prize in 2017.