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Optimal LLC Converter Design With Topology Morphing Control for Wide Voltage Range Battery Charging Applications

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ABSTRACT LLC converters benefit from soft switching and sinusoidal currents over dual active bridge (DAB) converters. The design process of an LLC converter involves the selection of resonant tank inductor, capacitor, magnetizing inductance, resonant frequency, and transformer turns ratio for proper operation within the desired range of voltages and power. However, the design and control of frequency-modulated LLC converters in wide voltage range applications is challenging due to the wide range of switching frequencies. Topology morphing control is an established technique utilized for countering the challenges of wide voltage range LLC operation. This work provides a design framework for an LLC converter with topology morphing for wide voltage range applications. The proposed design framework uses time domain analysis and a power loss model to evaluate the optimal converter parameters for efficiency maximization over the entire voltage range. Methodology of implementing online topology morphing with closed-loop control in a digital signal processor (DSP) considering an on-board battery charger (OBC) application is also provided. The design optimization process and control methodology are validated through a 300–700 V input, 250–450 V output, 3.3 kW hardware demonstrator. An experimental peak efficiency of 97.72% is achieved compared to a calculated 97.63% efficiency, proving the accuracy of the analytical model. Time weighted averaged efficiency above 96.7% is observed over the entire voltage range.

INDEX TERMS DC-DC converter, design optimization, frequency modulation, LLC, online topology morphing, resonant converter, time domain model, wide voltage range applications.

I. INTRODUCTION

The applications of DC-DC power converters in industrial and automotive fields are becoming increasingly sophisticated, with high demands for efficiency, power density, and complex application ratings. Compatibility for wide voltage range operation is one such requirement in DC-DC converters. Wide voltage range sources and loads in isolated DC-DC converter applications include renewable energy sources such as solar photo voltaic systems, fuel cells, and high voltage (HV) EV batteries [1]. The commonly used HV battery technologies in EVs, NMC and LFP Lithium-ion batteries, have a cell voltage range of 3–4.2 V and 2.5–3.65 V, respectively [2], [3]. This results in a wide voltage range in the battery pack, such as 250–450 V in 400-V nominally rated batteries, 610–850 V in 800-V nominally rated batteries, and 890–1250 V in 1.25-kV nominally rated batteries [4], [5].

Based on the analysis presented in [5], it is preferable for the power factor correction (PFC) rectifier to operate approximately unity voltage gain to minimize its losses. Hence, aside from HV batteries having a wide voltage range, the various global AC voltage levels can results in a wide voltage range at the input DC bus of the OBC's DC-DC converter. The input voltage (V_{in}) range of the OBC may range from 150–850V, considering AC voltage levels of 208Y/ 120V (240V split phase), 480Y/ 277V, or 600Y/ 347V in North America [3].

Resonant topologies are attractive for DC-DC converter applications as they benefit from a wide range of soft switching and near sinusoidal currents [6]. However, LLC/ CLLC

TABLE 1. Comparison Among State-of-the-Art Optimized LLC Converter Design Methods

Ref.	Optimization objective	Optimization variables	Optimization algorithm	Model	V_{in}/V_o range†	Benefits	Drawbacks
[11]	Minimize power loss	C_r, L_r, L_m	–	TDA	narrow input/ fixed output	Less computation time	Optimized at worst case operating point, n is not optimized
[17]	Maximize TWAE	C_r, L_r, L_m	variable step exhaustive search	TDA	narrow input/ output	Optimized for the entire V_o range	Optimized at worst case V_{in}, n is not optimized
[18]	Maximize efficiency	C_r, L_r, L_m, n, f_s	MATLAB fmincon	TDA	fixed input/ output	Use of mode solver to find accurate operating mode	Fixed V_{in} and V_o are considered
[19]	Minimize backflow power	C_r, L_r, L_m (fixed f_r)	–	FHA	fixed input/ wide output	A control method to reduce backflow power is not required	n is not optimized, Fixed V_{in} is considered
[20]	Minimize $v_{c,RMS}$ Minimize f_s range and RMS currents	C_r, L_r, L_m, n	Genetic algorithm (GA)	TDA	fixed input/ narrow output	Hierarchical optimization	Magnetics design not considered
[21]	Minimize RMS currents and core loss	C_r, L_r, L_m	GA	Data driven model	narrow input/ fixed output	Less computation time, multi-objective optimization	n is not optimized
This work	**Maximize TWAE averaged over V_{in}**	**C_r, L_r, L_m, f_r, n**	**fixed step exhaustive search**	**TDA**	**wide input/ ouput**	**Optimized for the entire operating region**	**High computation time**

† If $V_{in,max}/2 \geq V_{in,min}$ the voltage range is considered as wide, otherwise narrow.

converters with frequency modulation (FM) naturally prefer a narrow range of voltages to ensure operation in a narrow range of switching frequencies (f_s). Nevertheless, the LLC/CLLC converters are being explored alongside topological and control modifications for wide voltage range applications [1]. The techniques applied to implement wide voltage range operation can be classified into topological improvements or design and control optimizations [1]. Topological improvements include interleaving the inverter and/or rectifier bridges, interleaving transformers with multiple resonant tanks, or using additional switching legs [7], [8], [9], [10]. Design and control optimization methods include optimizing the converter design and control employing a hybrid control such as duty cycle and frequency control or topology morphing control [11], [12], [13]. The voltage gain of a DC-DC converter (G) is defined in terms of V_{in} and output voltage (V_o) as $G = nV_o/V_{in}$, where $n:1$ is the transformer turns ratio. Let the range of voltage gain of the converter be defined as $G = [G_{\min}, G_{\max}]$. As analyzed and concluded in [1], for voltage gains around the range $[G_{\min}, 2G_{\min}]$, topological improvements are not necessary and can be managed with the design and control optimization of conventional LLC/ CLLC topologies. The focus of this work falls under the category of design and control optimization for wide voltage range applications.

Changing the primary bridge of the converter between a full bridge (FB) and a half bridge (HB) is known as topology morphing (TM) [14]. In wide voltage range applications, TM is applied to the primary bridge (inverter) such that it operates in FB mode at lower voltage gains and in HB mode at higher voltage gains. The effective voltage gain during HB mode ($G_{HB} = nV_o/(V_{in}/2)$) is double that during FB ($G_{FB} = nV_o/V_{in}$), because the applied inverter voltage is [0, V_{in}] in HB mode compared to [-V_{in}, V_{in}] in FB mode. Implementing TM in resonant topologies is more convenient, as they can use the resonant capacitor as the DC blocking capacitor to minimize flux walking in the transformer [15]. Non-resonant topologies would require an additional capacitor and a switch to allow TM [16].

The resonant tank design of LLC/ CLLC includes the selection of resonant frequency (f_r), resonant tank inductance (L_r) and capacitance (C_r), magnetizing inductance (L_m), and n. When wide voltage range applications are considered, optimizing the resonant converter design is necessary to maximize efficiency and power density over the converter's entire voltage/ power range. A comparison among existing techniques for optimal LLC converter design methods is given in Table 1.

While TM in LLC converters can be achieved with the conventional topology without additional devices, morphing between FB and HB during normal operation should not adversely affect the output voltage stability or cause voltage and current stress beyond maximum component ratings. To ensure this, online topology morphing (OTM) has been explored in literature and generally falls under two categories: optimal trajectory control (OTC) based methods and gradual duty ratio variation based methods. State plane analysis based OTC facilitates transition between FB and HB instantaneously by implementing a transition trajectory control [13], [22], [23]. Gradual duty ratio variation methods are implemented where

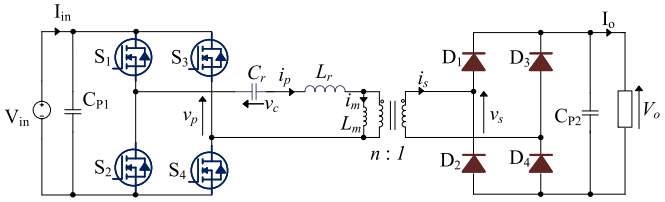


FIGURE 1. LLC converter topology.

linearized compensators are used in the closed-loop control [14], [24]. Although OTC control has superior response time and lower overshoot/ undershoot in V_o during TM, OTC implementation in LLC converters require measurements of state variables (resonant inductor current and resonant capacitor voltage), driving down power density and increasing the complexity of the control implementation. Hence, this work uses a gradual duty ratio variation method to implement OTM.

Considering the aforementioned points, this work provides the optimal design and control procedure for an LLC converter employing TM for wide voltage range applications. The LLC converter topology seen in Fig. 1 is considered in this work. The primary bridge morphs between FB and HB, and the secondary diode bridge will inherit synchronous rectification (SR). The authors previously proposed a methodology for converter design optimization using the time domain analysis (TDA) model for efficiency maximization in [25]. Due to the comprehensive nature of the TDA, it requires significant computational time and resources. This work improves the TDA model with faster computational time and validates the proposed design optimization methodology through a 3.3kW, 300–700V input voltage, and 250–450V output voltage hardware demonstrator for an on-board battery charger (OBC) application.

Since a smooth closed-loop control system is required for OTM implementation, the digital implementation of a cascaded closed-loop control system with online gain scheduling is also proposed. The design of dual loop control, with an inner current loop and an outer voltage loop for LLC converters based on small signal model analysis has been previously explored in [26], [27]. In [27], the current compensator consists of lookup table (LUT) based adaptive PI gains, LUT-based f_s feed-forward, and adaptive saturation limits with an anti-windup scheme to maintain tight current regulation for operation within a wide V_{in} and V_o range. The literature on OTM integrated closed loop control is limited to single loop control structures as presented in [14], [28] using voltage-controlled oscillators (VCOs). The closed-loop control developed in this work maintains tight voltage/current regulation by implementing gain scheduling in compensators through a regression model. This would use less memory compared to LUT-based methods.

Following the design and verification of a stable closed-loop control system, the OTM techniques are discussed. The existing OTM technique based on linearized compensator designs is an asymmetrical duty variation method for the primary bridge voltage [14]. The main drawback of this method is the DC-offset in the magnetizing current caused by asymmetrical bridge currents. To mitigate this, a symmetrical duty variation OTM technique is proposed in this work. Trade-offs of the asymmetrical and symmetrical approaches are outlined and guidelines of which OTM technique to select based on the design parameters are provided.

The contributions in this work are summarized below:

- Design optimization method for an LLC converter with TM, improving the work of [25] with lesser computational time.
- Digital implementation of a cascaded closed-loop control with regression model-based gain scheduling for an OBC application.
- Digital implementation of an OTM control method with minimized DC offset in transformer magnetizing current.
- A comparative analysis between asymmetrical and symmetrical OTM techniques and guidelines for selecting the most suitable OTM technique.

The rest of the manuscript is organized as follows: Section II provides the TDA-based design optimization method for an LLC converter with TM. Section III provides the cascaded closed-loop control design with gain scheduling. Section IV analyzes the existing OTM technique and improves its drawbacks by proposing a new OTM technique. Experimental validation is provided through a 3.3kW hardware demonstrator intended for an OBC application in Section V.

II. DESIGN OPTIMIZATION OF THE LLC CONVERTER

The LLC converter can be modeled either in the frequency domain using first harmonic approximation (FHA) based modeling or in the time domain. The accuracy of the FHA model is confined to operation within close proximity of $f_s = f_r$. Hence, in the case of wide voltage range applications, the accuracy of the FHA model would not suffice due to the large f_s range. On the other hand, the TDA model is more accurate than the FHA model but, computationally exhaustive. While it is challenging to obtain closed-form solutions with TDA, numerical solutions can be obtained using computational tools such as MATLAB. This section presents the development of the TDA model and the optimal design process of a TM-enabled LLC converter for efficiency maximization.

A. TIME DOMAIN MODEL

A step-by-step method of deriving the TDA model for an LLC converter considering both FB and HB at the inverter is provided in the authors' previous work [25]. The derivations are made based on the equivalent circuits in Fig. 2. The converter operation switches among the equivalent circuits A, B, and C based on the three modes of operation, $f_s = f_r$, $f_s < f_r$, or $f_s > f_r$, respectively. The timing intervals for each equivalent circuit A–C are illustrated in the waveforms of Fig. 3 and Table 2. The summary of all the functions derived for the

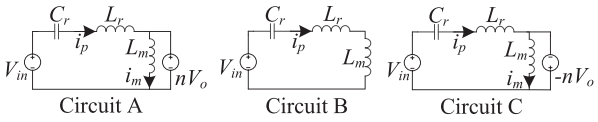


FIGURE 2. Equivalent circuits of LLC converter for three modes of operation in Table 2.

TABLE 2. Equivalent Circuits for $f_s < f_r$, $f_s = f_r$, and $f_s > f_r$

Mode of Operation	Equivalent Circuit
$f_s = f_r$	$0 \le t \le T_s/2$: Circuit A
$f_s < f_r$	$0 \le t \le t_b$: Circuit A, $t_b \le t \le T_s/2$: Circuit B
$f_s > f_r$	$0 \le t \le t_c$: Circuit A, $t_c \le t \le T_s/2$: Circuit C

TABLE 3. Time Domain Functions for Each Equivalent Circuit With Primary FB. For Equivalent Primary HB Functions Simply Add an Offset of $V_{in}/2$ to v_c

Circuit	Functions
A	$i_{pa}(t) = \frac{(-v_{ca0} + V_{in} - nV_o)}{\omega_r L_r} \sin(\omega_r t) + i_{pa0} \cos(w_r t)$
	$v_{ca}(t) = (v_{ca0} - V_{in} + nV_o) \cos(\omega_r t) + \frac{i_{pa0}}{\omega_r C_r} \sin(\omega_r t) + (V_{in} - nV_o)$
	$i_{ma}(t) = \text{sgn}(v_p) i_{pa0} + \frac{\text{sgn}(v_p) nV_o}{L_m} t$
B	$i_{pb}(t) = i_{mb}(t) = \frac{V_{in} - v_{cb0}}{\omega_1 (L_m + L_r)} \sin[\omega_1 (t - t_b)] + i_{pb0} \cos[\omega_1 (t - t_b)]$
	$v_{cb}(t) = (v_{cb0} - V_{in}) \cos[\omega_1 (t - t_b)] + \frac{i_{pb0}}{\omega_1 C_r} \sin[\omega_1 (t - t_b)] + V_{in}$
C	$i_{pc}(t) = i_{pc0} \cos[\omega_r (t - t_c)] - \frac{(V_{in} - v_{cc0} + nV_o)}{L_r \omega_r} \sin[\omega_r (t - t_c)]$
	$v_{cc}(t) = \frac{i_{pc0}}{\omega_r C_r} \sin[\omega_r (t - t_c)] + (V_{in} - v_{cc0} + nV_o) \cos[\omega_r (t - t_c)] - V_{in} - nV_o + 2v_{cc0}$
	$i_{mc}(t) = i_{mc0} - \frac{nV_o (t - t_c)}{L_m}$

primary AC current (i_p), voltage across the resonant capacitor (v_c), and magnetizing current (i_m) with respect to time are given in Table 3. It should be noted that the functions remain the same for both FB and HB operations at the primary bridge, except that v_c will have a DC offset of $V_{in}/2$ during HB mode.

The boundary values of the resonant tank currents and voltages in each equivalent circuit are denoted by i_{pa0}, v_{ca0}, i_{pb0}, v_{cb0}, i_{pc0}, and v_{cc0}. The boundary times for equivalent circuit A during $f_s < f_r$ and $f_s > f_r$ operations are denoted by t_b and t_c (as seen in Fig. 3), respectively. These boundary values and times need to be known to compute the functions in Table 3. The functions to compute the boundary values and times are formulated based on the boundary conditions and load current (I_o), as seen in Table 4. For the case of $f_s = f_r$ a closed form solution can be formed. However, for cases $f_s > f_r$ and $f_s < f_r$ the respective boundary values must be solved numerically.

The TDA model derived can be used to evaluate f_s of the LLC converter for a given operating point (V_{in}, V_o, and I_o of interest). High computational time to solve the TDA model is often seen as a disadvantage. However, computational time can be optimized by using tools such as MATLAB along with line search techniques to compute the boundary values and f_s [29]. MATLAB inbuilt solvers are used to solve for boundary voltage and current values, while the interval halving line search technique is used to solve for f_s and boundary time values. Fig. 3 also compares the waveforms of i_p and v_c from the TDA and the PLECS models for the three cases of $f_s = f_r$, $f_s < f_r$, and $f_s > f_r$ operation. It is observed that the TDA model closely follows the PLECS model results. Furthermore, a comparison amongst PLECS simulation, FHA, and TDA models of f_s estimation as a function of voltage gain is provided in Fig. 4(a). The average error in the FHA model compared to PLECS simulation results is ≈8%, while the error in the TDA model compared to the PLECS model is ≈1%. Moreover, the error in root mean square (RMS) values of i_p and v_c from the TDA and PLECS models are compared in Fig. 4(b). The average error of $i_{p,RMS}$ and $v_{c,RMS}$ over the entire f_s range is ≈2%. Hence, the TDA model is sufficiently accurate in estimating the operating point f_s and the RMS currents and voltage.

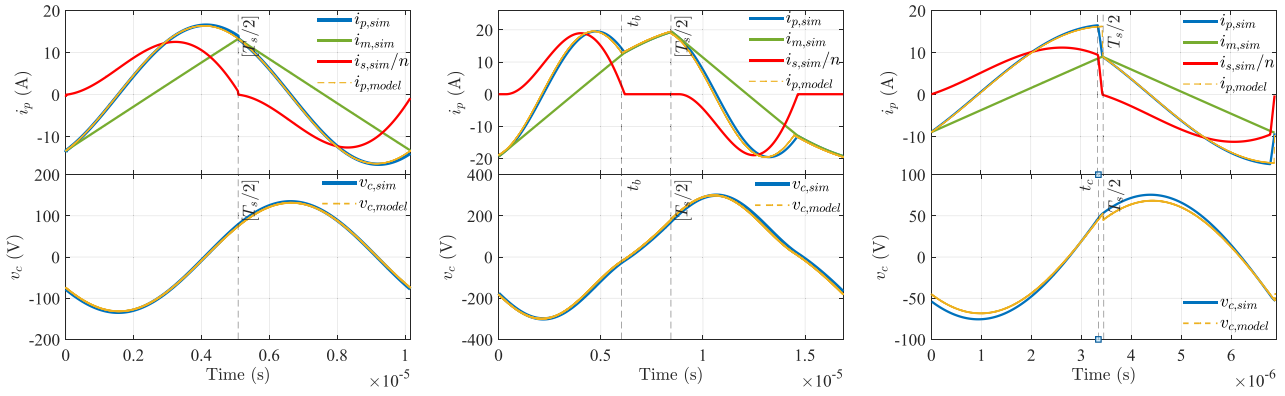
B. DESIGN OPTIMIZATION PROCESS

The aim of design optimization is to evaluate the optimal values for L_r, C_r, L_m, n, and f_r to maximize the converter efficiency over the entire operating range. Since the optimization objective is efficiency maximization, a power loss model is developed and used to derive the objective function.

The proposed optimal design method is applied to design an LLC converter intended for an OBC application. A design example with specifications in Table 5 is considered to verify the proposed design process. The required voltage gain range is reduced by utilizing TM for the primary bridge as previously discussed. As explained in the authors' previous work in [25], TM effectively reduces the range of f_s and converter voltage and current stresses. Hence, the proposed optimal design method determines the voltage gain range of FB–HB operation and optimizes the converter design for the effectively reduced range of voltage gain and corresponding converter stresses.

1) CONVERTER LOSS MODEL

A detailed converter loss model is developed to determine converter efficiency and formulate the objective function of the design optimization procedure. Semiconductor and magnetic losses are determined in the loss model. The analytical models for these loss computations are widely provided in the literature and are summarized in Table 6. The RMS and switching currents are computed based on the current functions derived from the TDA model and known

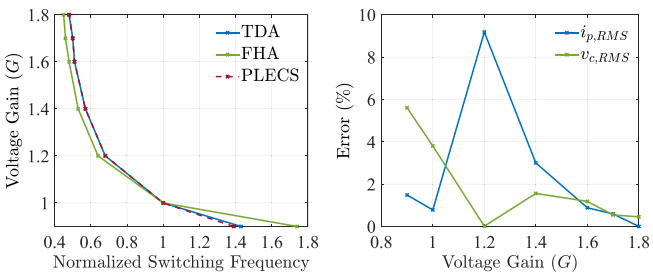


(a) $f_s = f_r$ (b) $f_s < f_r$ (c) $f_s > f_r$

FIGURE 3. Resonant tank current and voltage waveforms during three modes of operation with a primary FB.

TABLE 4. Functions to Compute Boundary Values Seen in Table 3 for the Three Modes of Operation. The Modes of $f_s < f_r$ and $f_s > f_r$ are to be Solved Numerically

Mode of Operation	Functions
$f_s = f_r$	$i_{pa0} = \dfrac{-nV_o}{4L_m f_s}, \quad v_{ca0} = \dfrac{-\pi^2 L_r f_s I_o}{n} + V_{in} - nV_o$
$f_s < f_r$	$i_{pb0} = i_{pa}(t_b) = i_{ma}(t_b), \quad v_{cb0} = v_{ca}(t_b), \quad -i_{pa0} = i_{pb}(T_s/2), \quad v_{ca0} + v_{cb}(T_s/2) = \begin{cases} V_{in}, & \text{if HB} \\ 0, & \text{if FB} \end{cases}$ $\dfrac{I_o}{n} = \dfrac{2}{T_s}\left[\dfrac{i_{pa0}}{\omega_r}\sin(\omega_r t_b) - \dfrac{V_{in} - nV_o - v_{ca0}}{\omega_r^2 L_r}(\cos(\omega_r t_b) - 1) - i_{pa0} t_b - \dfrac{nV_o}{2L_m} t_b^2\right]$
$f_s > f_r$	$i_{pc0} = i_{pa}(t_c), \quad i_{mc0} = i_{ma}(t_c), \quad -i_{pa0} = i_{pc}(T_s/2) = i_{mc}(T_s/2), \quad v_{cc0} = v_{ca}(t_c), \quad v_{ca0} + v_{cc}(T_s/2) = \begin{cases} V_{in}, & \text{if HB} \\ 0, & \text{if FB} \end{cases}$ $\dfrac{I_o}{n} = \dfrac{2}{T_s}\Big[\dfrac{i_{pa0}}{\omega_r}\sin(\omega_r t_c) + \dfrac{i_{pb0}}{\omega_r}\sin[\omega_r(T_s/2 - t_c)] - i_{pa0} t_c - i_{mc0}(T_s/2 - t_c) - \dfrac{V_{in} - nV_o - v_{ca0}}{\omega_r^2 L_r}\cos(\omega_r t_c) +$ $\dfrac{V_{in} + nV_o - v_{ca0}}{\omega_r^2 L_r}\cos[\omega_r(T_s/2 - t_c)] + \dfrac{-v_{ca0} + v_{cc0} - 2nV_o}{\omega_r^2 L_r} + \dfrac{nV_o T_s}{4L_m}(-2t_b + T_s/2)\Big]$



(a) Voltage gain vs. normalized switching frequency.

(b) Percentage error in i_p and v_c between TDA and PLECS models.

FIGURE 4. Comparison among TDA, FHA, and PLECS simulation models for f_s, i_p, and v_c.

TABLE 5. Specifications of the Design Example for LLC Converter Design Optimization

Notation	Description	Rating
V_{in}	Input voltage	300–700 V
V_o	Output voltage	250–450 V
P_o	Maximum output power	3.3 kW

switching instances. MOSFET on-state resistance ($R_{DS,on}$), diode forward voltage (V_F), and MOSFET switching energy tables (E_{on} and E_{off}) are available in the manufacturer data sheets. E_{on} and E_{off} can also be estimated through double pulse tests [30]. The conduction loss from the MOSFET body diodes during dead time (t_d) is also defined as a function of MOSFET turn-off current ($I_{Si,off}$), forward bias voltage of the body diode (V_{SD}), t_d, and f_s. The total equivalent series resistance (ESR) of the resonant tank (R_{res}) is the sum of ESRs of L_r and C_r.

Transformer core selection is based on the minimum switching frequency ($f_{s,min}$) as outlined in [25]. Hence,

TABLE 6. Power Loss Functions

Description	Loss function
MOSFET conduction loss	$R_{DS,on} i^2_{p,RMS}/2$
MOSFET turn-on loss	$f_s E_{on}$
MOSFET turn-off loss	$f_s E_{off}$
MOSFET body diode loss	$f_s t_d V_{SD} \lvert I_{Si,on} \rvert$
Diode conduction loss	$V_F i^2_{s,RMS}/\sqrt{2}$
Transformer core loss	$k_{fe} f_s^{\alpha} B_{max}^{\beta} V_e$
Transformer copper loss	$\frac{(i_{p,RMS}+i_{s,RMS}/n)^2 \lambda^2 MLT \rho}{4 W_A K_u A_c^2 B^2_{max}}$
Resonant tank loss	$i^2_{p,RMS} R_{res}$

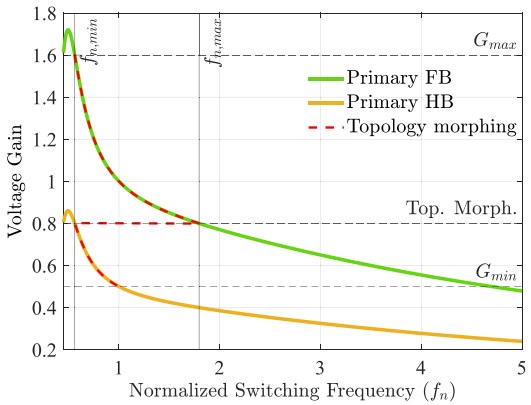


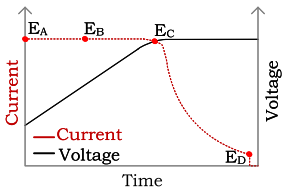
FIGURE 5. Voltage gain ($G = nVo/V_{in}$) with and without TM.

frequency-dependent terms such as volt-seconds product λ, maximum flux density $B_{\max}$, and Steinmetz coefficients (K_{fe}, α, and β) are computed at the operating point corresponding to $f_s = f_{s,min}$. Mean length per turn (MLT), cross-sectional area of the core (A_c), window area (W_A), and core volume (V_e) are dependent on the size of the selected core. ρ is the copper resistivity at 25^0C and K_u is the core utilization factor. For each core obtained from a core database, the copper and core losses are computed using the formulas in Table 6.

2) RANGE OF OPERATION FOR FB AND HB

The voltage gain range for FB and HB modes are illustrated in Fig. 5. Assume the range of $G = nVo/V_{in}$ is G_{min}–$G_{\max}$. When the converter operates in HB mode, its effective voltage gain is doubled. Since $G_{\max}$ for the converter is fixed at $V_{in,min}$ and $V_{o,\max}$, the maximum voltage gain for HB operation should be limited to $G_{\max}/2$. Hence, the FB voltage gain at which TM occurs is $G_{TM} = G_{\max}/2$. The converter will operate in FB mode for $G = [G_{\max}/2, G_{\max}]$ and HB mode for $G = [G_{min}, G_{\max}/2]$.

This will reduce the range of f_s for the entire operating region.



TWAE = $0.033E_A + 0.767E_B + 0.126E_C + 0.074E_D$ [4]

FIGURE 6. Time-weighted average efficiency calculation based on the battery charging profile.

3) DESIGN OPTIMIZATION PROBLEM

The optimization problem is defined using the optimization variables, objective function, and constraints c_1–c_3 as below:

$$\max_{n,h,f_r,Q} \quad \text{Avg. TWAE}$$

$$\text{s.t.} \quad c_1, c_2, c_3 \text{ are met.} \tag{1}$$

$$c_1 : f_{s,\min} > f_r \sqrt{\frac{1}{1+h}} \tag{2}$$

$$c_2 : L_m \leq \frac{t_d}{8 C_{DS} f_{s,\max}} \tag{3}$$

$$c_3 : v_{c,RMS} \leq V_{C,\max} \tag{4}$$

The optimization variables considered are n, Q-factor, $h = L_m/L_r$, and f_r. They are used to calculate resonant tank values as below [31]:

$$L_r = \frac{Q R_{e,\min}}{2\pi f_r}, C_r = \frac{1}{(2\pi f_r)^2 L_r}, L_m = h L_r \tag{5}$$

Fixed step exhaustive search algorithm is used to find the optimal values for n, Q, h, and f_r. The lower bounds for h, and Q are set following a review of typical values in LLC/CLLC converter designs. In the reference design used in this work h and Q are varied in the ranges of [4, 16] and [0.2, 1]. During the process of optimization, it is observed that wider the voltage range is, lower are the upper bounds of h and Q, which can yield feasible converter operation over the entire operating range. Lower and upper bounds for f_r can be set based on semiconductor limits and magnetics design capabilities. In this work, the range of f_r is set to [80, 200] kHz. The step size also affects the accuracy of the optimal values. The step sizes for h, Q, and f_r used in this work are 1, 0.1, and 5 kHz, respectively.

Constraint c_1 ensures operation within the inductive region so that zero voltage switching (ZVS) can be achieved. Constraint c_2 ensures that L_m is set such that the available dead time can guarantee full ZVS. The last constraint, c_3, ensures that resonant capacitor voltage does not exceed the manufacturable limits ($V_{C,\max}$).

A time-weighted averaged efficiency (TWAE) defined for OBC applications, as illustrated in Fig. 6, is considered to develop the objective function [17]. Since a wide V_{in} range is considered, TWAE is averaged over V_{in} range to obtain

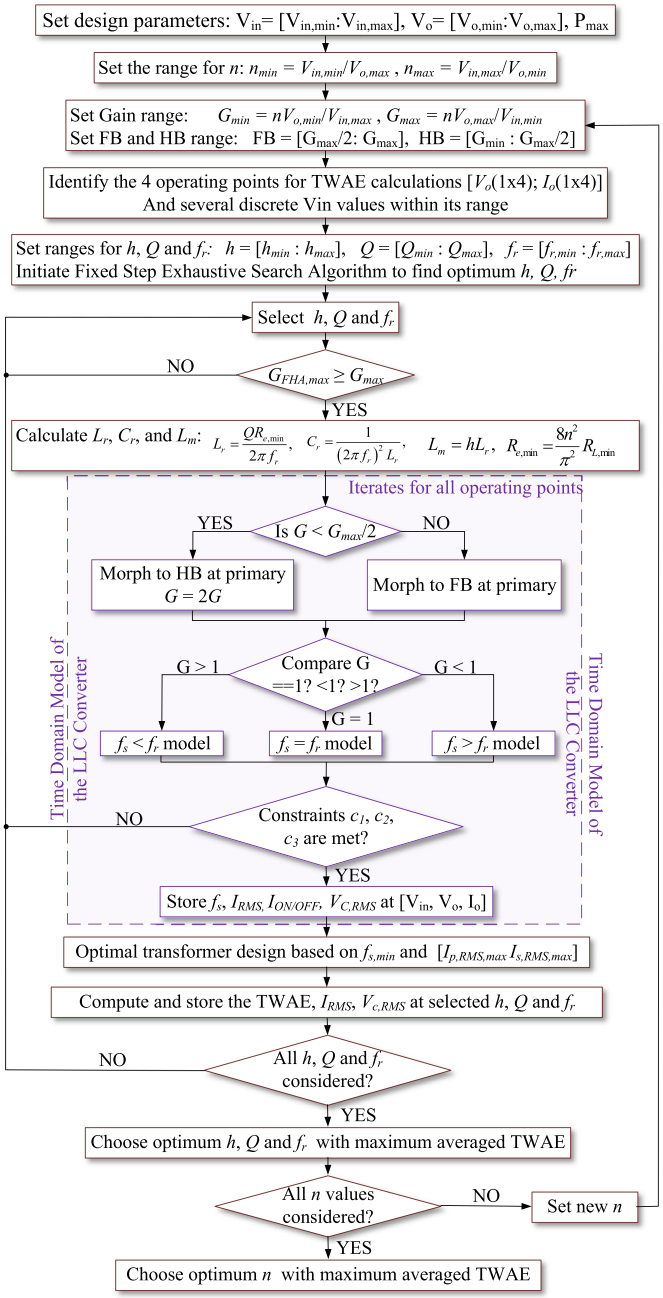


FIGURE 7. Flow chart for the design optimization of the LLC converter with topology morphing.

a single metric to assess the converter performance over the entire operating region. The framework for optimal converter design to maximize the efficiency over the wide voltage range is given in Fig. 7.

For computing semiconductor losses, GeneSiC SiC MOSFETs G3R20MT12K for the primary bridge and GeneSiC SiC diodes GD30MPS12H for the secondary bridge are used in the optimization loss model and the same are also used in the hardware demonstrator. The operating points considered for TWAE calculation are listed in Table 7. The final optimized

TABLE 7. Operating Points for TWAE Calculation

	V_o	I_o
A	250 V	7.3 A
B	350 V	7.3 A
C	450 V	7.3 A
D	450 V	2 A

TABLE 8. Optimal Design Parameters

	Parameter	Value
Key specifications	V_{in}	300–700 V
	V_o	250–450 V
	P_o	3.3 kW
Outputs from the optimal design framework	n	1.2
	h	8
	f_r	100 kHz
	Q	0.2
Resonant tank	L_r	12.7 μH
	C_r	200 nF
	L_m	102 μH
Switching frequency range	f_s	46–150 kHz
Part numbers	S_1–S_4	G3R20MT12K
	D_1–D_4	GD30MPS12H
	C_r	CKC21C663KDGLCAUTO
	L_r	custom made (JR Panel)
	Transformer	custom made (Payton)

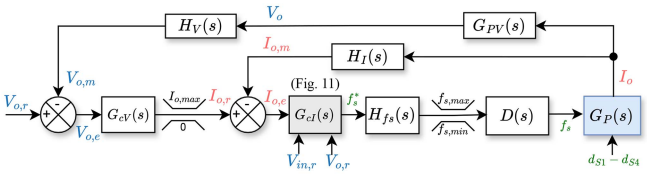


FIGURE 8. Cascaded closed-loop control structure.

parameters of the LLC converter using the proposed framework are given in Table 8.

III. CLOSED LOOP CONTROL DEVELOPMENT

Following the determination of the optimal converter parameters, a stable closed-loop control structure is required to achieve a smooth OTM technique. Hence, the design and implementation of the closed-loop control is discussed in this Section. A cascaded dual loop control structure illustrated in Fig. 8 is developed in this work. The definitions of the transfer functions are given below:

- $G_P(s)$: I_o (output) to f_s (control) transfer function.
- $G_{PV}(s)$: V_o to I_o transfer function.

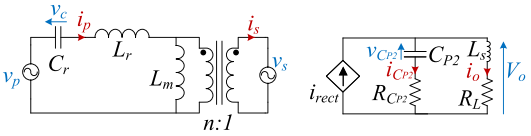


FIGURE 9. Equivalent circuit for state space modeling.

- $H_V(s)$: Multi-stage low pass filters (LPFs) and ADC sample and hold (S/H) delay for V_o measurement.
- $H_I(s)$: Multi-stage LPFs and ADC S/H delay for I_o measurement.
- $G_{cV}(s)$: Voltage compensator.
- $G_{cI}(s)$: Current compensator.
- $H_{fs}(s)$: Single-stage LPF for control output (f_s).
- $D(s)$: Accumulated delays from control hold and computation, digital PWM phase lag, and computation overhead time.
- $TF_{\text{uncomp},I}(s)$: Uncompensated current loop.
- $TF_{\text{uncomp},V}(s)$: Uncompensated voltage loop.
- $TF_{\text{comp},I}(s)$: Compensated current loop.
- $TF_{\text{comp},V}(s)$: Compensated voltage loop.

In battery charging applications, the inner current loop provides tight current regulation, while the outer voltage loop rejects system disturbances and maintains constant voltage regulation [27]. The closed-loop control and OTM are implemented in a Texas Instruments TMS320F28379D digital signal processor (DSP).

A. OPEN LOOP MODEL

An open loop model of the control system is required to design the compensated digital closed-loop control system. The uncompensated open loop ($TF_{\text{uncomp},I}$) is equated as (6). Firstly, the derivation of $G_P(s)$ is discussed.

$$TF_{\text{uncomp},I}(s) = G_P(s)H_I(s)H_{f_s}(s)D(s) \tag{6}$$

The extended describing functions (EDFs) based method introduced in [32] is the most widely used method to derive small signal models for resonant converters as their state variables contain switching frequency harmonics. The small signal model for an LLC converter is well defined in [33] to derive the plant transfer function between the perturbations of V_o and f_s. To derive the transfer function between output current perturbation ($\hat{i_o}$) and switching frequency perturbation ($\hat{f_s}$), the equivalent circuit model given in Fig. 9 is used. To introduce i_o as a state variable to the state space system, a parasitic inductance (L_s) of a very small value is modeled. Using EDFs, nonlinear terms of the state space model such as v_p, v_s, and i_{rect} are approximated. The small signal model derivations are not provided here for brevity [34], [35]. The small signal model will consist of the sine and cosine terms of the state variables i_p, i_s, and v_c, and the DC terms of i_o and $v_{C_{P2}}$. These will formulate $G_P(s)$ as an eighth-order system.

To derive the transfer functions for the delays and filters, which are parts of the open loop model, the methodology discussed in [36] is applied in this work. The RC LPFs are implemented along the signal chain at several locations for noise reduction. The LPF transfer function for a cut-off frequency of ω_k is in the form of $\omega_k/(\omega_k + s)$. The ADC S/H delay ($e^{-sT_{S/H}}$) is modeled using padé approximation [37]. Additional delays due to the DSP computation overhead time, digital PWM delay, and frequency hold delay summed up as the total delay (T_D) is modeled as $D(s) = e^{-sT_D}$.

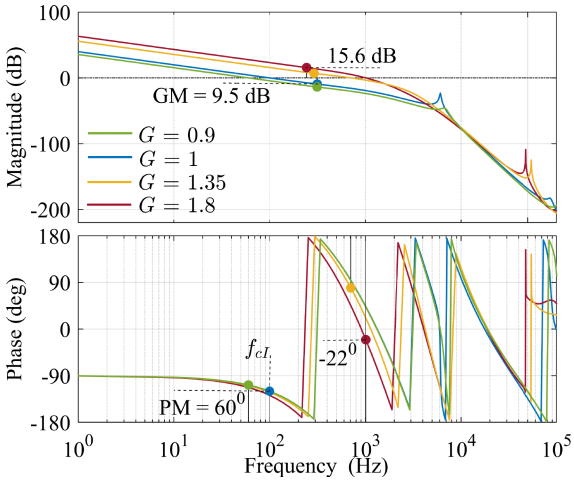


FIGURE 10. Compensated current loop gain for varying G with a PI controller designed at $G = 1$ (before gain scheduling).

B. COMPENSATOR DESIGN

Simple PI controllers ($K_P + K_I/s$) are used as voltage and current compensators. The method provided in [38] is used to design the PI controllers. Since the outer voltage loop should be decoupled and slower than the inner current loop, the cut-off frequency of the voltage loop (f_{cV}) is selected as 10% of the cut-off frequency of the current loop (f_{cI}) [39]. Hence, the cut-off frequencies are selected as $f_{cI} = 100$ Hz and $f_{cV} = 10$ Hz and the desired phase margin (PM) is set to 60°.

1) CURRENT COMPENSATOR

Using the classical frequency response method, open loop gain of $TF_{\text{uncomp},I}(s)$ is utilized for the current compensator design. As discussed in [26] and [27], $G_P(s)$ varies significantly for all the cases of $f_s < f_r$, $f_s = f_r$, and $fs > f_r$. Hence, a single pair of PI gains to make $G_{cI}(s)$ stable for the entire operating region cannot be obtained. The criteria for the system stability in this work is considered as PM > 45° and gain margin (GM) > 6 dB. The compensated current loop gain is formulated as in (7). Fig. 10 shows $TF_{\text{comp},I}(s)$ bode plots using the same PI compensator designed at half load current and unity voltage gain ($f_s = f_r$). It is observed that the compensated system will be unstable as it moves to higher voltage gains.

$$TF_{\text{comp},I}(s) = G_{cI}(s)TF_{\text{uncomp},I}(s) \tag{7}$$

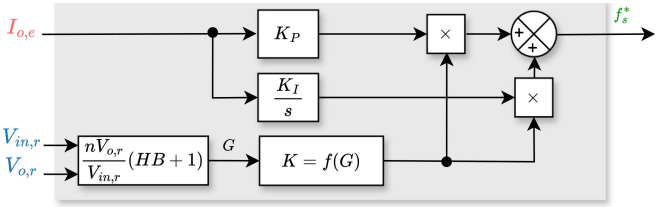


FIGURE 11. Current compensator with gain scheduling.

Adaptive gains are used to maintain stable compensator characteristics (i.e., PM, GM, and bandwidth close to desired values) over the entire operating region. The use of LUTs is a commonly used approach for scheduling the gains in PI controllers [27]. Regression models can avoid the limitations imposed by LUT-based control systems [40]. This work develops a regression model for gain scheduling in the current compensator. The process of developing the regression model is summarized as follows:

- Determine PI controller gains for the voltage gain range $G = G_{min} : G_{\max}$ using the design process previously described.
- Determine the ratios of K_P and K_I at each voltage gain as compared to the PI gains at $G = 1$ (i.e., $K_P/K_{P,G=1}$ and $K_I/K_{I,G=1}$ at a fixed G). It is observed that both K_P and K_I will have similar ratios (K_C) compared to those at $G = 1$ (i.e., $K_C = K_P/K_{P,G=1} = K_I/K_{I,G=1}$ at a fixed G).
- Develop a polynomial regression model for PI gain ratio as a function of G (i.e., $K_C = f(G)$).

The current compensator with gain scheduling is illustrated in Fig. 11. The voltage gain G is adjusted based on FB or HB mode. The flag $HB = 1$ if HB mode is enabled and $HB = 0$ if FB mode is enabled. A fourth-order polynomial is used as $K_C = f(G)$ in this work.

2) VOLTAGE COMPENSATOR

The stability of the current compensator is sensitive to G, whereas that of the voltage compensator is sensitive to the load. It is observed that once the voltage compensator is designed at a specific load current, as the load decreases, f_{cV} increases and vice-versa [36]. Since the voltage loop needs to be slower than the current loop, an increase in f_{cV} beyond f_{cI} is not desired. Hence, both compensators are designed at $G = 1$ and half load current, such that the compensated systems with the gain scheduling in the current loop remain stable for 50% to 100% load currents. For light load regulation (i.e., $I_o < 3.5$A in the design example), the gains of the voltage compensator are lowered by a factor K_V such that $f_{cI}/f_{cV} > 5$. It is observed that a single value for K_V can be fixed upon bode plot analysis at light load currents. The uncompensated ($TF_{\text{uncomp},V}(s)$) and compensated ($TF_{\text{comp},V}(s)$) voltage loop gains are given in (8) and (9), respectively.

$$TF_{\text{uncomp},V}(s) = G_{PV}(s)H_V(s) \tag{8}$$

$$TF_{\text{comp},V}(s) = TF_{\text{uncomp},V}(s)G_{cV}(s) \tag{9}$$

Since an OBC application is considered in this work, the stability of the compensated current and voltage loops over the range of the selected operating points in the charging profile of Fig. 6 for $V_{in} = 300$–700V is verified through frequency response analysis. These bode plots are provided in Fig. 12. It can be seen that throughout the operating points during the charging cycle, PM $> 39^\circ$, GM > 5.5dB, and $f_{cI}/f_{cV} > 5$, are maintained.

C. SOFT START

A soft start process is required to pre-charge the voltage at the output DC bus to the reference voltage level ($V_{o,r}$) to reduce the inrush currents during the converter start-up process and avoid over-voltage/ over-current damage to the devices. Two popular soft start schemes adopted and modified in DC-DC resonant converters are the f_s decreasing method and the phase shift control method [41], [42], [43]. In the f_s decreasing method, the converter starts at a very high f_s so G is low and then gradually decreases f_s to increase G.

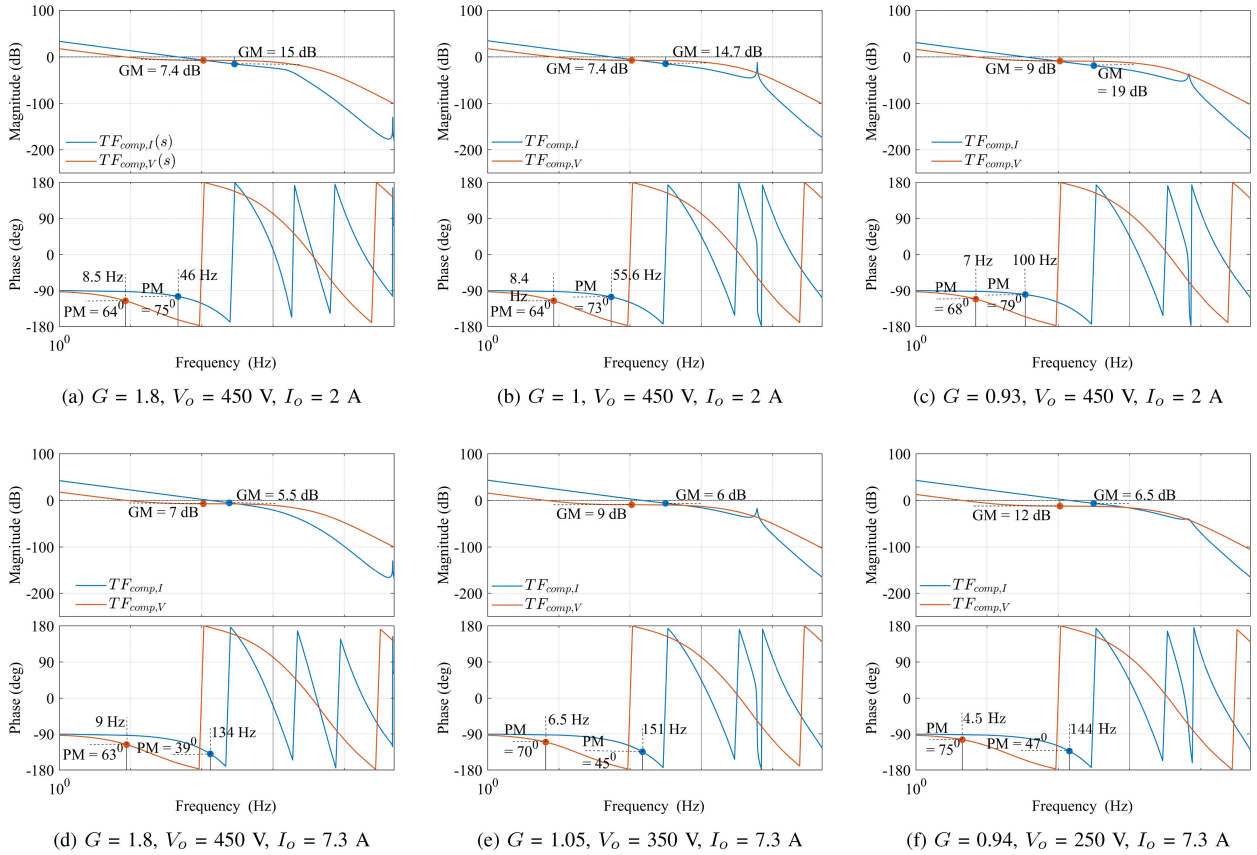
However, with the optimized LLC converter design the highest f_s to implement a frequency decreasing scheme is limited. Hence, the phase shift control method discussed in [42] and [43] is adopted in this work. Soft start schemes under both FB and HB operations are summarized in Fig. 13. Let d_{Si} be the duty ratio [0,1] of switch S_i. The switching frequency used during soft start ($f_{s,SS}$) is estimated using a linear regression model as a function of G, approximated from FHA. This will reduce the frequency error for the closed-loop control once soft start finishes and helps converge $V_{o,m}$ to $V_{o,r}$ faster with minimal distortion. The duty of the bridge voltage v_p is increased from $d = d_{min}$ to 0.5 in steps of Δd. In this work, $\Delta d = 10^{-4}$. In HB mode, the duty ratio of v_p is increased by increasing the duty of the PWM gate signal of S_1. In FB mode, the same is achieved by increasing the phase shift ($\varphi_{S_1-S_3}$) between the PWM gate signals of S_1 and S_3.

D. COMPARISON WITH EXISTING ARCHITECTURE

A comparison of the closed-loop control scheme implemented in this work with existing state-of-the-art is provided in Table 9. The frequency of implementing the control logic inside the DSP is represented by the control frequency. Compared to existing work, the advantages of the proposed cascaded dual loop control system are its ability to cater to a wide range of voltage gain along with the use of regression model-based gain scheduling, avoiding the computational burden of LUTs.

IV. ONLINE TOPOLOGY MORPHING CONTROL

OTM is required to change the topology between FB and HB without disrupting the power flow. It is not desirable to morph between FB and HB abruptly, as it may cause high overshoots or undershoots in voltage and current transients [14]. Considering the battery charging profile in Fig. 6, G increases as V_o gradually increases for a given V_{in}. If $G < G_{TM}$, during the converter start-up, it will start in HB mode and switch



(a) G = 1.8, V_o = 450 V, I_o = 2 A (b) G = 1, V_o = 450 V, I_o = 2 A (c) G = 0.93, V_o = 450 V, I_o = 2 A

(d) G = 1.8, V_o = 450 V, I_o = 7.3 A (e) G = 1.05, V_o = 350 V, I_o = 7.3 A (f) G = 0.94, V_o = 250 V, I_o = 7.3 A

FIGURE 12. **Frequency response of compensated loop gains of current and voltage loops at varying G and I_o.**

TABLE 9. **Comparison Among State-of-the-Art Closed-Loop Controls Implemented for LLC Converters**

Ref.	V_{in}/ V_o/ P_o	G	f_s, (f_r)	Closed-Loop Control Structure	DSP	Control Frequency
[27]	325–400 V/ 250–500 V/ 15 kW	0.63–1.54	109–140 kHz, (140.6 kHz)	Cascaded dual loop control with PI controllers and gain scheduling for inner current loop. Frequency control output and frequency saturation limits are feedforwarded from LUTs	STM32G474VE	20 kHz
[44]	240 V 24 V/ 200 W	1.00	0–300 kHz, (112 kHz)	Cascaded dual loop control with PI controllers	TMS320F28335	10 kHz
[45]	400 V/ 12 V/ 1 kW	0.96	(500 kHz)	OTC with adaptive SR control	TMS320F28027	167 kHz
[26]	120 V/ 18–34 V/ 150 W	0.8–1.51	70–150 kHz, (98 kHz)	Cascaded dual loop control with PI controllers	-	-
This work	**300–700 V/ 250 - 450 V/ 3.3 kW**	**0.5–1.8**	**44–161 kHz, (100 kHz)**	**Cascaded dual loop control with OTM, PI controllers and regression model based gain scheduling for inner current loop**	**TMS320F28379D**	**100 kHz**

to FB mode at a specific V_o when $G = G_{TM}$. Hence, the analysis in this Section is provided with respect to HB morphing to FB, as it is the most common scenario during battery charging.

OTM is simulated in PLECS using the converter model with the optimized ratings in Table 8. The voltage and current waveforms during an abrupt morphing from HB to FB is given inFig. 14(a). The converter operates at 45kHz during HB and 137kHz during FB as G changes from 1.8 to 0.9. V_o overshoots to double the reference voltage level and causes an increase in i_p by threefold and v_c by twofold. Hence, for a smooth transition from HB to FB modes and vice-versa, OTM

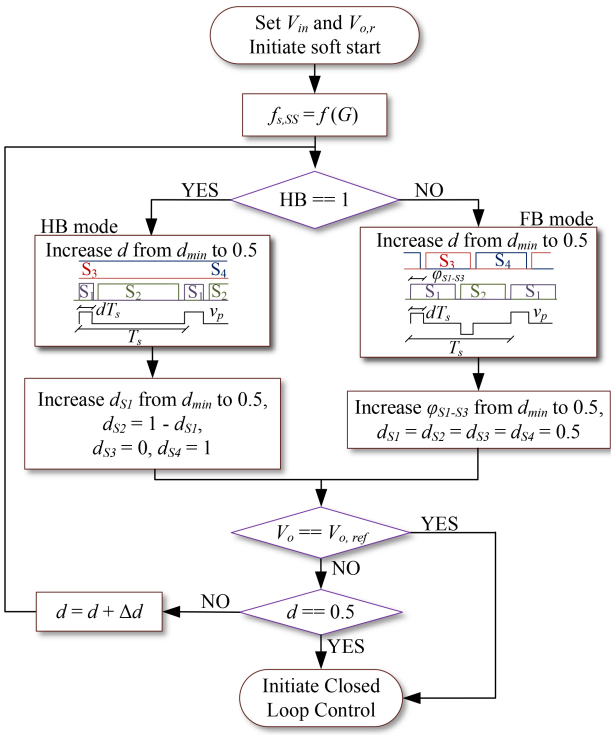


FIGURE 13. Soft start scheme for FB and HB operation.

techniques use duty ratio control along with the linearized compensators for FM [16]. The objectives of a smooth OTM technique are listed below:

- Uninterrupted power flow to the load.
- Tight regulation of V_o with minimal overshoot/ undershoot ($\leq 5\%$) and a stable closed-loop FM.
- Transformer AC currents i_p and i_s are within the maximum design margins and component ratings.
- i_m is within limits to avoid transformer core saturation.
- v_c is not exceeding the design limits during the morphing period.

An asymmetrical duty ratio variation method, as illustrated in Fig. 15(a) for OTM, was proposed in [14]. This method has the drawback of asymmetrical bridge voltages and currents, posing the risk of transformer core saturation due to a DC offset in i_m. To mitigate this, a symmetrical duty variation method is proposed in this work as seen in Fig. 15(b). However, this method has the drawback of higher AC RMS currents during TM compared to the asymmetrical method. The rest of this Section analyzes the two methods and provides a methodology to select the best OTM technique based on the converter parameters.

Digital implementation of OTM also depends on the DSP modulation scheme. The DSP modulation scheme adopted in this work uses two high-resolution ePWM modules as ePWM1 and ePWM2 to generate complementary PWM gate signals for leg 1 (S_1 and S_2) and leg 2 (S_3 and S_4), respectively. The up-counting mode, which counts up to the timer base period (TBPRD) value to produce PWM gate signals with frequency f_s, is used in both ePWM modules, with set and clear functions for the PWM signals are determined based on the compare register outputs CMPA and CMPB. The TBPRD determines f_s and is computed in the closed-loop control loop as below:

$$TBPRD = \frac{f_{clk}}{f_s} - 1 \tag{10}$$

where $f_{clk} = 100$MHz is the clock frequency of the ePWM module in TMS320F28379D. The top MOSFET of each leg is set high when the counter value is equal to the corresponding CMPA value and is set low when the counter value is equal to the corresponding CMPB value. Hence, the phase shift and duty ratio of the gate signals can be varied through user defined logic. A timing diagram for the implemented modulation scheme in FB and HB modes is provided in Fig. 16. The saw tooth waveform represents the up-counter in the ePWM modules with the relevant CMPA and CMPB values.

A. ASYMMETRICAL DUTY RATIO VARIATION METHOD

The asymmetrical duty ratio variation method for OTM was first proposed in [14]. The modulation waveforms when morphing from HB to FB, along with v_p, are given in Fig. 17. The duty ratio of the negative half cycle is gradually increased from 0 to 0.5 by increasing d_{S3} from 0 to 0.5 and decreasing $d_{S4} = 1 - d_{S3}$ in a complementary fashion. To ensure a smooth transition while maintaining tight output voltage regulation with cascaded closed-loop control, a long morphing duration (t_{TM}) in the range of 100ms is considered [28]. The duty ratio of S_3 and S_4 are varied by gradually increasing/ decreasing the respective comparator register values in the ePWM module one by one [14]. During OTM, the closed-loop control continues to regulate V_o through FM.

Simulation results of the asymmetrical duty variation method are given in Fig. 14(b). It is seen that asymmetrical v_p is causing DC offset in currents i_p, i_s, and i_m. The DC offset in i_m poses the risk of core saturation [46]. In [14], the authors reported a maximum of 70% increase in $i_{m,pk}$ compared to its steady-state value. The additional flux density caused by the DC component (B_{DC}) in i_m can be calculated using (11), where $I_{m,DC}$ is the maximum DC offset in i_m, μ is the permeability of the core, N_p is the number of turns in the primary, and l_e is the magnetic path length of the core [47].

$$B_{DC} = \frac{\mu N_p I_{m,DC}}{l_e} \tag{11}$$

To avoid core saturation, the sum of the maximum AC and DC flux densities of the core should be less than the saturation flux density of the core:

$$B_{sat} > B_{DC} + B_{AC} \tag{12}$$

AC flux density (B_{AC}) can be computed from (13), where d is the duty ratio of v_p and A_c is the effective cross-section

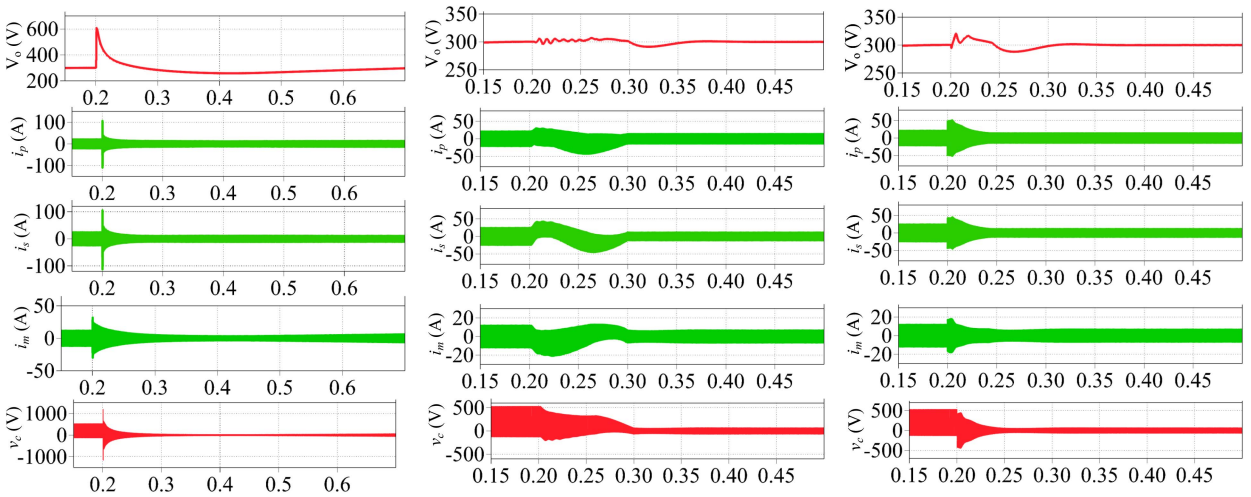


FIGURE 14. PLECS simulation results for OTM methods at $V_{in} = 400$ V, $V_o = 300$ V, $I_o = 7.3$ A.

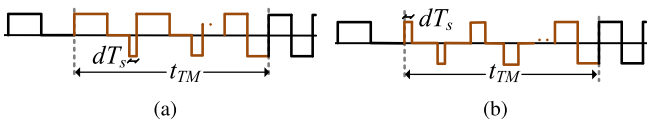


FIGURE 15. Primary bridge voltage in (a) asymmetrical and (b) symmetrical duty variation methods of OTM from HB to FB.

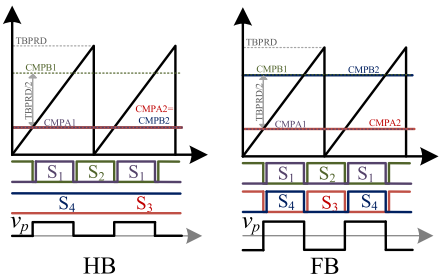


FIGURE 16. PWM scheme for FB and HB operation with up-count mode in ePWM modules.

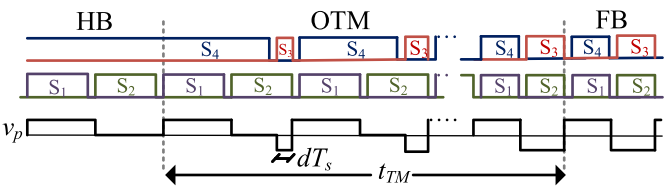


FIGURE 17. Asymmetrical duty variation method.

area [48].

$$B_{AC} = \frac{dV_{in}}{2f_s N_p A_c} \tag{13}$$

Hence, using (11)–(13) and transformer parameters, the design limit for $I_{m,DC}$ can be computed as derived in (14). To avoid core saturation $I_{m,DC} < I_{m,DC,limit}$ should be satisfied.

$$I_{m,DC,limit} = \left(B_{sat} - B_{AC,\max}\right) \frac{l_e}{\mu N_p} \tag{14}$$

A LUT-based OTM technique is implemented in [28] to minimize the DC offset in magnetizing current. It changes the duty ratio of both positive and negative half cycles of v_p to minimize i_m. The optimal duty ratio of the positive half cycle for the gradually increasing duty ratio of the negative half cycle of v_p is calculated offline and stored in LUTs in the control system. However, due to the limitations imposed by LUTs, as previously discussed in Section III, a symmetrical duty ratio variation method is proposed in this work to prevent the DC offset in i_m while avoiding the use of LUTs.

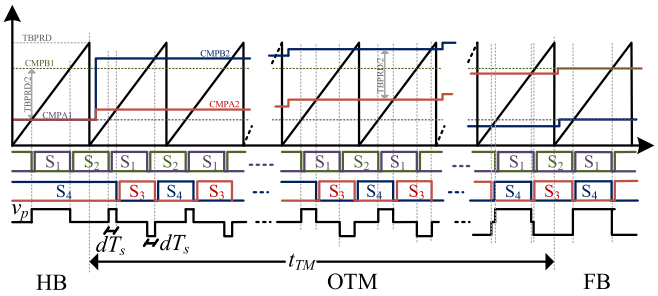


FIGURE 18. Symmetrical duty variation method († TBPRD is not to scale).

B. SYMMETRICAL DUTY RATIO VARIATION METHOD

The modulation waveforms for the proposed symmetrical duty ratio variation method when morphing from HB to FB are presented in Fig. 18. At the morphing command from HB

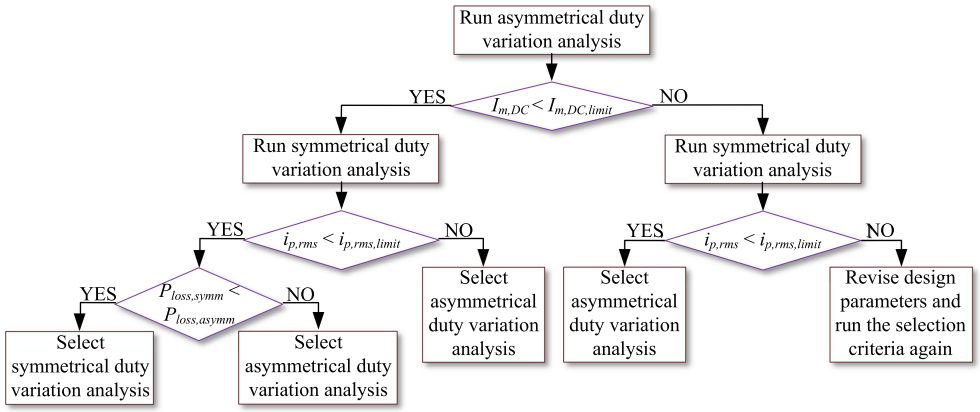


FIGURE 19. Framework for selecting the best OTM technique out of asymmetrical and symmetrical duty variation methods.

TABLE 10. Comparison Between Asymmetrical and Symmetrical Duty Variation Methods in Terms of Maximum Absolute Values and Percentage Compared to Maximum Component Ratings

	HB Steady State Values	Max. Component Ratings	Max. Values in Simulation Results				Max. Values in Experimental Results			
			Asymmetrical		Symmetrical		Asymmetrical		Symmetrical	
				%		%		%		%
V_o	300 V	1.2 kV (Diode)	308 V	26%	314.2 V	26%	316 V	26%	324 V	27%
$i_{p,RMS}$	12.7 A	43 A (C_r)	13.8 A	32%	20.9 A	49%	13.4 A	31%	20 A	47%
$I_{m,DC}$	0 A	15.24 A	7.3 A	48%	0 A	0%	4.96 A	33%	0 A	0%
$v_{c,RMS}$	287.4 V	530 V at 80 kHz †	283 V	53%	321.6 V	61%	288 V	54%	337 V	64%

† $f_s < 80$ kHz at the instance maximum $v_{c,RMS}$ is observed during OTM.

to FB, S_3 and S_4 operate with 50% duty cycle and the phase shift φ_{S1-S3} between S_1 and S_3 is set to the bridge voltage duty ratio d, which increases from a pre-calculated duty (d_{HB}) to 0.5. This will result in a symmetrical bridge voltage v_p.

d_{HB} is calculated to ensure V_o can be regulated to $V_{o,r}$ at the same f_s as HB. This duty ratio value can be estimated from FHA and verified using an open loop simulation model. Since TM occurs at a fixed gain (i.e., in this design example at $G = 0.9$), the pre-calculated value for d_{HB} can be fixed for the entire operating region.

Simulation results of the asymmetrical duty variation method are given in Fig. 14(c). Higher currents compared to asymmetrical duty variation method are observed. However, all the voltages and currents are symmetrical avoiding a DC offset in i_m.

C. COMPARISON BETWEEN ASYMMETRICAL AND SYMMETRICAL METHODS

As alluded to before, there are trade-offs in the conventional asymmetrical and proposed symmetrical OTM methods. A comparative analysis between the asymmetrical and the proposed symmetrical duty ratio variation methods is provided in Table 10.

The output voltage overshoot in both asymmetrical and symmetrical techniques are $\leq 5\%$. However, it can be observed that the asymmetrical duty ratio method has the disadvantage of DC offset in i_m, posing the risk of transformer saturation, while the symmetrical duty variation method has the disadvantage of comparatively higher resonant tank currents. Nevertheless, the digital implementation of both OTM techniques is simple and does not require memory allocation for LUTs.

The appropriate OTM technique can be selected based on the limits of the component ratings. A framework for choosing the most suitable OTM technique out of the asymmetrical and symmetrical duty variation methods is provided in Fig. 19. Since the analytical functions to estimate the worst case $I_{m,DC}$ and $i_{p,RMS}$ during OTM are challenging to derive, the design engineer can rely on simulation-based results to assess the worst case. Hence, the most suitable OTM technique can be selected based on the one that generates the currents within the design limits. If both techniques satisfy the design limits, then the power loss generated during OTM can be estimated as per Table 6 and compared to select the technique with the lowest power loss.

In the case of this design example, both asymmetrical and symmetrical duty variation methods have their worst case currents and voltages well below the maximum component

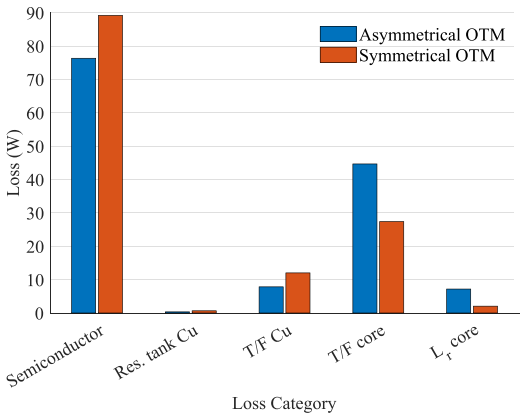


FIGURE 20. Loss comparison between asymmetrical and symmetrical duty variation methods during OTM.

ratings. Hence, a loss analysis between the two OTM techniques is conducted to find the technique with lowest losses. The loss comparison between asymmetrical and symmetrical duty variation methods during OTM is illustrated in Fig. 20. The ohmic and switching losses of the symmetrical method are higher than those of the asymmetrical method due to higher RMS currents. The transformer and inductor core losses in the asymmetrical OTM method are higher than those of the symmetrical method due to the DC-offset. The power loss during OTM with asymmetrical technique is estimated to be 136W, while that with symmetrical technique is 131 W, when $P_o = 2.2$ kW. Therefore, symmetrical technique is preferred over the asymmetrical technique as it has lower power loss. However, experimental results for both asymmetrical and symmetrical duty variation methods are provided.

V. EXPERIMENTAL VALIDATION

This Section provides the experimental results for the validation of the optimized LLC converter design, closed-loop control design, and OTM techniques.

A. DESIGN OPTIMIZATION APPLICATION

The hardware demonstrator is built based on the converter design parameters given in Table 8. The converter operation is validated through wide voltage range operation. The waveforms of bridge voltages and AC currents under FB and HB operation for buck ($G = 1.35$ and 1.8), boost ($G = 0.96$), and unity ($G = 1$) voltage gain operation over the wide voltage range are given in Fig. 21.

The waveforms of v_c during FB and HB operation at maximum voltage gain point ($G = 1.8$) are given in Fig. 22. A DC offset of $V_{in}/2$ is observed in v_c during HB operation, increasing its RMS voltage compared to FB operation, even though the converter operates at the same load. Based on the TDA analysis presented in Section II, a worst case $v_{c,RMS}$ of 398.6 V is also observed at the maximum voltage gain point: $V_{in} = 600$ V (HB), $V_o = 450$ V, and $I_o = 7.3$ A. $v_{c,RMS}$ observed during experiments at the same operating point as seen in Fig. 22(b) is 388 V, validating the TDA model with $< 3\%$ error margin.

1) SOFT START AND CLOSED-LOOP CONTROL

The soft start scheme presented in Fig. 13 is implemented in this work to start the converter in both FB and HB. Waveforms for FB modes are provided in Fig. 23. A smooth transition from soft start to closed-loop control with stable voltage regulation is observed. To validate the dynamics of the closed-loop control, a voltage reference change is applied from 300V to 350V, and the relevant waveforms are presented in Fig. 24.

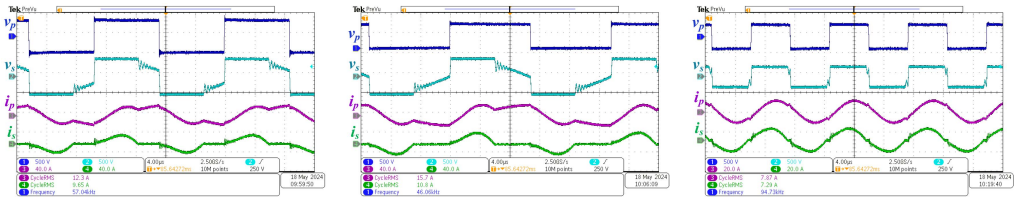
2) EFFICIENCY EVALUATION

The efficiency of the hardware prototype is evaluated over the wide voltage range using a Zimmer precision power analyzer (LMG 671). A DC electronic load (NHR 4760) is used as the load. The efficiency map evaluated at varying voltage levels is given in Fig. 25(a). The TWAE calculated based on Fig. 6 for the operating points listed in Table 7 at different V_{in} levels is provided in Fig. 25(b). Furthermore, the efficiency map at varying I_o and fixed voltage levels is provided in Fig. 25(c). A peak efficiency of 97.72% is observed at $V_{in} = 300$V, $V_o = 250$V, and $I_o = 7.3$A. However, instead of the peak efficiency, TWAE is a better metric at gauging the converter performance in OBC applications. A maximum TWAE of 96.98% is observed at $V_{in} = 400$V. It is also observed that TWAE is $> 96.7\%$ for the entire range of V_{in}. Fig. 25(b) also compares the TWAE between experimental results and the analytical model. The error in the TWAE estimate from the analytical model is within $\pm 1\%$.

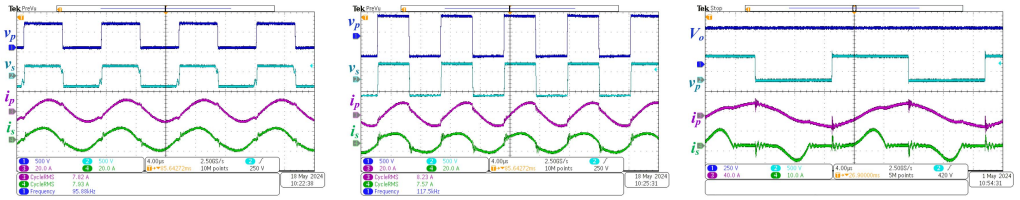
A comparison of wide voltage range LLC converter designs in literature with voltage ratings similar to this work is provided in Table 11. Compared to the available statistics, the proposed optimized design can attain higher TWAE without using additional devices.

B. ONLINE TOPOLOGY MORPHING

Considering the battery charging profile illustrated in Fig. 6, G increases as V_o increases for a given V_{in}. If $G < G_{TM}$, the converter initially operates in HB mode. When G reaches G_{TM} as V_o increases, the converter morphs from HB to FB mode. Hence, experiments are conducted during OTM from HB to FB at the operating point $V_{in} = 400$V, $V_o = 300$V, and $I_o = 7.3$A. The converter operates at $f_s = 44.45$kHz during HB and $f_s = 160.5$kHz during FB. Fig. 26 provides the waveforms for HB and FB operation over the same time scale as a baseline for the waveforms during OTM.

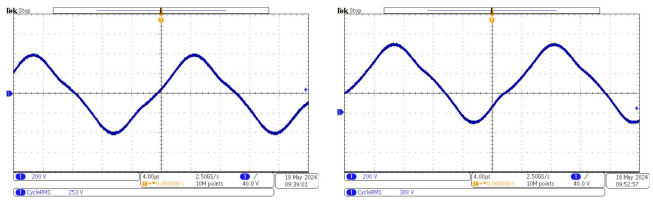


(a) V_{in} = 400 V (FB), V_o = 450 V (b) V_{in} = 600 V (HB), V_o = 450 V (c) V_{in} = 300 V (FB), V_o = 250 V



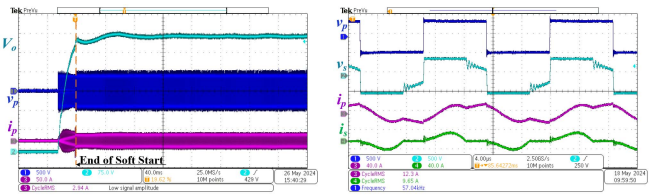
(d) V_{in} = 600 V (HB), V_o = 250 V (e) V_{in} = 500 V (FB), V_o = 400 V (f) V_{in} = 600 V (HB), V_o = 450 V, I_o = 2 A

FIGURE 21. Bridge voltage and current waveforms for (a), (b): $f_s < f_r$, (c): $f_s > f_r$, (d), (e): $f_s = f_r$ under I_o = 7.3 A load current, and (f): $f_s < f_r$ under I_o = 2 A.



(a) V_{in} = 300 V (FB) (b) V_{in} = 600 V (HB)

FIGURE 22. v_c during FB and HB at $f_s < f_r$, V_o = 450 V, I_o = 7.7.3 A.



(a) Soft start to closed-loop transition (b) Zoomed in view during soft start

FIGURE 23. Soft start with FB mode at V_{in} = 400 V, V_o = 450 V, I_o = 7.3 A.

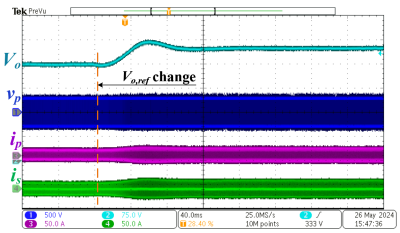


FIGURE 24. $V_{o,r}$ change from 300 V to 350 V at V_{in} = 300 V, I_o = 7.3 A, FB mode.

TABLE 11. Comparison Among Wide Voltage Range LLC Designs

Ref.	[49]	[50]	[51]	This work
V_{in} (V)	400	250–450	390	**300–700**
V_o (V)	250–430	400	10–420	**250–450**
P_o (kW)	2	0.5	1	**3.3**
f_s range (kHz)	47.2–100	95–140	100	**44–161**
Control	FM	FM	phase shift	**FM**
Peak Efficiency	97.5%	93.1%	98.1%	**97.72%**
TWAE	95.7%*	-	96.0%*	**96.93%** ‡
Primary + Secondary Devices†	6M+4D	6M+8D	4M+4D	**4M+4D**
Additional Passive Elements	1 inductor	1 capacitor	1 LLC tank	-

* Estimated from available efficiency maps

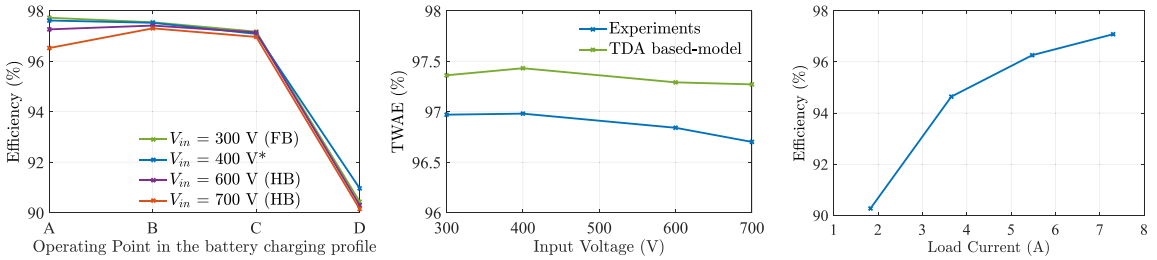
‡ Averaged over the entire V_{in} range

† MOSFETs (M) and diodes (D)

The waveforms for the asymmetrical duty variation scheme during OTM from HB to FB are provided in Fig. 27. Asymmetrical AC currents are observed in i_p, i_s, and i_m . A maximum DC offset of -4.96A is observed in i_m .

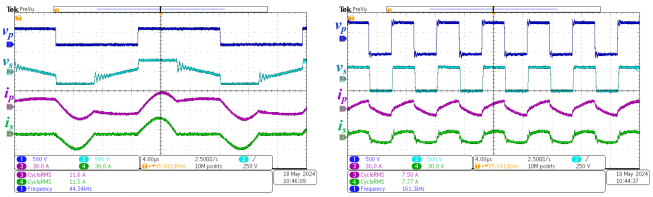
The waveforms for symmetrical duty ratio variation during OTM from HB to FB at the same operating point are provided in Fig. 28. Symmetrical AC currents are observed in i_p, i_s, and i_m without any DC offset. However, at the start of OTM, $i_{p,RMS}$ is 20A.

Table 10 also provides a quantitative comparison between two OTM techniques based on the experimental results with respect to the key objectives of smooth OTM discussed in Section IV. It can be observed that the results from the experiments closely correlate with those observed during the simulation.



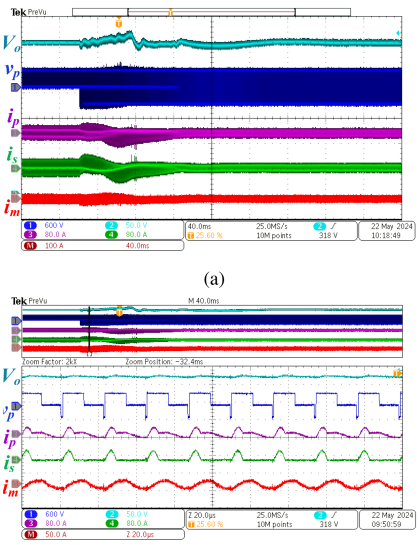
(a) Varying voltages at fixed I_o = 7.3 A (b) TWAE for varying V_{in} (c) Varying I_o at V_{in} = 400 V (FB), V_o = 450 V

FIGURE 25. Efficiency maps at varying voltages and load currents. (Operating points A–D of the battery charging profile are as per Table 7.) *HB at point A, FB at points B to D.



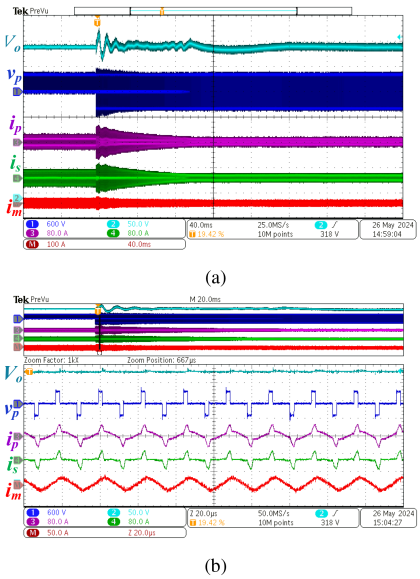
(a) HB (b) FB

FIGURE 26. Comparison between HB and FB operation at $G = 0.9$, $V_{in} = 400$ V, $V_o = 300$V, $I_o = 7.3$ A.



(a) (b)

FIGURE 27. OTM from HB to FB with asymmetrical duty variation.



(a) (b)

FIGURE 28. OTM from HB to FB with symmetrical duty variation.

VI. CONCLUSION

This paper presents an optimized LLC converter design with OTM control for wide voltage range OBC applications. The frequency modulated LLC converter benefits from TM between FB and HB to operate in a wide voltage range without the need of additional components. A design framework is proposed to find the optimal converter parameters (L_r, C_r, L_m, n, and f_r) to maximize its efficiency over a wide voltage range. Converter efficiency is analytically obtained using validated TDA and power loss models. A hardware demonstrator rated at 300–700 V input voltage, 250–450 V output voltage, and 3.3 kW maximum power for an OBC application is developed to validate the design optimization method.

Since the optimized LLC converter requires morphing the primary bridge between a FB and a HB without interrupting the power transfer, existing OTM techniques are assessed, and a novel symmetrical OTM technique is proposed. The objectives of a smooth OTM technique are identified as tight regulation of V_o, minimal increase in resonant tank voltages, and currents with limited DC offset in magnetizing current to avoid transformer saturation. A stable closed-loop control is also required to achieve smooth OTM. Hence, a cascaded dual loop controller design with an inner current loop and outer voltage loop is also presented. PI controllers are used for both voltage and current compensators. Adaptive gains in the current PI controller are used to provide V_o and I_o regulation over a wide voltage range. A regression model as a function of the voltage gain is proposed for current compensator gain

scheduling. The hardware demonstrator of the optimized LLC converter is used to validate the converter operation over a wide range of operating points.

The state-of-the-art OTM techniques proposed for LLC converters use asymmetrical duty variation methods and have the challenge of managing the DC offset in transformer magnetizing current due to asymmetric bridge voltages and currents. A new OTM technique with symmetrical duty variation is proposed to avoid asymmetrical currents. Simulation and experimental results to compare the asymmetrical OTM technique and the proposed symmetrical OTM technique are provided. It is observed that while the proposed symmetrical OTM method can get rid of DC offset in magnetizing current, it has higher resonant tank currents during the morphing duration compared to the asymmetrical method. A decision algorithm to select the optimal OTM technique based on the component ratings and power loss is also proposed. Both OTM techniques are validated through experiments.

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