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A Novel Reduced Switches Nine-Level Inverter Applicable in Aircraft Ground Power Unit

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ABSTRACT Ground power unit (GPU) converters are often required to efficiently manage power distribution in various ground-based applications, necessitating designs that balance performance, and cost-effectiveness. In this paper, a novel nine-level output converter using a single voltage source, 8 unidirectional and one bidirectional MOSFET switches, and two capacitors has been presented to utilize in GPUs. A simple modulation algorithm (PWM) has been applied to achieve a THD of 3.1% on the output voltage at 115/200 V and 400 Hz without the need for additional filtering. With a relatively small output filter, the THD is further reduced to less than 1%. The proposed converter utilized a lower number of devices to output a nine-level staircase in comparison to existing converters. Additionally, the proposed converter employs inherent self-voltage balancing for capacitor voltages, thereby simplifying the control algorithm. In this paper, the topology analysis, modulation algorithm, capacitor calculation, loss, efficiency, and performance analysis of the proposed topology have been presented. The proposed circuit has been compared to recently published papers in terms of switch, capacitor, diode, and source numbers. The theoretical and experimental performance of the topology has been verified by simulation on PSIM software and experimental setup.

INDEX TERMS Nine-level inverter, self-balancing capacitor, single voltage source, double capacitor, ground power unit.

I. INTRODUCTION

Since inception of multilevel inverters (MLI), their usage has expanded to several applications that need converting DC to AC voltage. Multilevel inverters are used in both high-voltage and low-voltage applications because of low total harmonic distortion (THD) and low power losses. The main advantages of multilevel inverters in comparison to two-level inverters are lower blocked voltage on the switches, lower THD, etc [1], [2], [3].

The output waveform of the multilevel inverters has an acceptable harmonic spectrum and so has higher voltage quality. Traditional topologies of MLIs use too many components, driver boards, isolated input voltages, and charge balance circuits that lead to higher prices of converter [4], [5]. In [6], by using two diodes, two capacitors, one inductor, and eight unidirectional switches a nine-level voltage waveform at the output has been proposed. No voltage control circuit is used for balancing the capacitor voltage. The topology is the combination of switched-capacitor and fly-capacitor topology. The maximum efficiency of the presented topology at 600 W output power is 96.6%.

The topology proposed in [7] is the combination of a T-type and active neutral point clamp (ANPC) circuit. The circuit consists of four capacitors, four unidirectional switches, and three bidirectional switches that make 9-level waveforms at the output. The maximum efficiency is 97.7%. In [8] authors proposed a nine-level inverter with two capacitors, nine unidirectional switches, two bidirectional switches, and an inductance. The proposed topology has capacitor voltage balancing capability. The total harmonic distortion of the converter at heavy load is 1.48%.

An improved quadruple boosting nine-level inverter presented in [9] uses ten unidirectional switches, three diodes, and two capacitors. The circuit has capacitor voltage balancing capability. The topology has the boosting capability to $4V_{in}$. Authors in [10] proposed a GaN-based interleaved fly

capacitor multilevel inverter that can be switched at higher frequencies. Topology uses 16 switches and 7 capacitors. The proposed topology at the power of 1.2 KW has a peak efficiency of 98.6%. A new nine-level inverter using eight switches, three capacitors, and two diodes was proposed in [11]. Capacitors voltage can be charged up to V_{in} and $0.5V_{in}$ without any auxiliary circuit. The proposed topology at the output power of 500 W has a maximum efficiency of 96.4%. In [12], authors proposed a nine-level inverter that has common ground capability by using nine switches, three capacitors, and a diode. The converter has voltage-boosting capability to $2V_{in}$. Also, the converter has 97.9% efficiency at the power of 570 W.

Paper [13] proposed a new topology using eight unidirectional switches, a bidirectional switch, two diodes, and three capacitors for making a nine-level output waveform. The converter boosts the voltage up to $2V_{in}$. Authors in [14] proposed a nine-level converter ten unidirectional switches, a bidirectional switch, and three capacitors. The converter has a boosting capability of up to $2V_{in}$ and don't need any additional circuits for balancing capacitor voltages. The peak efficiency of 96.4% was achieved at the power of 100 W.

For the ground power unit of the airplane (GPU), output voltages and currents of MLIs have low harmonic distortions. So, small-size output filter elements guarantee the quality of the output waveforms to be at the desired level of THD <= 3%. Also, a low voltage drop at the inverter outputs filter under 400 Hz operation is the result of small-size filter elements. Also, by using multilevel inverters in GPU applications, improving system poles and damping ratio is the result of small size inductance at the output filter [15], [16].

To achieve optimal output voltage performance in inverter systems, increasing the switching frequency and adjusting circuit parameters are common strategies used to reduce harmonics.

However, applying these methods to GPUs presents challenges, such as the limited switching capabilities of power semiconductor devices and a low carrier ratio (R_c), which is the ratio of the switching frequency to the operating AC frequency (400 Hz) in high-power applications.

Increasing the amounts of inductance and capacitance is one way to improve the quality of the output voltage; however, in such circumstances, the phase-frequency characteristic of the output will also vary, making it impossible to eliminate the phase imbalance. Larger values of circuit parameters result in a slow dynamic response, making it more difficult to control the converter dynamically.

To overcome the aforementioned problems in this paper, a nine-level inverter using a DC source, eight unidirectional switches, a bidirectional switch, and two capacitors are proposed for GPU application. Compared to the traditional topologies, the proposed topology has higher voltage levels with lower component numbers, notably improved harmonic content, decreased output *dv/dt*, decreased electromagnetic interference, smaller filter inductance, and increased carrier ratio. In addition, low switching and conduction power losses,

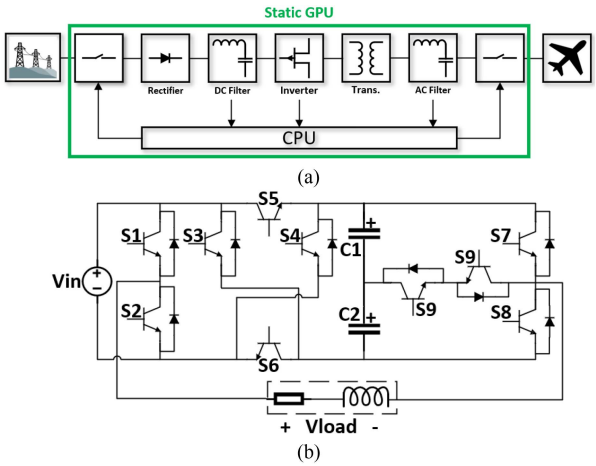


FIGURE 1. (a) Schematic diagram of static ground power unit, (b) Proposed circuit topology of the nine-level inverter.

enhanced efficiency, and high modularity are other important characteristics of the suggested multilevel converter. Also, the topology has the self-voltage balance capability of capacitors that simplifies the overall circuit topology and switching algorithm. A desired output voltage waveform can be synthesized from the multiple voltage levels with MLI. The major contributions of this paper are as follows:

1) Reduced component numbers in the proposed converter.
2) Self-balancing of capacitors voltage.
3) Application of proposed converter at GPU

The rest of the paper is organized as follows. The new topology is presented and analyzed in Section II. Capacitor calculation and loss analysis are presented in Section III-A comparison of the proposed topology with existing multilevels can be found in Section IV. Finally, simulation and experimental results are given in Section V.

II. STATIC GROUND POWER UNIT

A version of a solid-state frequency converter with an output of 115 V_{Phase}–400 Hz called static ground power unit (GPU). Thus, solid-state GPU offering low maintenance, lower price, and high efficiency, is one of the most promising converters for GPU usage in the aviation sector.

The static GPU (SGPU) comprises an LC filter, an isolation output transformer, and a power electronic inverter. An overview of the GPU hardware system is shown in Fig. 1(a). The input stage of the GPU, contains a power rectifier, in which the output is connected to a DC filter reducing the current ripple of the rectifier and also reducing the voltage ripples. An isolating transformer's primary winding is connected to the inverter, which receives power from the DC link. The output filter is attached to the transformer's secondary winding. The output voltage distortion is decreased by the output LC filter. GPU is a special power supply (inverter) unit that will be connected to the aircraft at the airports when the main motors of the aircraft are shut down. So, GPU will provide the required voltage and current to the aircraft

TABLE 1. Switching Pattern of Proposed Inverter

V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	C_1	C_2
+2	1	0	0	1	0	0	0	1	0	D	D
+1.5	1	0	0	1	0	0	0	0	1	D	-
+1	1	0	0	0	1	1	0	1	0	C	C
+0.5	1	0	0	0	1	1	0	0	1	C	C
+0	1	0	0	0	1	1	1	0	0	C	C
−0	0	1	0	0	1	1	0	1	0	C	C
−0.5	0	1	0	0	1	1	0	0	1	C	C
−1	0	1	0	0	1	1	1	0	0	C	C
−1.5	0	1	1	0	0	0	0	0	1	-	D
−2	0	1	1	0	0	0	1	0	0	D	D

to final check of electronic and electric equipment of the aircraft.

So, the static ground power unit could be modeled as a power source with a fundamental frequency of 400 Hz and high internal impedance from output filter inductance. At the main frequency, the voltage drop across filter and transformer leakage inductances will be significant, and harmonic currents will be intense. To guarantee a robust output voltage and lower THD in output voltage at various loads, the output impedance seen in the load must be as low as possible. To reduce the output current ripple, the LC filter is used at the output level of the solid-state converter where the L is up to 0.3 PU for 400 Hz converters and 0.05 PU for 50/60 Hz converters. So, the voltage drop at the output filter of the GPU system is 8 times more than the traditional inverter of 50 Hz. Based on MIL- STD704F (USA) standard for Air Plane Ground power units the output voltage must be in the range of 108–118 V, with THD of <= 3%, and output frequency should be in the range of 393–407 Hz.

III. PROPOSED NINE-LEVEL INVERTER

A. CIRCUIT TOPOLOGY

Fig. 1(b) shows the proposed circuit topology of the nine-level inverter which consists of a DC power supply, two electrolytic capacitors, eight unidirectional switches, and a bidirectional switch. By neglecting the voltage drops on switches, the proposed inverter has nine output voltage levels: $\pm 2V_{DC}$, $\pm 1.5V_{DC}$, $\pm 1V_{DC}$, $\pm 0.5V_{DC}$ and 0.

B. DESCRIPTION OF VOLTAGE LEVELS

The switching pattern list of the proposed inverter has been shown in Table 1. Also, to simplify the topology understanding, current paths are shown in Fig. 2.

Assumptions have been given as:

1) All power switches are ideal (on-state resistance and the forward voltage drops are zero).
2) Both capacitors have the same capacity and are large enough.
3) The load is pure resistance
4) The inverter reaches steady states.
5) Both capacitors are charged to $V_{DC}/2$.

Mode 1: Fig. 2(a), shows the first operating mode of the inverter. Switches 1, 4, and 8 are ON. So, the voltage of capacitors will be added to the DC power source voltage and make the voltage level of the $2V_{DC}$ at the output. In this mode the capacitors discharged.

Mode 2: Fig. 2(b), shows the second operation mode of the inverter. Switches 1, 4, and 9 are ON. Switch 9 is bidirectional. The voltage of the capacitor C_1 added to the input DC source voltage and made the voltage level $1.5V_{DC}$ at the output load. In this mode the capacitor C_1 discharged.

Mode 3: Fig. 2(c), shows the third operation mode of the inverter. Switches 1, 5, 6, and 8 are ON. In this mode, the capacitors are charged, and the voltage level of V_{DC} has been created at the inverter output.

Mode 4: Fig. 2(d), shows the fourth operation mode of the inverter. Switches 1, 5, 6, and 9 are ON. The load voltage level of $0.5V_{DC}$ is obtained by subtracting the capacitor C_2 voltage from the input source voltage. In this mode, the capacitors are charged.

Mode 5: Fig. 2(e), shows the fifth operation mode of the inverter. Switches 1, 5, 6, and 7 are ON. The load is short-circuited by switches 1, 5, and 7. So, the voltage level is zero. In this mode, the capacitors are charged.

C. MODULATION ANALYSIS

The operation principle of the proposed inverter has been shown in Fig. 3. The converter staircase output waveform can be synthesized by quasi-square signals $V_{oi}(i = 1, 2, 3, 4)$, with $\pm V_{DC}/2$ amplitudes and conducting angles $\theta_i(i = 1, 2, 3, 4)$. The angles should comply the (1).

$$0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 = 90 \tag{1}$$

For each quasi-square waveform, the Fourier decomposition can be expressed as:

$$V_{oi} = \frac{2V_{dc}}{\pi} \sum_{a=1,3,\ldots}^{\infty} \frac{\cos(a\theta_i)}{a} \sin a\omega t \tag{2}$$

Where ω is the angular frequency of the output waveform. So, the output voltage Fourier decomposition is:

$$V_o = \frac{2V_{dc}}{\pi} \sum_{a=1,3,\ldots}^{\infty} \sum_{i=1}^{4} \frac{\cos(a\theta_i)}{a} \sin a\omega t \tag{3}$$

From (3), the fundamental component of the output waveform can be extracted as:

$$V_{of} = \frac{2V_{dc}}{\pi} \sum_{i=1}^{4} \cos\theta_i \sin \omega t \tag{4}$$

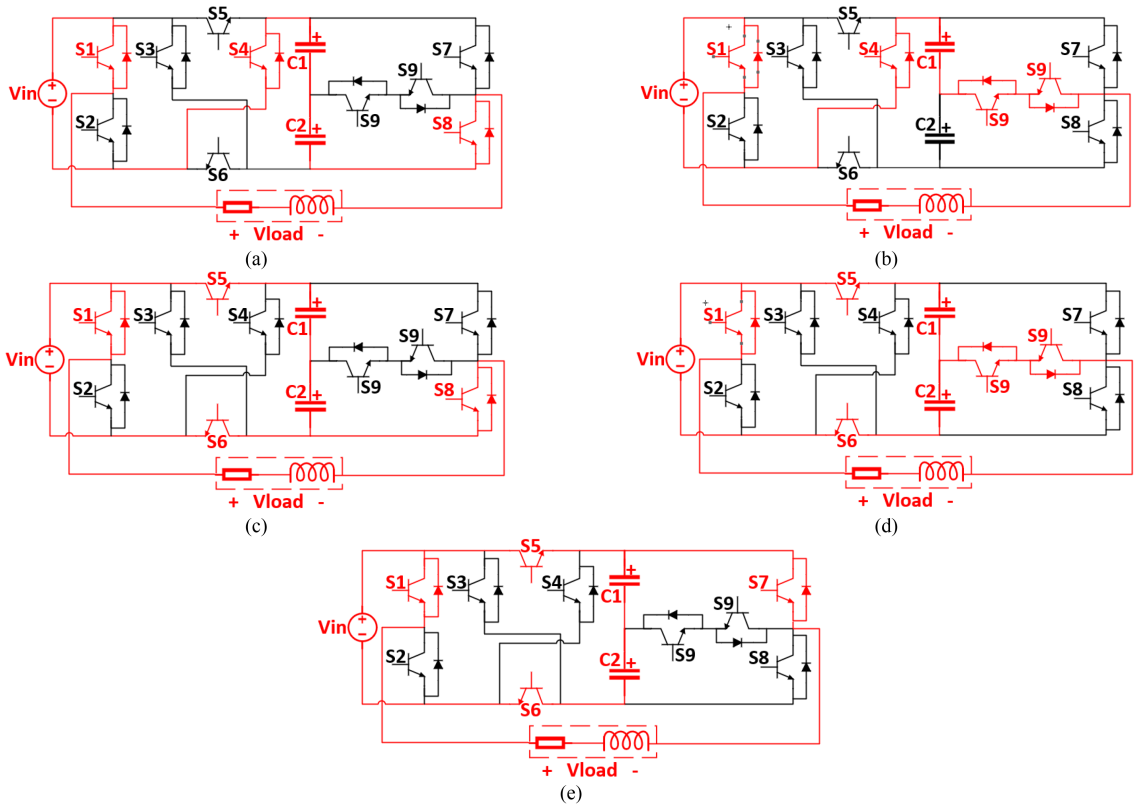


FIGURE 2. Switching patterns at the level of (a) $2V_{DC}$, (b) $1.5V_{DC}$, (c) V_{DC}, (d) $0.5V_{DC}$, (e) 0^{+}.

Hence, the modulation index amplitude of the fundamental waveform, M_{of} can be expressed as:

$$M_{of} = \frac{1}{4}\sum_{i=1}^{4}\cos\theta_i \tag{5}$$

Also, the THD of the proposed inverter can be expressed as:

$$THD = \frac{\sqrt{\sum_{a=3,5,\ldots}^{\infty}\left[\sum_{i=1}^{4}\frac{\cos(a\theta_i)}{a}\right]^2}}{\sum_{a=1}^{4}\cos(\theta_a)} \times 100\% \tag{6}$$

By using the selected harmonic elimination method, the 5th, 7th, and 11th harmonics can be eliminated. So, the conducting angles $\theta_i (i = 1, 2, 3, 4)$ can be calculated by the related equations as shown below:

$$\begin{cases} \mathrm{Cos}(\theta_1) + \mathrm{Cos}(\theta_2) + \mathrm{Cos}(\theta_3) + \mathrm{Cos}(\theta_4) = 4M_{0f} \\ \mathrm{Cos}(5\theta_1) + \mathrm{Cos}(5\theta_2) + \mathrm{Cos}(5\theta_3) + \mathrm{Cos}(5\theta_4) = 0 \\ \mathrm{Cos}(7\theta_1) + \mathrm{Cos}(7\theta_2) + \mathrm{Cos}(7\theta_3) + \mathrm{Cos}(7\theta_4) = 0 \\ \mathrm{Cos}(11\theta_1) + \mathrm{Cos}(11\theta_2) + \mathrm{Cos}(11\theta_3) + \mathrm{Cos}(11\theta_4) = 0 \end{cases} \tag{7}$$

If we assume $M_{of} = 0.8$, the related conducting angles can be obtained as:

$$\theta_1 = 9.84^{\circ},\ \theta_2 = 20.37^{\circ}$$
$$\theta_3 = 40.05^{\circ},\ \theta_4 = 60.42^{\circ} \tag{8}$$

By applying the calculated angles to Fig. 3, the appliable switching waveforms to the switches $S_1 - S_9$ can be obtained. Also, by placing (7) in (6), the theoretical THD of the proposed inverter can be expressed as 3.13%.

D. VOLTAGE STRESS ON SWITCHES

Voltage Stress on switches can be investigated by the maximum voltage on the switch when it is OFF. As can be calculated from Fig. 2 the maximum voltage on the switches 3, 4 are $V_{Max,OFF} = 2V_{DC}$, the maximum voltage on the switches 1, 2, 5, 6, 7, 8 are $V_{Max,OFF} = V_{DC}$ and the maximum voltage on switch 9 is $V_{MaxOFF} = {}^{V_{DC}}/_{2}$.

E. MODULATION STRATEGY

Different modulation methods are used in different multi-level inverters to generate a semi-sinusoidal staircase waveform at the output. In this paper, a phase disposition PWM (PD-PWM) technique has been used for generating the gate signals of the switches. Simplicity and lower THD are the main advantages of this method.

III. LOSS ANALYSIS AND CAPACITOR CALCULATION

A. CAPACITOR DESIGN AND RIPPLE LOSS ANALYSIS

Maximum voltage ripple on capacitors must be limited to less than 10% of the maximum voltage on the capacitor that appears when capacitors in the proposed topology discharge to the load in series with the voltage source [17]. Capacitor

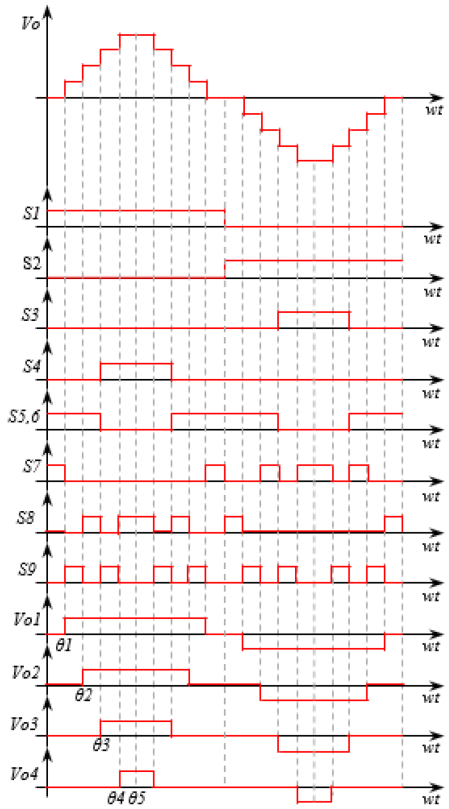


FIGURE 3. Switching patterns and the output voltage at each voltage level.

capacitance, discharge period, and load type are determined by the range of voltage fluctuation. It is obvious from Table 1 and Fig. 3 that the largest discharge period in the positive half cycle occurs from θ_3 to $\pi - \theta_3$, when the output voltages are $+2V_{DC}$ and $+1.5V_{DC}$. Also in the negative half cycle, the largest discharge period occurs when the output voltages are -$2V_{DC}$ and -$1.5V_{DC}$. From the current path in Fig. 2, The two capacitors have the same discharge current that is assumed as i_o and $i_o/2$ for the output voltage of $\pm 2V_{DC}$ and $\pm 1.5V_{DC}$ respectively. So, the maximum continues discharging value of each capacitor during θ_3 to $\pi - \theta_3$ can be calculated as:

$$\Delta Q = \int_{\theta_3}^{\theta_4} \frac{i_o}{2\omega} d\omega t + \int_{\theta_4}^{\pi-\theta_4} \frac{i_o}{\omega} d\omega t + \int_{\pi-\theta_4}^{\pi-\theta_3} \frac{i_o}{2\omega} d\omega t \quad (9)$$

The largest discharge value and maximum voltage ripple because of aligning the peak of load current with the midpoint of the discharging period occurs when the load is pure resistance. So, the calculated capacitance value in the pure resistance condition will be larger than when the inductive load is applied. By assuming the pure resistance load, the load current and load voltage waveform are staircase waveforms. So, (9) can be simplified as:

$$\Delta Q = \frac{V_{dc}}{4\pi f_o R_o} (4\pi - 3\theta_3 - 5\theta_4) \quad (10)$$

where f_o is the output voltage frequency and R_o is the resistance load value.

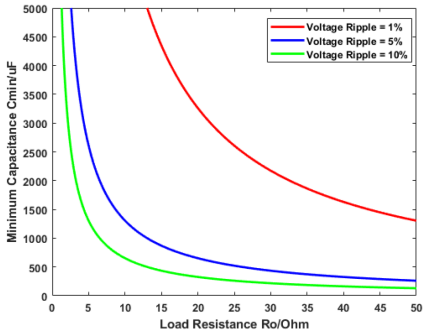


FIGURE 4. Load resistance versus minimum capacitance at the frequency of 400 Hz.

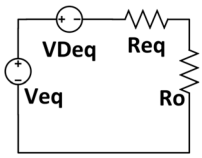


FIGURE 5. Equivalent current path.

Hence, the voltage ripple on each capacitor can be calculated as:

$$\Delta V = \frac{V_{dc}}{4\pi f_o R_o C} (4\pi - 3\theta_3 - 5\theta_4) \quad (11)$$

Where C is the capacitance of each capacitor. If we assume the maximum allowable voltage ripple on the capacitors is ΔU_{Ripple}, the minimum capacitor value calculated as:

$$C_{\min} = \frac{V_{dc}}{4\pi f_o R_o \Delta U_{Ripple}} (4\pi - 3\theta_3 - 5\theta_4) \quad (12)$$

Fig. 4 expresses the relation of load resistance versus minimum capacitance and output frequency. As it can be seen, to keep the voltage ripple in the allowable range, capacitance size will be increased by increasing output power. Also, by increasing the output frequency the required capacitance will decrease. So, the loss related to ripple can be expressed as:

$$P_{Rip} = f_0 C \Delta V^2 \quad (13)$$

B. CONDUCTING LOSS ANALYSIS

Parasitic parameters such as on-state resistance of switches, and forward voltage drops of diodes lead to conduction loss. The equivalent current path is shown in Fig. 5 where V_{equ} shows output voltage, V_{Dequ} shows voltage drop on the diode, R_{eq} shows equivalent parasitic resistance and R_o shows load resistance. For simplicity, all the switches are the same and have the same r_s and all the body diode of switches are the same and have the same voltage drop of V_D and internal resistance of r_D. From the analysis of Section II, under pure resistance load conditions, the equivalent parameters can be

TABLE 2. Detailed Parameters of Each Switch

Parameters	S_1, S_2	S_3, S_4	S_5, S_6	S_7, S_8	S_9
V_{bsw}	V_{DC}	$2V_{DC}$	V_{DC}	V_{DC}	$V_{DC}/2$
f_s	f_o	f_o	$2f_o$	f_o	$2f_o$

calculated as:

$$V_{equ} = \begin{cases} 0 & i = 0 \\ V_{DC}/2 & i = 1 \\ V_{DC} & i = 2 \\ 3V_{DC}/2 & i = 3 \\ 2V_{DC} & i = 4 \end{cases} \tag{14}$$

$$V_{Dequ} = \begin{cases} V_D & i = 0, 2, 3 \\ 2V_D & i = 1 \\ 0 & i = 4 \end{cases} \tag{15}$$

$$r_{eq} = \begin{cases} r_D + r_S & i = 0 \\ \frac{3r_D + ESR_c}{2} + 2r_s & i = 1 \\ r_D + 3r_S & i = 2 \\ \frac{r_D + ESR_c}{2} + 3r_s & i = 3 \\ 2ESR_c + 4r_S & i = 4 \end{cases} \tag{16}$$

where ESR_c is the equivalent series resistance of the capacitor and i can be expressed as:

$$i = \left| \frac{2V_o}{V_{DC}} \right| \tag{17}$$

From Figs. 3 and 5, the average conduction loss can be calculated as:

$$P_{con} = \frac{2}{\pi} \sum_{i=1}^{4} \left\{ \left(\frac{V_{equ} - V_{Dequ}}{r_{eq} + R_o} \right)^2 \times r_{eq} \times (\theta_{i+1} - \theta_i) \right\} \tag{18}$$

In fact, ESR_c of the electrolytic capacitor is inversely proportional to the capacitor capacitance. So, increasing the capacitor capacitance can decrease the voltage ripple and ripple loss. Also, increasing the capacitor capacitance decreases the parasitic ESR_c that leads to decreasing the conduction loss of the capacitor. However, a trade-off between the capacitance and the price of the capacitor must be done.

C. SWITCHING LOSS ANALYSIS

An overlap in voltage and current waveforms in switching states causes switching losses. Switching losses can be estimated from charging and discharging of the parasitic capacitance between drain-source [20] as:

$$P_{Switch} = f_s C_{ds} {V_{bsw}}^2 \tag{19}$$

where f_s is switching frequency, C_{ds} is the parasitic capacitance of the drain source and V_{bsw} is the maximum block voltage of each switch. The value of f_s, C_{ds} and V_{bsw} has been shown in Table 2. Thus, the switching loss can be expressed as:

$$P_{Switch} = 8.5 f_o C_{ds} {V_{DC}}^2 \tag{20}$$

TABLE 3. Comparison of Proposed Topology With Other Past Structures

	$N_{Switch\ Uni}$	$N_{Switch\ Bi}$	N_{Diode}	N_{Cap}	N_{Ind}	$\eta\%$	V_{SwMsx}	THD
[6]	8	0	2	2	1	96.3	$2V_{DC}$	1%
[7]	4	3	0	2	0	96.5	$3V_{DC}$	8.7%
[8]	9	2	0	2	1	---	V_{DC}	1.2%
[9]	10	0	3	2	0	---	$2V_{DC}$	---
[10]	16	0	0	7	0	---	---	2%
[11]	8	0	2	3	0	96.3	1.5 V_{DC}	---
[12]	9	0	1	3	0	96.5	1.5 V_{DC}	---
[13]	8	1	2	3	0	96.2	V_{DC}	12.6%
[14]	10	1	0	3	0	97.1	V_{DC}	8.8%
[18]	9	1	0	2	0	---	V_{DC}	12.5%
[19]	9	0	2	2	0	83.5	$2V_{DC}$	3.1%
[20]	7	0	4	2	0	85.9	V_{DC}	0.8%
Pro.	8	1	0	2	0	95.3	$1.125V_{DC}$	0.9%

TABLE 4. Parameters of Proposed Topology

Parameters	Value
On-state resistance of the switches (R_{on})	550 $m\Omega$
Capacitance of Capacitors	1000 μF
Input DC Voltage (V_{DC})	80 V
Output Frequency (f_o)	400 Hz

So, the efficiency, in theory, can be calculated as:

$$\eta = \frac{P_o}{P_{Rip} + P_{Con} + P_{switch} + P_o} \tag{21}$$

where P_o is the output power of the proposed converter.

IV. COMPARISONS WITH EXISTING TOPOLOGIES

All proposed topologies in [17], [20], [21] uses switched capacitor techniques and can increase output waveform levels by increasing the component numbers. So, the comparison must be made between the converters with the same number of output voltage levels.

The comparison results under the same output voltage levels are listed in Table 3. The topology presented in [6] used eight MOSFETs, two diodes, two capacitors, and an inductor for producing nine-level waveforms at the output of the converter. The topology of [7] used four MOSFETs as unidirectional switches, three pairs of MOSFETs as bidirectional switches, and two capacitors for nine-level output. The topology in [8] used nine MOSFETs as unidirectional switches, two pairs of MOSFETs as bidirectional switches, two capacitors, and an inductor for producing the same level output waveform. The disadvantage of [6] and [8] is using inductors that will lead to more complexity, higher cost, and higher volume of converter. Paper [9] used ten MOSFETs as unidirectional switches, three diodes, and two capacitors. Ref. [10] used sixteen GaN switches and seven capacitors for

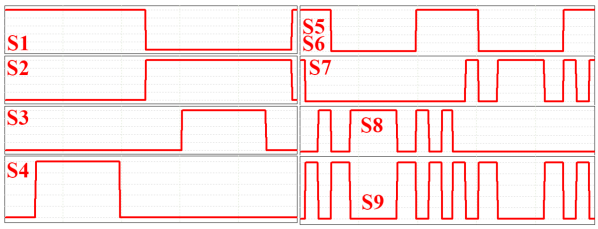


FIGURE 6. Waveforms of driving signals.

producing nine-level output. Authors in [18] proposed a nine-level inverter with 9 unidirectional switches, a bidirectional switch, and two capacitors. The advantage of this paper is using GaN switches that reduce the volume but have a cost disadvantage. The main disadvantage of [11], [12], [13], [14] is using three capacitors in topology that need extra volume and cost. Authors in [19] proposed a nine-level converter that has nine unidirectional switches with two diodes and two capacitors. The ground load isn't the same as the power supply of the converter.

From Table 3 it is obvious that our proposed nine-level inverter utilizes lower component counts compared to topologies proposed in [1], [3], [4], [5], [6], [7], [8], [9], [14], and [19] which will lead to smaller topology sizes, lower cost, higher reliability, and efficiency.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

To verify the performance of the proposed nine-level inverter, the PSIM platform has been utilized for simulation. The converter parameters for simulation are listed in Table 4. Simulation results of output voltage and gate signals of the power switches are shown in Fig. 6. As it can be seen from Fig. 6, switches 1, 2, 3, 4, 7, and 8 work at f_o and switches 5, 6, and 9 work at $2f_o$.

Fig. 7 shows the output voltage and current of the proposed converter. In Fig. 7(a), the load is pure resistance so the output voltage and current of the converter are in the same phase, the RMS value of the voltage is 115 V and the RMS value of the current is 3.3 A. Fig. 7(b) shows the output voltage and current at an R-L load of 35 $\Omega + 5$ mH.

As can be seen, the current is 20° lagging the voltage. Fig. 8(b) shows the output voltage, output current, and capacitor voltage under load change (dynamic condition) from 105 $\Omega + 55$ mH to 35 $\Omega + 5$ mH. As can be seen, when the load changes the output voltage remains the same, the load current increases, and the phase shift decreases.

B. EXPERIMENTAL RESULTS

To verify the performance of the proposed topology, an experimental prototype has been implemented as shown in Fig. 9. The parameters of the circuit are the same as in Table 4, and also the specification of the devices is listed in Table 5. The

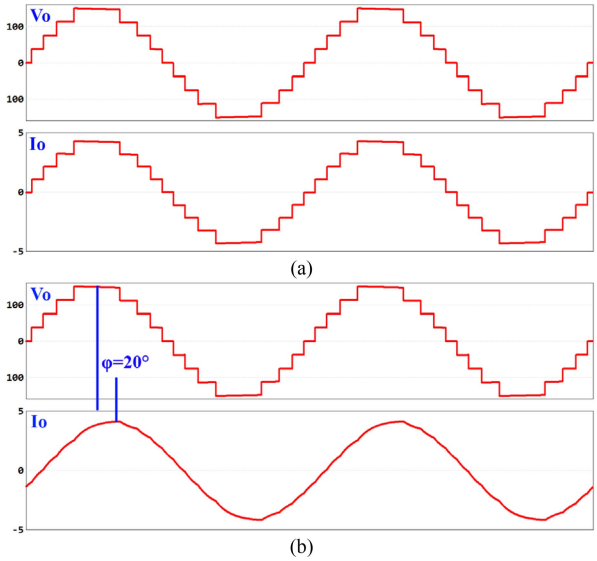


FIGURE 7. Simulation results of output voltages and currents under different load types. (a) $R_o = 35\Omega$. (b) $Z_L = 35\Omega + j12.5$ ($R_o = 35\Omega$, $L_o = 5$ mH, $\varphi = 20°$).

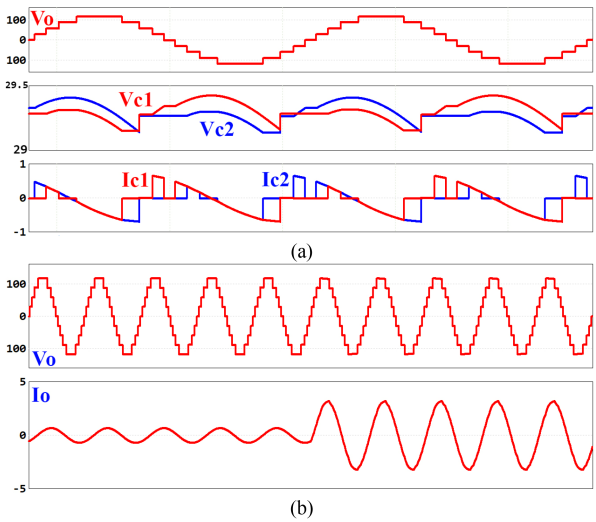


FIGURE 8. Simulation waveforms of (a) output voltage and capacitor voltages and currents, (b) output voltage and outputcurrent under load change.

experimental results of output voltage and current of the proposed converter under pure resistance load have been shown in Fig. 10(a).

The RMS value of the output voltage and current are 115/200 V and 3.1 A, respectively, with 400 Hz. In comparison with the simulation results, there is a small difference between output voltages and current magnitudes because of the parasitic elements and parameter tolerance. From the experimental results, the efficiency of the proposed topology is 95.3% which is less than the theoretical efficiency of 96.9% calculated by (20).

The experimental result of the converter with an R-L load of 35$\Omega + 5$ mH under a modulation index of 89% and with

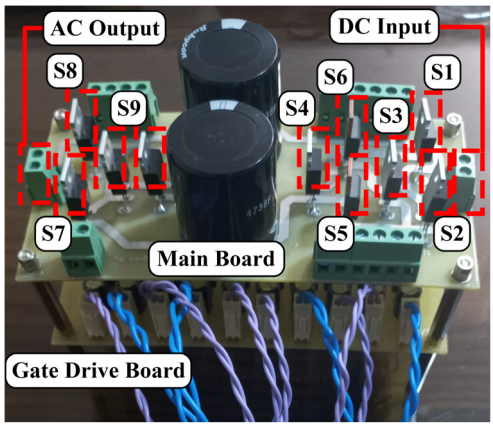


FIGURE 9. Experimental setup.

TABLE 5. Components of Experimental Setup

Devices	Specification
Switch $S_1, S_2, S_3, S_4, S_7, S_8, S_9$	HGTG12N60A4D
Switch S_5, S_6	GP10NC60K
Capacitor C_1, C_2	1000 µF
Controller	ATMEGA32A
Optocouplers	P521

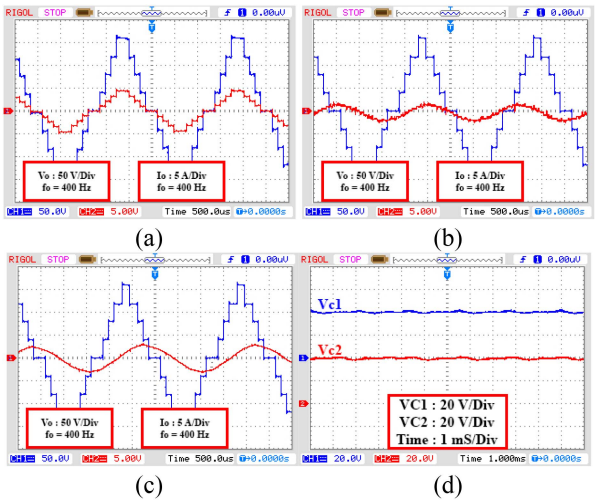


FIGURE 10. Experimental results of output voltage and current at (a) resistance load (*R*), (b) resistance inductance load (35Ω + 5 mH) and modulation index of 89%, (c) resistance inductance load (35Ω + 60 mH) and modulation index of 80%, and (d) capacitors voltage.

an R-L load of 35Ω + 60 mH under a modulation index of 80% are shown in Fig. 10(b) and (c), respectively. Also, by increasing the inductance of the load the phase shift of the current increased. Results of Fig. 10(c) confirm that the proposed circuit can handle high inductive loads, and the circuit can support reactive loads. The experimental results of both

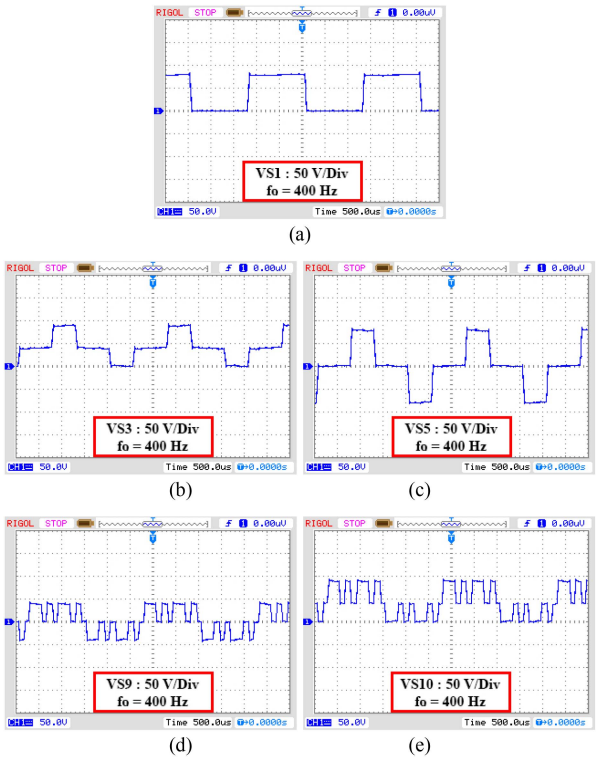


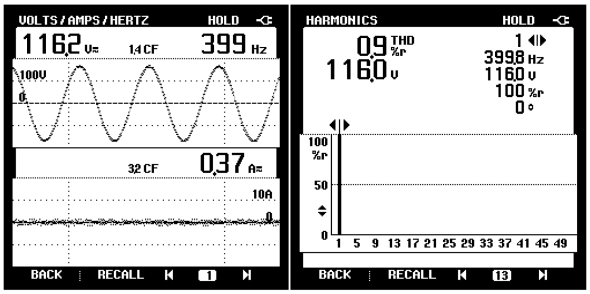
FIGURE 11. Experimental waveforms of voltages of switch: (a) S_1, (b) $S_{3,8}$, (c) S_5, (d) S_9, (e) S_{10}.

capacitor voltages have been shown in Fig. 10(d). The self-balancing of the capacitor's voltage has been approved in this figure with the voltage values of 40 V.

Fig. 11 shows the blocking voltage of the switches. As can be seen, the maximum voltage on S_1, S_3, S_5, S_9 and S_{10} are about 80V, 90V, 80V, 40V and 90V respectively. Because of using more switches in multi-level inverters, the output voltage is divided between the switches and so the voltage stress on the switches is low. In the proposed converter the voltage stress is 1.125 of input voltage and 0.55 of output maximum voltage.

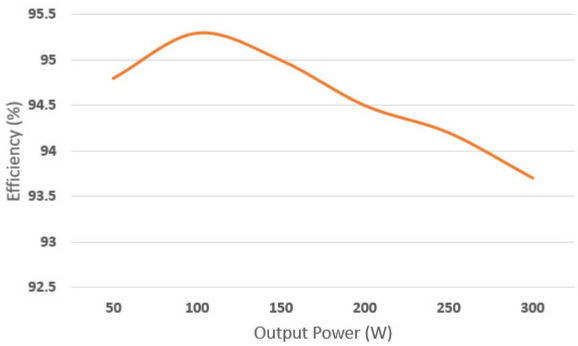
To fulfill the GPU standard requirements, a small L-C low pass filter with $C = 22\,\mu F$ and $L = 0.8$ mH with $f_c = 1.2$ kHz is used at the output of the converter. The experimental result of the output voltage and THD is shown in Fig. 12(a) and (b) respectively. It's obvious that by using a small filter at the output of the converter, the THD of the output voltage decreases to 0.9% with an RMS value of 115/200 V and frequency of 400 Hz that satisfy the GPU standards.

Fig. 13(a) shows the experimental efficiency of the proposed converter. As can be seen, the maximum efficiency is at 100 W output power. Also, Fig. 13(b) shows an efficiency comparison of some other topologies with the proposed topology. As can be seen, since the element numbers of our proposed topology are less than the element numbers of [19], and [22] so, it has a higher efficiency compared to [19], and [22].

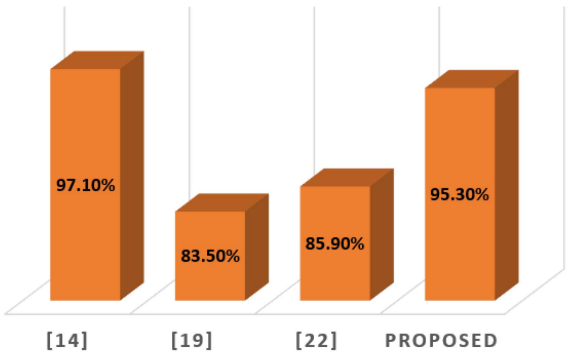


(a) (b)

FIGURE 12. Experimental waveforms of (a) Output voltage, (b) Total harmonic distortion (THD).



(a)



(b)

FIGURE 13. (a) Experimental efficiency of the proposed converter, (b) Experimental efficiency comparison of the converters at 100 W output power.

VI. CONCLUSION

In this paper, a novel nine-level converter including 8 bidirectional switches, one unidirectional switch, two capacitors, and a single voltage source is proposed for aircraft ground power unit (GPU). The proposed inverter in comparison with some recently proposed topologies utilizes lower component counts that will lead to smaller topology sizes, lower cost, higher reliability, and efficiency.

Also, the inherent voltage balance capability of the converter avoids unbalanced voltages on capacitors which leads to reduced converter size and cost and a simple modulation algorithm. Meanwhile, the proposed 9-level converter has a THD of 3.13% on the output voltage without utilizing any filter which is in line with related standards. By a relatively small LC filter, the THD has been reduced to 0.9% which is much less than the standard value of 3%. Switch stress analysis, capacitor calculation and loss analysis of the converter have been discussed in the paper.

Lower inductance size at the output of MLI will lead to lower voltage drop at the output filter and improved system poles and damping ratio. The main advantages of the proposed converter are listed as follows:

1) The number of switches has been reduced in comparison to similar converters with the same output level.
2) The THD value of the proposed topology approaches the range of related standards without the need for a filter, requiring only a small filter for further improvement.
3) Application of proposed inverter at GPU.

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